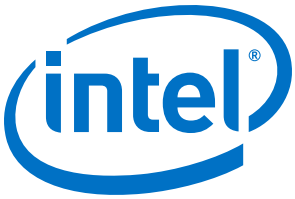

Intel® Stratix® 10 10GBASE-KR PHY IP Core User Guide

Updated for Intel® Quartus® Prime Design Suite: **19.2**

UG-20084 | 2019.07.19
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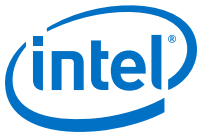

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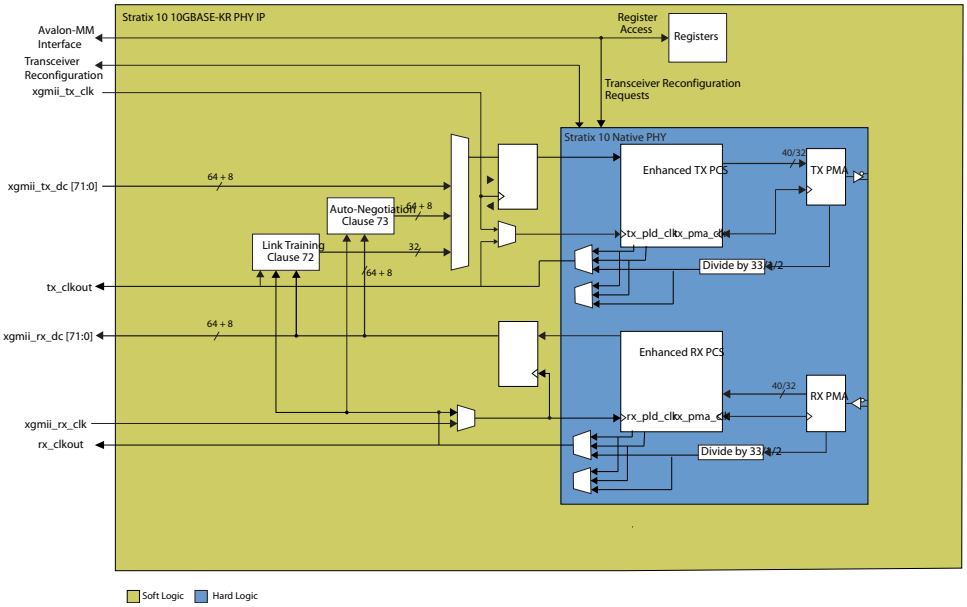
1. Datasheet

The Intel® Stratix® 10 10GBASE-KR PHY IP core implements the *IEEE 802.3 2015 Standard*.

Figure 1. Intel Stratix 10 10GBASE-KR Block Diagram



Related Information

- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- Generating a Combined Simulator Setup Script
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.

1.1. Intel Stratix 10 10GBASE-KR PHY IP Core Supported Features

The Intel Stratix 10 10GBASE-KR PHY IP core supports the following features:

- Auto-negotiation (AN) for backplane Ethernet as defined in *Clause 73 of the IEEE 802.3 2015 Standard*.
- 10GBASE-KR Ethernet protocol with link training as defined in *Clause 72 of the IEEE 802.3 2015 Standard*. In addition to the link-partner TX tuning as defined in *Clause 72*, this PHY also automatically configures the local device RX interface to achieve less than 10^{-12} bit error rate (BER) target.
- Forward error correction (FEC) as defined in *Clause 74 of the IEEE 802.3 2015 Standard*. This is an optional feature which provides an error detection and correction mechanism.
- The Intel Stratix 10 10GBASE-KR PHY IP core includes the following modules to enable operation over a backplane:
  - Auto-negotiation (AN)— The 10GBASE-KR PHY IP core can auto-negotiate between 10GBASE-KR, and 10GBASE-KR with FEC PHY types. The AN function is mandatory for Backplane Ethernet.
  - Link training (LT)— The LT mechanism allows the 10GBASE-KR PHY to automatically configure the link-partner TX PMDs for the lowest Bit Error Rate (BER).

Related Information

IEEE website
The IEEE 802.3 Standard 2015 is available on the IEEE website.

1.2. Device Family Support

Table 1. Intel FPGA IP Core Device Support Levels

Device Support Level	Definition
Advance	The IP core is available for simulation and compilation for this device family. Timing models include initial engineering estimates of delays based on early post-layout information. The timing models are subject to change as silicon testing improves the correlation between the actual silicon and the timing models. You can use this IP core for system architecture and resource utilization studies, simulation, pinout, system latency assessments, basic timing assessments (pipeline budgeting), and I/O transfer strategy (data-path width, burst depth, I/O standards tradeoffs).
Preliminary	The IP core is verified with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. It can be used in production designs with caution.
Final	The IP core is verified with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.

Table 2. Intel Stratix 10 10GBASE-KR PHY IP Core Device Family Support

Device Family	Support Level
Intel Stratix 10	Advance

1.3. IP Core Speed Grade Support

Table 3. Slowest Supported Device Speed Grades

IP Core	Device Family	Supported Core Speed Grade
Intel Stratix 10 10GBASE-KR PHY IP	Intel Stratix 10	-2

1.4. Resource Utilization

The following numbers were obtained by compiling the PHY IP core for Intel Stratix 10 devices using the Intel Quartus® Prime Pro Edition 17.1. The numbers of ALMs and logic registers are rounded up to the nearest 100.

Table 4. Resource Utilization

IP variation	ALMs	Registers	M20K Blocks
Intel Stratix 10 10GBASE-KR PHY IP core (with Auto-negotiation and Link training)	2900	3600	8

1.5. Release Information

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP versioning scheme (X.Y.Z) number changes from one software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Table 5. Release Information

Item	Description
IP Version	19.1.1
Intel Quartus Prime Version	19.2
Release Date	2019.07.19
Ordering Code	IP-10GBASEKRPHY

2. Getting Started

The following section explains how to install, parameterize, simulate, and initialize the Intel Stratix 10 10GBASE-KR PHY IP core:

2.1. Installing and Licensing Intel FPGA IP Cores

The Intel Quartus Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license. Some Intel FPGA IP cores require purchase of a separate license for production use. The Intel FPGA IP Evaluation Mode allows you to evaluate these licensed Intel FPGA IP cores in simulation and hardware, before deciding to purchase a full production IP core license. You only need to purchase a full production license for licensed Intel IP cores after you complete hardware testing and are ready to use the IP in production.

The Intel Quartus Prime software installs IP cores in the following locations by default:

Figure 2. IP Core Installation Path

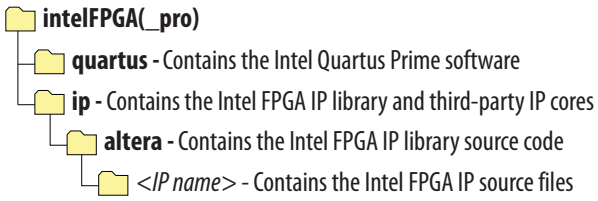


Table 6. IP Core Installation Locations

Location	Software	Platform
<drive>:\intelFPGA_pro\quartus\ip\altera	Intel Quartus Prime Pro Edition	Windows*
<home directory>:/intelFPGA_pro/quartus/ip/altera	Intel Quartus Prime Pro Edition	Linux*

2.1.1. Intel FPGA IP Evaluation Mode

The free Intel FPGA IP Evaluation Mode allows you to evaluate licensed Intel FPGA IP cores in simulation and hardware before purchase. Intel FPGA IP Evaluation Mode supports the following evaluations without additional license:

- Simulate the behavior of a licensed Intel FPGA IP core in your system.
- Verify the functionality, size, and speed of the IP core quickly and easily.
- Generate time-limited device programming files for designs that include IP cores.
- Program a device with your IP core and verify your design in hardware.

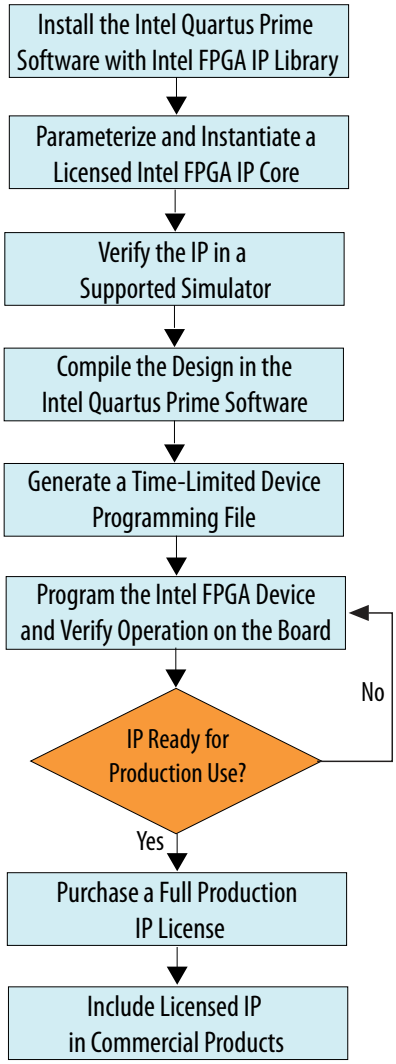
Intel FPGA IP Evaluation Mode supports the following operation modes:

- **Tethered**—Allows running the design containing the licensed Intel FPGA IP indefinitely with a connection between your board and the host computer. Tethered mode requires a serial joint test action group (JTAG) cable connected between the JTAG port on your board and the host computer, which is running the Intel Quartus Prime Programmer for the duration of the hardware evaluation period. The Programmer only requires a minimum installation of the Intel Quartus Prime software, and requires no Intel Quartus Prime license. The host computer controls the evaluation time by sending a periodic signal to the device via the JTAG port. If all licensed IP cores in the design support tethered mode, the evaluation time runs until any IP core evaluation expires. If all of the IP cores support unlimited evaluation time, the device does not time-out.
- **Untethered**—Allows running the design containing the licensed IP for a limited time. The IP core reverts to untethered mode if the device disconnects from the host computer running the Intel Quartus Prime software. The IP core also reverts to untethered mode if any other licensed IP core in the design does not support tethered mode.

When the evaluation time expires for any licensed Intel FPGA IP in the design, the design stops functioning. All IP cores that use the Intel FPGA IP Evaluation Mode time out simultaneously when any IP core in the design times out. When the evaluation time expires, you must reprogram the FPGA device before continuing hardware verification. To extend use of the IP core for production, purchase a full production license for the IP core.

You must purchase the license and generate a full production license key before you can generate an unrestricted device programming file. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (*<project name>*`_time_limited.sof`) that expires at the time limit.

Figure 3. Intel FPGA IP Evaluation Mode Flow



Note: Refer to each IP core's user guide for parameterization steps and implementation details.

Intel licenses IP cores on a per-seat, perpetual basis. The license fee includes first-year maintenance and support. You must renew the maintenance contract to receive updates, bug fixes, and technical support beyond the first year. You must purchase a full production license for Intel FPGA IP cores that require a production license, before generating programming files that you may use for an unlimited time. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (`<project name>_time_limited.sof`) that expires at the time limit. To obtain your production license keys, visit the Self-Service Licensing Center.

The Intel FPGA Software License Agreements govern the installation and use of licensed IP cores, the Intel Quartus Prime design software, and all unlicensed IP cores.

Related Information

- Intel Quartus Prime Licensing Site
- Introduction to Intel FPGA Software Installation and Licensing

2.2. Specifying the IP Core Parameters and Options

The Intel Stratix 10 10GBASE-KR PHY parameter editor allows you to quickly configure your custom IP variation. Perform the following steps to specify IP core options and parameters in the Intel Quartus Prime Pro Edition software:

1. In the Intel Quartus Prime Pro Edition, click **File ➤ New Project Wizard** to create a new Intel Quartus Prime project, or **File ➤ Open Project** to open an existing Intel Quartus Prime project. The wizard prompts you to specify a device.
2. In the IP Catalog (**Tools ➤ IP Catalog**), locate and double-click **Stratix 10 10GBASE-KR PHY**. The **New IP Variant** window appears.
3. Specify a top-level name for your custom IP variation. The parameter editor saves the IP variation settings in a file named *<your_ip>*`.ip`.
4. Click **Create**. The parameter editor appears.
5. On the **IP** tab, specify the parameters for your IP core variation. Refer to *Parameter Settings* for information about specific IP core parameters.
6. Optionally, to generate a simulation testbench or compilation and hardware design example, follow the instructions in the *Design Example* section.
7. Click **Generate HDL**. The **Generation** dialog box appears.
8. Specify output file generation options, and then click **Generate**. The IP variation files generate according to your specifications.
9. Click **Finish**. The parameter editor adds the top-level `.ip` file to the current project automatically. If you are prompted to manually add the `.ip` file to the project, click **Project ➤ Add/Remove Files in Project** to add the file.
10. After generating and instantiating your IP variation, make appropriate pin assignments to connect ports.

Related Information

- Parameter Settings on page 15
- Design Example on page 42

2.3. Generated File Structure

The Intel Quartus Prime Pro Edition software generates the following IP core output file structure.

For more information about the file structure of the design example, refer to the *Design Example* section.

Figure 4. IP Core Generated Files

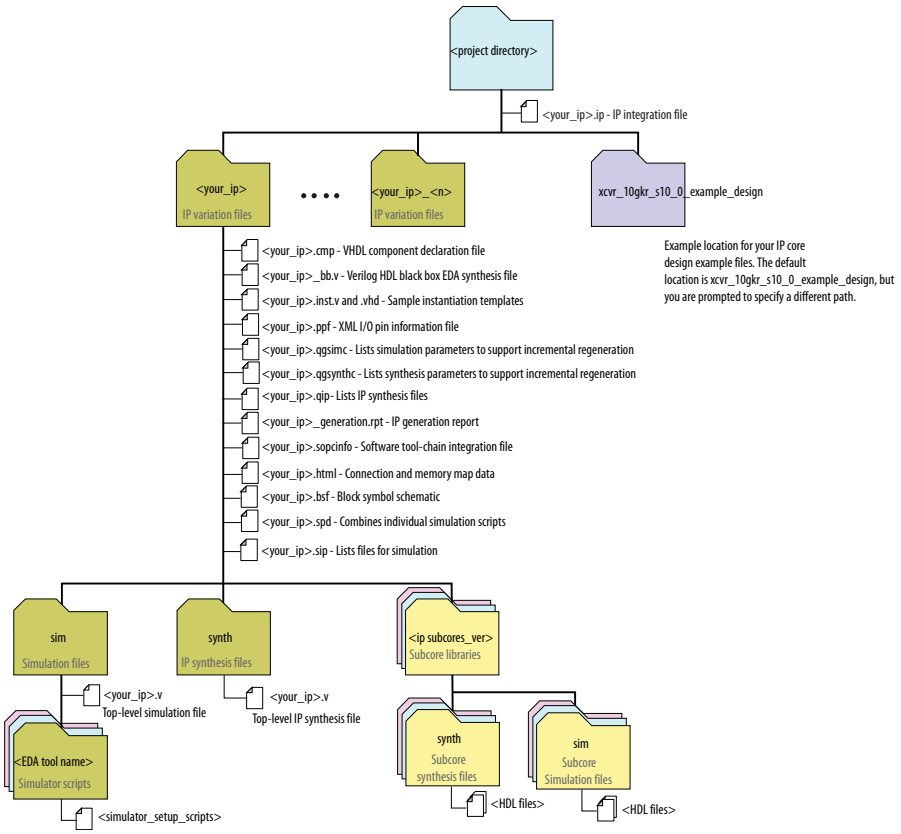


Table 7. IP Core Generated Files

File Name	Description
<*your_ip*>.ip	The The top-level IP variation file. <*your_ip*> is the name that you give your IP variation.
<*your_ip*>.cmp	The VHDL Component Declaration (**.cmp**) file is a text file that contains local generic and port definitions that you can use in VHDL design files. This IP core does not support VHDL. However, the Intel Quartus Prime Pro Edition software generates this file.
<*your_ip*>.html	A report that contains connection information, a memory map showing the address of each slave with respect to each master to which it is connected, and parameter assignments.
<*your_ip*>_generation.rpt	IP or Platform Designer generation log file. A summary of the messages during IP generation.
<*your_ip*>.qgsimc	Lists simulation parameters to support incremental regeneration.
<*your_ip*>.qgsynthc	Lists synthesis parameters to support incremental regeneration.
<*your_ip*>.qip	Contains all the required information about the IP component to integrate and compile the IP component in the Intel Quartus Prime software.
<*your_ip*>.sopcinfo	Describes the connections and IP component parameterizations in your Platform Designer system. You can parse its contents to get requirements when you develop software drivers for IP components.

continued...

File Name	Description
<*your_ip*>.csv	Contains information about the upgrade status of the IP component.
<*your_ip*>.bsf	A Block Symbol File (**.bsf**) representation of the IP variation for use in Intel Quartus Prime Block Diagram Files (**.bdf**).
<*your_ip*>.spd	Required input file for `ip-make-simscript` to generate simulation scripts for supported simulators. The **.spd** file contains a list of files generated for simulation, along with information about memories that you can initialize.
<*your_ip*>.ppf	The Pin Planner File (**.ppf**) stores the port and node assignments for IP components created for use with the Pin Planner.
<*your_ip*>_bb.v	You can use the Verilog black-box (**_bb.v**) file as an empty module declaration for use as a black box.
<*your_ip*>_inst.v or _inst.vhd	HDL example instantiation template. You can copy and paste the contents of this file into your HDL file to instantiate the IP variation. This IP core does not support VHDL. However, the Intel Quartus Prime Pro Edition software generates the `_inst.vhd` file.
<*your_ip*>.v	HDL files that instantiate each submodule or child IP core for synthesis or simulation.
mentor/	Contains a ModelSim* script `msim_setup.tcl` to set up and run a simulation.
aldec/	Contains a Riviera-PRO* script `rivierapro_setup.tcl` to setup and run a simulation.
synopsys/vcs/ synopsys/vcsmx/	Contains a shell script `vcs_setup.sh` to set up and run a VCS* simulation. Contains a shell script `vcsmx_setup.sh` and `synopsys_ sim.setup` file to set up and run a VCS MX* simulation.
cadence/	Contains a shell script `ncsim_setup.sh` and other setup files to set up and run an NCSim* simulation.
submodules/	Contains HDL files for the IP core submodules.
<*child IP cores*>/	For each generated child IP core directory, Platform Designer generates `synth/` and `sim/` sub-directories.

Related Information

Design Example Directory Structure on page 42
Information about the Stratix 10 10GBASE-KR PHY IP design example file structure.

2.4. Simulating the IP Core

You can simulate your Intel Stratix 10 10GBASE-KR IP core variation with the functional simulation model and the testbench generated with the design example provided with this IP core. The functional simulation model is a cycle-accurate model that allows for fast functional simulation of your IP core instance using industry-standard Verilog or VHDL simulators. For more information, refer to *Design Example* section.

The functional simulation model and testbench files are generated in project subdirectories. These directories also include scripts to compile and run the design example.

2.5. Integrating Your IP Core in Your Design

2.5.1. Pin Assignments

When you integrate your Intel Stratix 10 10GBASE-KR PHY IP core instance in your design, you must make appropriate pin assignments. While compiling the IP core alone, you can create virtual pins to avoid making specific pin assignments for top-level signals. When you are ready to map the design to hardware, you can change to the correct pin assignments.

Related Information

Quartus Prime Pro Edition Help version 19.2
For information about the Quartus Prime software, including virtual pins.

2.5.2. Adding the Transceiver PLL

Intel Stratix 10 10GBASE-KR PHY IP core requires an external PLL to drive the TX transceiver serial clock, in order to compile and to function correctly in hardware. In many cases, the same PLL can be shared with other transceivers in your design.

The TX transceiver PLL is instantiated with an Intel FPGA ATX PLL IP core. The TX transceiver PLL must always be instantiated outside the Intel Stratix 10 10GBASE-KR PHY IP core.

You can use the IP Catalog to create a transceiver PLL.

- Select **Stratix 10 L-Tile/H-Tile Transceiver ATX PLL**.
- In the parameter editor, set the following parameter values:
  - **PLL output frequency** to **5156.25 MHz**
  - **PLL auto mode reference clock frequency (integer)** to **644.53125 MHz** or **322.265625 MHz**

You must connect the `tx_serial_clk` input pin of the Intel Stratix 10 10GBASE-KR IP core PHY link to the output port of the ATX PLL.

2.5.3. Adding the fPLL

Intel Stratix 10 cores require an external fPLL to drive the `xgmii_tx_clk` and `xgmii_rx_clk` clock signals. You can use single fPLL across multiple instances of 10GBASE-KR PHY IP core.

2.5.4. Adding the Intel Stratix 10 Transceiver PHY Reset Controller

You must add an Intel Stratix 10 Transceiver PHY Reset Controller IP core to your design, and connect it to the Intel Stratix 10 10GBASE-KR PHY IP core reset signals. This block implements a reset sequence that resets the device transceiver correctly.

You can use the IP Catalog to create a transceiver PHY reset controller. In the Intel Stratix 10 Transceiver PHY Reset Controller IP parameter editor, you must perform the following for compatibility with the 10GBASE-KR PHY IP core:

- Select the **RX digital reset mode** to **Manual** if auto-negotiation mode is enabled.

2.5.5. Placement Settings for the Intel Stratix 10 10GBASE-KR PHY IP Core

The Intel Quartus Prime Pro Edition software provides the options to specify design partitions or Logic Lock regions for incremental compilation, to control placement on the device. To achieve timing closure for your design, you might need to provide floorplan guidelines using one or both of these features.

The appropriate floorplan is always design-specific, and depends on your full design.

Related Information

Intel Quartus Prime Pro Edition User Guide: Design Optimization
Describes incremental compilation, design partitions, and LogicLock Plus regions.

2.6. Intel Stratix 10 10GBASE-KR IP Core Testbench

Intel provides a compilation-only example design and a testbench with most variations of the Intel Stratix 10 10GBASE-KR PHY IP core.

2.7. Compiling the Full design

You can use the **Start Compilation** command on the Processing menu in the Intel Quartus Prime software to compile your design. After successfully compiling your design, program the targeted Intel FPGA with the Programmer and verify the design in hardware.

Note: The Intel Stratix 10 10GBASE-KR PHY IP core design example synthesis directories include Synopsys Design Constraint (`.sdc`) files that you can copy and modify for your own design.

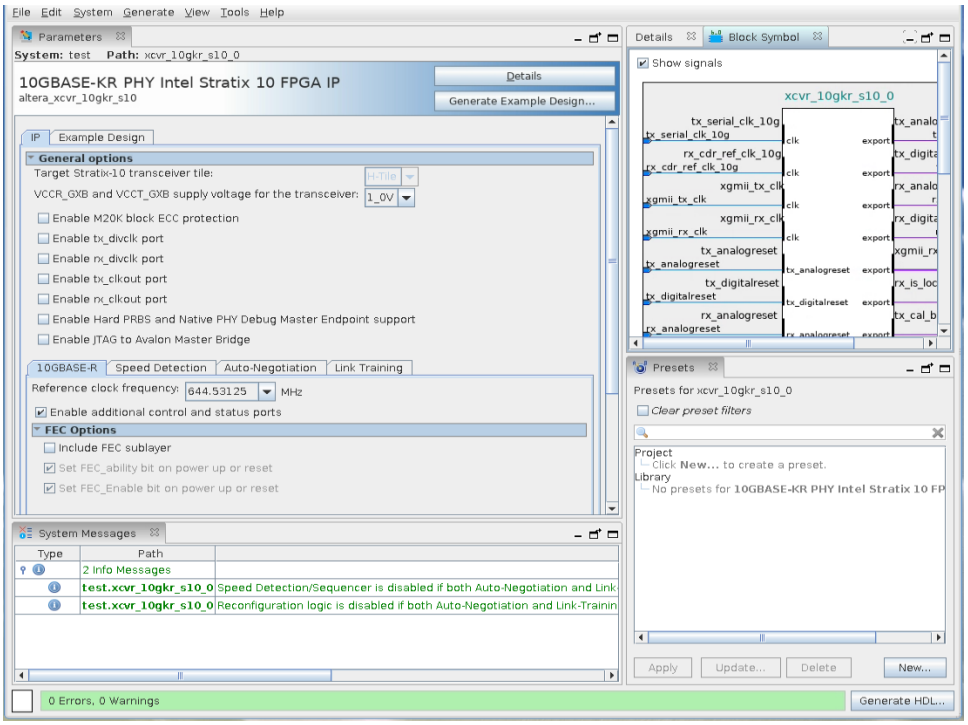
Related Information

- Design Compilation
- Programming Intel FPGA Devices

3. Parameter Settings

The Intel Stratix 10 10GBASE-KR parameter editor provides the parameters you can set to configure the Intel Stratix 10 10GBASE-KR PHY IP core and simulation and hardware design example. You can select the Intel Stratix 10 10GBASE-KR PHY IP core from the Intel Quartus Prime Pro Edition IP catalog. To customize the PHY IP core, specify the parameters in the IP parameter editor.

Figure 5. IP Parameter Editor



The Intel Stratix 10 10GBASE-KR PHY parameter editor has an **IP** tab and an **Example Design** tab. For information about the **Example Design**, refer to the *Design Example* section.

Table 8. Intel Stratix 10 10GBASE-KR PHY IP Core Parameters: IP Tab

Parameter	Options	Description
General Options		
Target Stratix-10 transceiver tile	L-Tile, H-Tile	Specifies the transceiver tile on your target Intel Stratix 10 device. The **Device** setting of the Intel Quartus

continued...

Parameter	Options	Description
		Prime Pro Edition project in which you generate the IP core determines the transceiver tile type. In the current version of theIntel Quartus Prime Pro Edition, this parameter is grayed out. The correct tile is derived when you select a device for the project. The IP generates the correct transceiver tile type for your target Intel Stratix 10 device.
VCCR_GXB and VCCT_GXB supply voltage for the transceiver	1_0V, 1_1V	Selects the VCCR_GXB and VCCT_GXB supply voltage for the transceiver. For 10 Gbps data rate, you can select this value either to 1 V or 1.1 V.
Enable M20K block ECC protection	On/Off	When you turn on this parameter, you enable error correction code (ECC) support on the embedded Nios® II CPU system.
Enable tx_divclk port	On/Off	When you turn on this parameter, the `tx_pma_div_clkout` port is enabled. Refer to the Clock and Reset Interfaces section for more information about this port.
Enable rx_divclk port	On/Off	When you turn on this parameter, the `rx_pma_div_clkout` port is enabled. Refer to the *Clock and Reset Signals* section for more information about this port.
Enable tx_clkout port	On/Off	When you turn on this parameter, the `tx_clkout` port is enabled. Refer to the *Clock and Reset Signals* section for more information about this port.
Enable rx_clkout port	On/Off	When you turn on this parameter, the `rx_clkout` port is enabled. Refer to the *Clock and Reset Signals* section for more information about this port.
Enable Hard PRBS support and Native PHY Debug Master Endpoint support	On/Off	When you turn on this parameter, you enable the Native PHY Debug Master Endpoint (NPDME) and Hard PRBS data generation and checking logic in the Native PHY. The transceiver toolkit (TTK) requires NPDME to be enabled in the Native PHY IP core.
Enable JTAG to Avalon Master Bridge	On/Off	If turned on, the IP core includes a JTAG to Avalon-MM Master bridge connecting internally to status and reconfiguration registers. This allows to run the Ethernet Link Inspector using the System Console
Tab: **10GBASE-R**		
Reference clock frequency	644.53125 MHz 322.265625 MHz	Specifies the input reference clock frequency.
Enable additional control and status ports	On/Off	When you turn on this parameter, the core includes the `rx_block_lock` and `rx_hi_ber` output.

continued...

Parameter	Options	Description
FEC Options		
Include FEC sublayer	On/Off	When you turn on this parameter, the core includes logic to support hard *Clause 74* FEC.
Set FEC_ability bit on power up and reset	On/Off	When you turn on this parameter, the core sets the `Assert KR FEC Ability` bit (0xB0[16]) FEC ability bit during power up and reset, causing the core to assert the FEC ability. This option is required for FEC functionality. This parameter is available if you turn on **Include FEC sublayer**.
Set FEC_Enable bit on power up and reset	On/Off	When you turn on this parameter, the IP core sets the `KR FEC Request` bit (`0xB0[18]`) during power up and reset, causing the core to request the FEC ability during auto-negotiation. This option is required for FEC functionality. This parameter is available if you turn on **Include FEC sublayer**.
Tab: **Speed Detection**		
Avalon-MM clock frequency	156.25 MHz	Specifies the clock frequency for `mgmt_clk`. The legal range is 100 MHz to 161 MHz (inclusive). This parameter is available if you turn on either **Enable Auto-Negotiation** or **Enable Link Training**
Link fail inhibit time for 10Gb Ethernet	504 ms	Specifies the time before `link_status` is set to FAIL or OK. A link fails if the `link_fail_inhibit_time` has expired before `link_status` is set to OK. The Ethernet standard range is 500 ms to 510 ms and IP core legal range is 10 ms to 1270 ms. For more information, refer to *Clause 73 Auto Negotiation for Backplane Ethernet in IEEE Std 802.3-2015*. This parameter is available if you turn on either **Enable Auto-Negotiation** or **Enable Link Training**
Enable PCS-Mode port	On/Off	Enables or disables the PCS-Mode port.
Tab: **Auto-Negotiation**		
Enable Auto-Negotiation	On/Off	When you turn on this parameter, the IP core includes logic to implement auto-negotiation feature.
Pause ability-C0	On/Off	When you turn on this parameter, the IP core indicates on the Ethernet link that it supports symmetric pauses. For more information, refer to *IEEE 802.3 Annex 28B*. This parameter is available if you turn on **Enable Auto-Negotiation**.

continued...

Parameter	Options	Description
Pause ability-C1	On/Off	When you turn on this parameter, the IP core indicates on the Ethernet link that it supports asymmetric pauses. For more information, refer to *IEEE 802.3 Annex 28B*. This parameter is available if you turn on **Enable Auto-Negotiation**.
Tab: **Link Training**		
Enable Link Training	On/Off	Enables or disables the Link Training feature.
Maximum bit error count	15, 31, 63, 127, 255, 511, 1023	Specifies the number of bit errors for the error counter expected during each step of the link training. The number of errors depends upon the amount of time for each step and the quality of the physical link media. The default value is 511. This parameter is available if you turn on **Enable Link Training**.
Number of frames to send before sending actual data	127, 255	Specifies the number of additional training frames the local link partner delivers to ensure that the link partner can correctly detect the local receiver state. This number is the value of `wait_timer`. The default value is 127. This parameter is available if you turn on **Enable Link Training**.
PMA parameters (only available when you turn on **Enable Link Training**)		
VMAXRULE	0-31	Specifies the maximum V_{OD}. The default value is 30.
VMINRULE	0-31	Specifies the minimum V_{OD}. The default value is 6.
VODMINRULE	0-31	Specifies the minimum V_{OD} for the first tap. The default value is 14.
VPOSTRULE	0-38	Specifies the maximum value that the internal algorithm for pre-emphasis will ever test in determining the optimum post-tap setting. The default value is 25.
VPRERULE	0-31	Specifies the maximum value that the internal algorithm for pre-emphasis will ever test in determining the optimum pre-tap setting. The default value is 16.
PREMAINVAL	0-31	Specifies the Preset V_{OD} value. This value is set by the Preset command of the link training protocol, defined in Clause 72.6.10.2.3.1 of the Link Training protocol. This is the value from which the algorithm starts. The default value is 30.
PREPOSTVAL	0-31	Specifies the preset Post-tap value. The default value is 0.

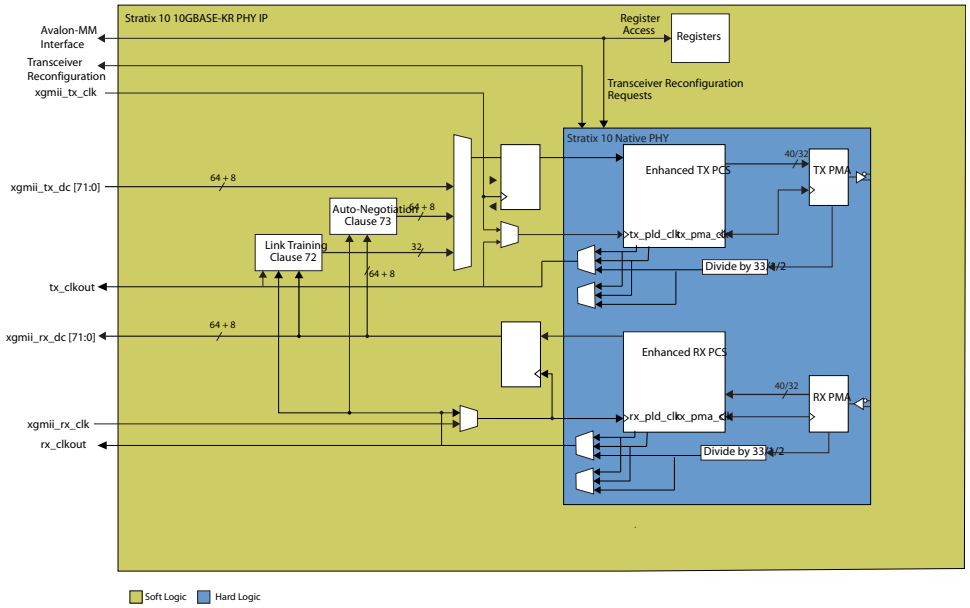
continued...

Parameter	Options	Description
PREPREVAL	0-15	Specifies the preset Pre-tap value. The default value is 0.
INITMAINVAL	0-31	Specifies the initial V_{OD} value. This value is set by the Initialize command of the link training protocol. The default value is 25.
INITPOSTVAL	0-38	Specifies the initial Post-tap value. The default value is 13.
INITPREVAL	0-15	Specifies the initial Pre-tap value. The default value is 3.

4. Functional Description

The Intel FPGA 10GBASE-KR PHY IP core implements an Ethernet MAC in accordance with the *802.3 2015 Standard*. The IP core implements an Ethernet PCS and PMA (PHY) that handles the frame encapsulation and flow of data between a client logic and Ethernet network. The following figure shows the supporting components inside the Intel Stratix 10 10GBASE-KR PHY IP core.

Figure 6. Intel Stratix 10 10GBASE-KR PHY IP Core Block Diagram



The Intel Stratix 10 10GBASE-KR PHY IP core includes the following components:

Enhanced PCS Datapaths

The Enhanced PCS and PMA inside the Native PHY are configured as a 10GBASE-R PHY. Refer to the *PCS architecture chapters of Intel Stratix 10 Transceiver PHY User Guide* for more details on how these blocks support 10G protocols and FEC.

Auto Negotiation, IEEE 802.3 Clause 73

The auto-negotiation component synchronizes the start time of the link training on both sides of the link. This function ensures that the link training can complete in 500 ms or less, as required by the IEEE specification.

Link Training (LT), IEEE 802.3 Clause 72

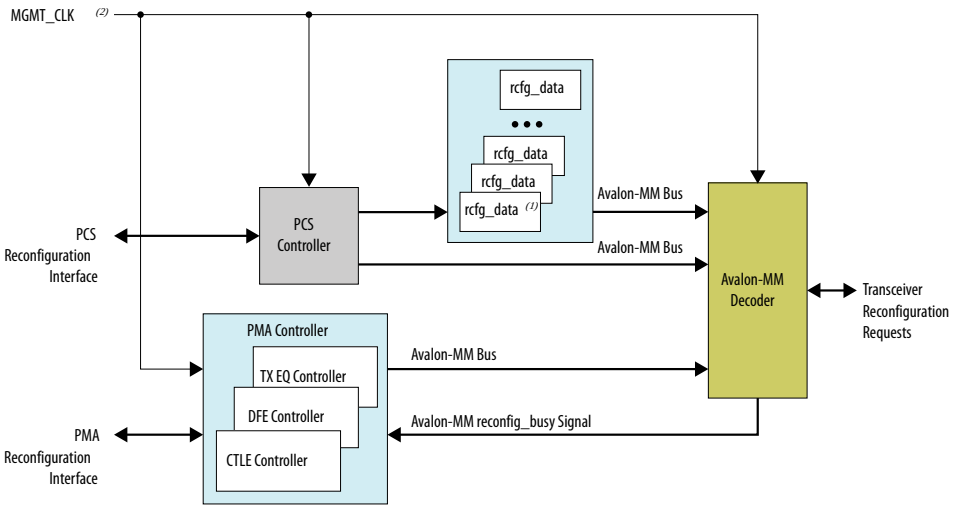
Intel Stratix 10 devices have soft link training IP that complies with the IEEE 802.3 Clause 72 standard training procedure. This IP includes:

- Training frame lock that is different from the regular 64b/66b frame_lock
- Training frame generation
- The control channel codec
- Local Device (LD) coefficient update
- Link Partner (LP) coefficient generation

Reconfiguration Block

The Reconfiguration Block performs Avalon® Memory-Mapped Interface (Avalon-MM) writes to the PHY for both PCS and PMA reconfiguration. The Avalon-MM master accepts requests from the PMA or PCS controller. It performs Read-Modify-Write or Write commands on the Avalon-MM interface. The PCS controller receives rate change requests from the Sequencer and translates them to a series of Read-Modify-Write or Write commands to the PMA and PCS.

Figure 7. Reconfiguration Block



Notes:
1. rcfg = Reconfiguration
2. MGMT_CLK = Management Clock

Related Information

Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide

5. Intel Stratix 10 10GBASE-KR PHY Registers

5.1. Register Map

Table 9. Intel Stratix 10 10GBASE-KR PHY Register Map

Word Offset	Register Type
0x4B0-0x4BF	General 10GBASE-KR registers
0x4C0-0x4CF	Auto-negotiation registers (only available when you turn on **Enable Auto-Negotiation** parameter)
0x4D0-0x4EF	Link training registers (only available when you turn on **Enable Link Training** parameter)

5.2. Register Definitions

You can access the Intel Stratix 10 10GBASE-KR PHY registers on the Avalon-MM PHY management interface. To modify a field value in any of the following registers, you must perform a read-modify-write operation to ensure you do not modify the values of any other fields in the register.

Table 10. Intel Stratix 10 10GBASE-KR PHY Registers

Register fields not listed are reserved.

Word Addr	Bit	R/W	Register Name	Description
0x4B0	0	RW	`Reset SEQ`	When set to 1, resets the 10GBASE-KR sequencer (auto rate detect logic), initiates a PCS reconfiguration, and may restart auto-negotiation, link training or both if AN and LT are enabled. `SEQ Force Mode [3:0]` forces these modes. This bit is self-clearing.
	1	RW	`Disable AN Timer`	Auto-negotiation disable timer. If disabled (`Disable AN Timer = 1`) , AN may get stuck and require software support to remove the ABILITY_DETECT capability if the link partner does not include this feature. In addition, software may have to take the link out of loopback mode if the link is stuck in the ACKNOWLEDGE_DETECT state. To enable this timer set `Disable AN Timer = 0`.
	2	RW	`Disable LF Timer`	When set to 1, disables the Link Fail Inhibit timer. When set to 0, the Link Fault timer is enabled.
	3	RW	`fail_lt_if_ber`	When set to 1, the most recent LT measurement is a non-zero number. Treat this as a failed run.

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Word Addr	Bit	R/W	Register Name	Description
	7:4	RW	SEQ Force Mode[3:0]	Forces the sequencer to a specific protocol. You must write the Reset SEQ bit to 1 for the Force to take effect. The following encodings are defined: • 0000: No force • 0001: Reserved • 0010: Reserved • 0100: 10GBASE-R • 0101: 10GBASE-KR • 1100: 10GBASE-KR FEC
	8	Reserved		
	12	RW	LT Failure Response	When set to 1, LT failure causes the PHY to go into data mode. When set to 0, LT failure restarts auto-negotiation (if enabled). If auto-negotiation is not enabled, then the PHY restarts LT. The default value is 1.
	16	RW	Assert KR FEC ability 171.0	When set to 1, FEC is enabled. When set to 0, FEC is disabled. Resets to the CAPABLE_FEC parameter value.
	17	RW	KR FEC enable err ind 171.1	When set to 1, KR PHY FEC decoding errors are signaled to the PCS. When set to 0, FEC errors are not signaled to the PCS. See *Clause 74.8.3 of IEEE 802.3.2015* for details.
	18	RW	Assert KR FEC request	When set to 1, enables the FEC request. When this bit changes, you must assert the Reset SEQ bit (0x4B0 [0]) to renegotiate with the new value. When set to 0, disables the FEC request.
0x4B1	0	RO	SEQ Link Ready	When asserted, the sequencer is indicating that the link is ready.
	1	RO	SEQ AN timeout	When asserted, the sequencer has had an auto-negotiation timeout. This bit is latched and is reset when the sequencer restarts auto-negotiation.
	2	RO	SEQ LT timeout	When set, indicates that the Sequencer has had a Link Training timeout.
	13:8	RO	SEQ Reconfig Mode[5:0]	Specifies the Sequencer mode for PCS reconfiguration. The following modes are defined: • Bit 8, mode[0]: AN mode • Bit 9, mode[1]: LT Mode • Bit 10, mode[2]: 10G data mode • Bit 11, mode[3]: Reserved • Bit 12, mode[4]: Reserved • Bit 13, mode[5]: 10G FEC mode
	16	RO	KR FEC ability 170.0	When set to 1, indicates that the 10GBASE-KR PHY supports FEC. Set as parameter SYNTH_FEC. For more information, refer to *Clause 45.2.1.84 of IEEE 802.3-2015*.
	17	RO	KR FEC err ind ability 170.0	When set to 1, indicates that the 10GBASE-KR PHY is capable of reporting FEC decoding errors to the PCS. For more information, refer to *Clause 74.8.3 of IEEE 802.3-2015*.
0x4B2	11	RW	KR FEC TX Error Insert	Writing a 1 inserts one error pulse into the TX FEC depending on the Transcoder and Burst error settings. This bit self clears.

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Word Addr	Bit	R/W	Register Name	Description
0x4C0	0	RW	AN enable	When set to 1, enables auto-negotiation function. The default value is 1. For additional information, refer to *7.0.12 in Clause 73.8 Management Register Requirements, of IEEE 802.3-2015*.
	1	RW	AN base pages ctrl	When set to 1, the user base pages are enabled. You can send arbitrary data via the user base page low/high bits. When set to 0, the user base pages are disabled and the state machine generates the base pages to send.
	2	RW	AN next pages ctrl	When set to 1, the user next pages are enabled. You can send any arbitrary data via the user next page low/high bits. When set to 0, the user next pages are disabled. The state machine generates the null message to send as next pages.
	3	RW	Local device remote fault	When set to 1, the local device signals Remote Faults in the auto-negotiation pages. When set to 0, a fault has not occurred.
	4	RW	Force TX nonce value	When set to 1, forces the TX nonce value to support some UNH testing modes. When set to 0, this is normal operation.
	5	RW	Override AN Parameters Enable	When set to 1, overrides the AN_TECH, AN_FEC, and AN_PAUSE parameters and uses the bits in 0x4C3 instead. You must reset the Sequencer to reconfigure and restart into auto negotiation mode. When set to 0, this is normal operation and is used with 0x4B0 bit 0 and 0x4C3 bits[30:16].
	7	RW	Ignore nonce field	When set to 1, tells the IP core to ignore the TX nonce field. This mode supports auto-negotiation when the IP core is in loopback mode.
0x4C1	0	RW	Reset AN	When set to 1, resets all the 10GBASE-KR auto negotiation state machines. This bit is self-clearing.
	4	RW	Restart AN TX SM	When set to 1, restarts the 10GBASE-KR TX state machine. This bit is self-clearing. This bit is active only when the TX state machine is in the auto-negotiation state. For more information, refer to *7.0.9 in Clause 73.8 Management Register Requirements of IEEE 802.3-2015*.
	8	RW	AN Next Page	When asserted, new next page info is ready to send. The data is in the XNP TX registers. When 0, the TX interface sends null pages. This bit self clears. Next Page (NP) is encoded in bit D15 of Link Codeword. For more information, refer to *Clause 73.6.9 and 7.16.15 of Clause 45.2.7.6 of IEEE 802.3-2015*.
0x4C2	1	RO	AN page received	When set to 1, a page has been received. When 0, a page has not been received. The current value clears when the register is read. For more information, refer to *7.1.6 in Clause 73.8 of IEEE 802.3-2015*.
	2	RO	AN Complete	When asserted, auto-negotiation has completed. When 0, auto-negotiation is in progress. For more information, refer to *7.1.5 in Clause 73.8 of IEEE 802.3-2015*.
	3	RO	AN ADV Remote Fault	When set to 1, fault information has been sent to the link partner. When 0, a fault has not occurred. The current value clears when the register is read. Remote Fault (RF) is encoded in bit D13 of the base Link Codeword. For more information, refer to *Clause 73.6.7 of and 7.16.13 of IEEE 802.3-2015*.
	4	RO	AN RX SM Idle	When set to 1, the auto-negotiation state machine is in the idle state. Incoming data is not Clause 73 compatible. When 0, the auto-negotiation is in progress.

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Word Addr	Bit	R/W	Register Name	Description
	5	RO	AN Ability	When set to 1, the transceiver PHY is able to perform auto-negotiation. When set to 0, the transceiver PHY is not able to perform auto-negotiation. If you selected **Enable Auto-Negotiation** in the IP Parameter Editor, your variant includes auto negotiation, and this bit is tied to 1. For more information, refer to *7.1.3 and 7.48.0 of Clause 45 of IEEE 802.3-2015*.
	6	RO	AN Status	When set to 1, link is up. When 0, the link is down. The current value clears when the register is read. For more information, refer to *7.1.2 of Clause 45 of IEEE 802.3-2015*.
	7	RO	LP AN Ability	When set to 1, the link partner is able to perform auto negotiation. When 0, the link partner is not able to perform auto-negotiation. For more information, refer to *7.1.0 of Clause 45 of IEEE 802.3-2015*.
	8	RO	FEC negotiated – enable FEC from SEQ	When set to 1, PHY is negotiated to perform FEC. When set to 0, PHY is not negotiated to perform FEC.
	9	RO	SEQ AN Failure	When set to 1, a sequencer auto-negotiation failure has been detected. When set to 0, an auto-negotiation failure has not been detected.
	17:12	RO	KR AN Link Ready[5:0]	Provides a one-hot encoding of an_receive_idle = true and link status for the supported link as described in Clause 73.10.1. The following encodings are defined: • 6'b000001: 1000BASE-KX • 6'b000010: 10GBASE-KX4 • 6'b000100: 10GBASE-KR • 6'b001000: 40GBASE-KR4 • 6'b010000: 40GBASE-CR4 • 6'b100000: 100GBASE-CR10
0x4C3	15:0	RW	User base page low	When 0x4C0 bit [1] = 1 (AN base pages ctrl), sets the lower bits of the auto-negotation Base Page. The following bits are defined: • [15]: Next page bit (NP). • [14]: ACK bit (ACK). It is set automatically by the IP core. • [13]: Remote Fault (RF). • [12]: Reserved (C2). • [11]: PAUSE ASM_DIR (C1). Device can provide asymmetric PAUSE. • [10]: PAUSE Ability (C0). Device can provide symmetric PAUSE. • [9:5]: Echoed nonce field (E[4:0]). It is set automatically by the IP core. • [4:0]: Selector. This is normally set to 5'b10000 to indicate IEEE802.3 For more information, refer to *Clause 73.6 Link Codeword Encoding of IEEE 802.3-2015*.
	21:16	RW	Override AN_TECH[5:0]	AN_TECH value with which to override the current value. The following bits are defined: • [16]: Technology = 1000BASE-KX (A0) • [17]: Technology = 10GBASE-KX4 (A1) • [18]: Technology = 10GBASE-KR (A2) • [19]: Technology = 40GBASE-KR4 (A3) • [20]: Technology = 40GBASE-CR4 (A4) • [21]: Technology = 100GBASE-CR10 (A5)

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Word Addr	Bit	R/W	Register Name	Description
				You must set 0x4C0 bit-5 (`Override AN Parameters Enable`) for this to take effect .
	25:24	RW	`Override AN_FEC[1:0]`	AN_FEC value with which to override the current value. The following bits are defined: • [24]: FEC Ability (F0) • [25]: FEC Requested (F1) You must set 0x4C0 bit-5 (`Override AN Parameters Enable`) for this to take effect.
	30:28	RW	`Override AN_PAUSE[2:0]`	AN_PAUSE value with which to override the current value. The following bits are defined: • [28]: Pause Ability (C0) • [29]: Pause Asymmetric Direction (C1) • [30] Reserved (C2) You must set 0x4C0 bit-5 (`Override AN Parameters Enable`) for this to take effect.
0x4C4	31:0	RW	`User base page high`	When 0x4C0 bit [1] = 1 (`AN base pages ctrl`), sets the lower bits of the auto-negotation Base Page. The following bits are defined: • [4:0]: TX Nonce field (T[4:0]) • [5]: Technology = 1000BASE-KX (A0) • [6]: Technology = 10GBASE-KX4 (A1) • [7]: Technology = 10GBASE-KR (A2) • [8]: Technology = 40GBASE-KR4 (A3) • [9]: Technology = 40GBASE-CR4 (A4) • [10]: Technology = 100GBASE-CR10 (A5) • [11]: Technology = 100GBASE-KP4 (A6) • [12]: Technology = 100GBASE-KR4 (A7) • [13]: Technology = 100GBASE-CR4 (A8) • [31:14]: Reserved for future technology. For more information, refer to *Clause 73.6 Link Codeword Encoding of IEEE 802.3-2015*.
0x4C5	15:0	RW	`User Next page low`	When 0x4C0 bit-2 = 1 (`AN next pages ctrl`), sets the lower bits of the auto-negotation Next Page. The following bits are defined: • [15]: Next page bit (NP) • [14]: Next page ACK (ACK). This is bit is written by the IP core. • [13]: Message Page (MP). • [12]: ACK2 bit (ACK2). • [11]: Toggle bit (T). • [10:0]: Message code field/Unformatted Code Field (M/U[10:0]). The use of these bits depends on the MP bit setting. For more information, refer to *Clause 73.7.7.1 Next page encodings of IEEE 802.3-2015*.
0x4C6	31:0	RW	`User Next page high`	When 0x4C0 bit-2 = 1 (`AN next pages ctrl`), sets the upper bits of the auto-negotation next page. The following bits are defined: • [31:0]: Unformatted Code Field (U[31:0]/U[42:11]). The bits included depend on the MP bit from the lower bits of the Next Page. For more information, refer to *Clause 73.7.7.1 Next page encodings of IEEE 802.3-2015*.

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Word Addr	Bit	R/W	Register Name	Description
0x4C7	15:0	RO	LP base page low	The AN RX state machine receives these bits from the link partner. The following bits are defined: • [15]: Next page bit (NP). • [14]: ACK bit (ACK). • [13]: Remote Fault (RF). • [12]: Reserved (C2). • [11]: PAUSE ASM_DIR (C1). Device can provide asymmetric PAUSE. • [10]: PAUSE Ability (C0). Device can provide symmetric PAUSE. • [9:5]: Echoed nonce field (E[4:0]). • [4:0]: Selector.
0x4C8	31:0	RO	LP base page high	The AN RX state machine receives these bits from the link partner. The following bits are defined: • [31:30]: Reserved • [29:5]: Correspond to page bits [45:21] of the Link codeword Base Page from the link partner which are the technology ability • [4:0]: Correspond to bits [20:16] of the Link codeword Base Page from the link partner which are TX Nonce bits
0x4C9	15:0	RO	LP Next page low	The AN RX state machine receives these bits from the link partner. The following bits are defined: • [15]: Next page bit (NP) • [14]: Next page ACK (ACK). • [13]: Message Page (MP). • [12]: ACK2 bit (ACK2). • [11]: Toggle bit (T). • [10:0]: Message code field/Unformatted Code Field (M/U[10:0]). For more information, refer to *Clause 73.7.7.1 Next Page encodings of IEEE 802.3-2015*.
0x4CA	31:0	RO	LP Next page high	The AN RX state machine receives these bits from the link partner. Bits [31:0] correspond to page bits [47:16] of the Next Page from the link partner.
0x4CB	24:0	RO	AN LP ADV Tech_A[24:0]	Received technology ability field bits of Clause 73 auto negotiation. The 10GBASE-KR PHY supports bit [0] and bit [2]. The following protocols are defined: • [0]: 1000BASE-KX • [1]: 10GBASE-KX4 • [2]: 10GBASE-KR • [3]: 40GBASE-KR4 • [4]: 40GBASE-CR4 • [5]: 100GBASE-CR10 • Bit 24:6 are reserved For more information, refer to *Clause 73.6.4 and AN LP base page ability registers (7.19-7.21) of Clause 45 of IEEE 802.3-2015*.
	26:25	RO	AN LP ADV FEC_F[1:0]	Received FEC ability bits FEC (F0:F1) is encoded in bits D46:D47 of the Link codeword Base Page from the link partner. • [1]: FEC Requested (F1) • [0]: FEC Ability (F0) See Clause 73.6.5 of *IEEE 802.3-2015* for details.

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Word Addr	Bit	R/W	Register Name	Description
	27	RO	AN LP ADV Remote Fault	Received Remote Fault (RF) ability bits. RF is encoded in bit D13 of the Link codeword Base Page from the link partner. For more information, refer to Clause 73.6.7 of *IEEE 802.3-2015*.
	30:28	RO	AN LP ADV Pause Ability_C[2:0]	Received pause ability bits. Pause (C0:C1) is encoded in bits D11:D10 of the base link codeword in Clause 73 AN as follows: • [0]: PAUSE Ability (C0) • [1]: ASM_DIR (C1) • [2]: Reserved (C2)
0x4D0	0	RW	Link Training enable	When set to 1, enables the 10GBASE-KR start-up protocol. When 0, disables the 10GBASE-KR start-up protocol. The default value is 1. This register is only available when you turn on **Enable Link Training** parameter. Otherwise, it returns 0 for IP variants without link training. For more information, refer to *Clause 72.6.10.3.1 and 10GBASE-KR PMD control register bit (1.150.1) of IEEE 802.3-2015*.
	1	RW	dis_max_wait_tmr	When set to 1, disables the LT max_wait_timer. Used for characterization mode when setting much longer BER timer values. The default value is 0.
	2	RW	Enable TX EQ tuning	Enables TX equalization tuning during Link Training. When set to 1, sends request for Tx Pre/Post tap adjustment during Link Training for optimizing link. When set to 0, IP sends no request for Tx Pre/Post tap adjustment to link partner.
	3	RW	VOD Training enable	When set to 1, enables Vod (main) tap adjustment during Link Training. When set to 0, disables Vod (main) tap adjustment during Link Training. The default value is 1 for synth and 0 for sim.
	7:4	RW	main_step_cnt [3:0]	Specifies the number of equalization steps for each main tap update. There are about 20 settings for the internal algorithm to test. The valid range is 1-15. The default value is 4'b0001.
	11:8	RW	prepost_step_cnt [3:0]	Specifies the number of equalization steps for each pre- and post-tap update. From 16-31 steps are possible. The default value is 4'b0001.
	14:12	RW	equal_cnt [2:0]	Adds hysteresis to the error count to avoid local minimums. The following values are defined: • 3'b000 = 0 • 3'b001 = 2 • 3'b010 = 4 • 3'b011 = 8 • 3'b100 = 16 • 3'b101 = 32 • 3'b110 = 64 • 3'b111 = 128 The default value is 3'b101.
	15	RW	disable Initialize PMA on max_wait_timeout	When set to 1, PMA values (VOD, Pre-tap, Post-tap) are not initialized upon entry into the Training_Failure state. This happens when max_wait_timer_done, which sets training_failure = true (register 0x4D2 bit 3). Used for

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Word Addr	Bit	R/W	Register Name	Description
				UNH testing. When set to 0, PMA values are initialized upon entry into `Training_Failure` state. Refer to Figure 72-5 of *IEEE 802.3-2015* for more details. The default value is 0.
	16	RW	`Ovride LP Coef enable`	When set to 1, overrides the link partner's equalization coefficients; software changes the update commands sent to the link partner TX equalizer coefficients. When set to 0, uses the link training logic to determine the link partner coefficients. Used with 0x4D1 bit-4 and 0x4D4 bits[7:0]. The default value is 0.
	17	RW	`Ovride Local RX Coef enable`	When set to 1, overrides the local device equalization coefficients generation protocol. When set, the software changes the local TX equalizer coefficients. When set to 0, uses the update command received from the link partner to determine local device coefficients. Used with 0x4D1 bit-8 and 0x4D4 bits[23:16]. The default value is 0.
	18	Reserved		
	19	RW	`Auto/Manual RX Adaptation`	When set to 1, RX adaptation is in manual mode. IP uses bits[31:22] to set CTLE/VGA values during Link Training. When set to 0, RX adaptation is in auto-adaptation mode. IP ignores bits[31:22] in this mode. The default value is 0 for synth and 1 for sim.
	22:20	RW	`Manual CTLE-AC`	Sets by IP during Link Training. IP multiplies this field by 2 and set that value as CTLE-AC. The default value is 0.
	27:23	RW	`Manual CTLE-DC value`	Sets by IP during Link Training. IP multiplies this field by 2 and set that value as CTLE-DC. The default value is 0.
	31:28	RW	`Manual VGA value`	Sets by IP during Link Training. IP multiplies this field by 2 and set that value as VGA. The default value is 0.
0x4D1	0	RW	`Restart Link training`	When set to 1, resets the 10GBASE-KR start-up protocol. When set to 0, continues normal operation. This bit self clears. For more information, refer to the state variable `mr_restart_training` as defined in *Clause 72.6.10.3.1 and 10GBASE-KR PMD control register bit (1.150.0) IEEE 802.3-2015.*
	4	RW	`Updated TX Coef new`	When set to 1, there are new link partner coefficients available to send. The LT logic starts sending the new values set in 0x4D4 bits[7:0] to the remote device. When set to 0, continues normal operation. This bit self clears. Must enable this override in 0x4D0 bit16.
	8	RW	`Updated RX coef new`	When set to 1, new local device coefficients are available. The LT logic changes the local TX equalizer coefficients as specified in 0x4D4 bits[23:16]. When set to 0, continues normal operation. This bit self clears. Must enable the override in 0x4D0 bit17.
0x4D2	0	RO	`Link Trained - Receiver status`	When set to 1, the receiver is trained and is ready to receive data. When set to 0, receiver training is in progress. For more information, refer to the state variable rx_trained as defined in *Clause 72.6.10.3.1 of IEEE 802.3-2015*.
	1	RO	`Link Training Frame lock`	When set to 1, the training frame delineation has been detected. When set to 0, the training frame delineation has not been detected. For more information, refer to the state variable frame_lock as defined in *Clause 72.6.10.3.1 of IEEE 802.3-2015*.

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Word Addr	Bit	R/W	Register Name	Description
	2	RO	Link Training Start-up protocol status	When set to 1, the start-up protocol is in progress. When set to 0, start-up protocol has completed. For more information, refer to the state training as defined in *Clause 72.6.10.3.1 of IEEE 802.3-2015*.
	3	RO	Link Training failure	When set to 1, a training failure has been detected. When set to 0, a training failure has not been detected For more information, refer to the state variable training_failure as defined in *Clause 72.6.10.3.1 of IEEE 802.3-2015*.
	4	RO	Link Training Error	When set to 1, excessive errors occurred during Link Training. When set to 0, the BER is acceptable.
	5	RO	Link Training Frame lock Error	When set to 1, indicates a frame lock was lost during Link Training. If the tap settings specified by the fields of 0x4D5 are the same as the initial parameter value, the frame lock error was unrecoverable.
0x4D3	9:0	RW	ber_time_frames	Specifies the number of training frames to examine for bit errors on the link for each step of the equalization settings. Used only when ber_time_k_frames is 0.The following values are defined: • A value of 2 is about 10^3 bytes • A value of 20 is about 10^4 bytes • A value of 200 is about 10^5 bytes The default value for simulation is 2'b11. The default value for hardware is 0.
	19:10	RW	ber_time_k_frames	Specifies the number of thousands of training frames to examine for bit errors on the link for each step of the equalization settings. Set `ber_time_m_frames = 0` for time/bits to match the following values: • A value of 3 is about 10^7 bits = about 1.3 ms • A value of 25 is about 10^8 bits = about 11ms • A value of 250 is about 10^9 bits = about 11 0ms The default value for simulation is 0. The default value for hardware is 0xF.
	29:20	RW	ber_time_m_frames	Specifies the number of millions of training frames to examine for bit errors on the link for each step of the equalization settings. Set `ber_time_k_frames = 4'd1000 = 0x43E8` for time/bits to match the following values: • A value of 3 is about 10^{10} bits = about 1.3 seconds • A value of 25 is about 10^{11} bits = about 11 seconds • A value of 250 is about 10^{12} bits = about 110 seconds
0x4D4	5:0	RO/RW	LD coefficient update[5:0]	Reflects the contents of the first 16-bit word of the training frame sent from the local device control channel. Normally, the bits in this register are read-only; however, when you override training by setting the `Ovride Coef enable` control bit, these bits become writeable. The following fields are defined: • [5: 4]: Coefficient (+1) update — 2'b11: Reserved — 2'b01: Increment — 2'b10: Decrement — 2'b00: Hold • [3:2]: Coefficient (0) update (same encoding as [5:4]) • [1:0]: Coefficient (-1) update (same encoding as [5:4]) For more information, refer to 10G BASE-KR LD coefficient update register bits (1.154.5:0) in *Clause 45.2.1.80.3 of IEEE 802.3-2015*.

continued...

Word Addr	Bit	R/W	Register Name	Description
	6	RO/RW	LD Initialize Coefficients	When set to 1, requests the link partner coefficients be set to configure the TX equalizer to its INITIALIZE state. When set to 0, continues normal operation. For more information, refer to 10G BASE-KR LD coefficient update register bits (1.154.12) in *Clause 45.2.1.80.3 and Clause 72.6.10.2.3.2 of IEEE 802.3-2015*.
	7	RO/RW	LD Preset Coefficients	When set to 1, requests the link partner coefficients be set to a state where equalization is turned off. When set to 0 the link operates normally. For more information, refer to 10G BASE-KR LD coefficient update register bit (1.154.13) in *Clause 45.2.1.80.3 and Clause 72.6.10.2.3.2 of IEEE 802.3-2015*.
	13:8	RO	LD coefficient status[5:0]	Status report register for the contents of the second, 16-bit word of the training frame most recently sent from the local device control channel. The following fields are defined: • [5:4]: Coefficient (post-tap) — 2'b11: Maximum — 2'b01: Minimum — 2'b10: Updated — 2'b00: Not updated • [3:2]: Coefficient (0) (same encoding as [5:4]) • [1:0]: Coefficient (pre-tap) (same encoding as [5:4]) For more information, refer to 10G BASE-KR LD status report register bit (1.155.5:0) in *Clause 45.2.1.81 of IEEE 802.3-2015*.
	14	RO	Link Training ready - LD Receiver ready	When set to 1, the local device receiver has determined that training is complete and is prepared to receive data. When set to 0, the local device receiver is requesting that training continue. Values for the receiver ready bit are defined in *Clause 72.6.10.2.4.4*. For more information, refer to 10G BASE-KR LD status report register bit (1.155.15) in *Clause 45.2.1.81 of IEEE 802.3-2015*.
	21:16	RO/RW	LP coefficient update[5:0]	Reflects the contents of the first 16-bit word of the training frame most recently received from the control channel. Normally the bits in this register are read only; however, when training is disabled by setting low the KR Training enable control bit, these bits become writeable. The following fields are defined: • [5: 4]: Coefficient (+1) update — 2'b11: Reserved — 2'b01: Increment — 2'b10: Decrement — 2'b00: Hold • [3:2]: Coefficient (0) update (same encoding as [5:4]) • [1:0]: Coefficient (-1) update (same encoding as [5:4]) For more information, refer to 10G BASE-KR LP coefficient update register bits (1.152.5:0) in *Clause 45.2.1.78.3 of IEEE 802.3-2015*.
	22	RO/RW	LP Initialize Coefficients	When set to 1, the local device transmit equalizer coefficients are set to the INITIALIZE state. When set to 0, normal operation continues. The function and values of the initialize bit are defined in *Clause 72.6.10.2.3.2*. For more information, refer to 10G BASE-KR LP coefficient update register bits (1.152.12) in *Clause 45.2.1.78.3 of IEEE 802.3-2015.*
	23	RO/RW	LP Preset Coefficients	When set to 1, the local device TX coefficients are set to a state where equalization is turned off. Preset coefficients are used. When set to 0, the local device operates normally. The

continued...

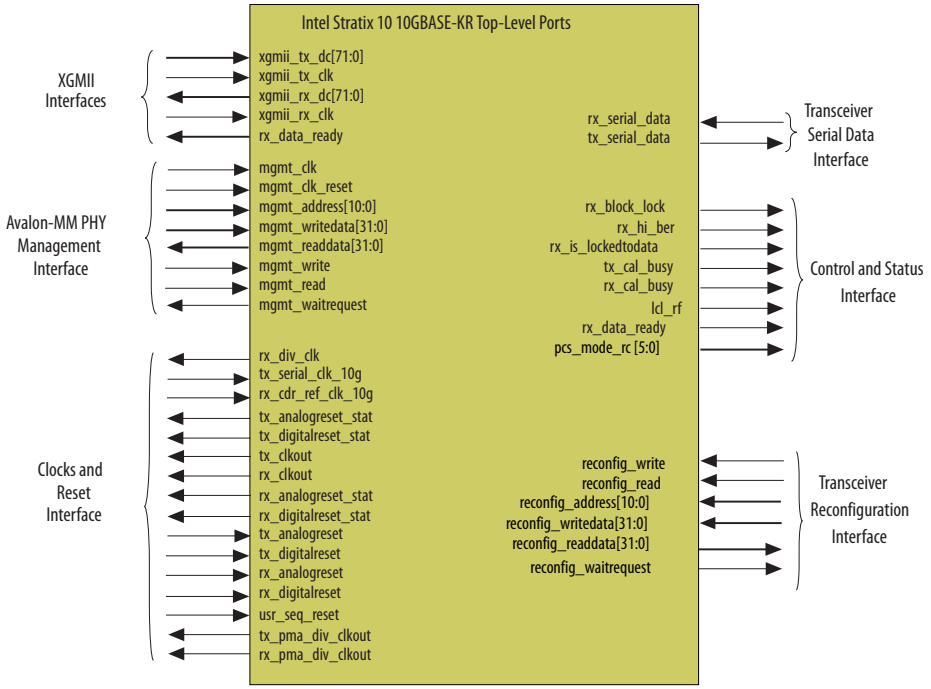
Word Addr	Bit	R/W	Register Name	Description
				function and values of the preset bit are defined in *Clause 72.6.10.2.3.1*. The function and values of the initialize bit are defined in *Clause 72.6.10.2.3.2*. For more information, refer to 10G BASE-KR LP coefficient update register bits (1.152.13) in *Clause 45.2.1.78.3 of IEEE 802.3-2015*.
	29:24	RO	LP coefficient status[5:0]	Status report register reflects the contents of the second, 16-bit word of the training frame most recently received from the control channel: The following fields are defined: • [5:4]: Coefficient (+1) — 2'b11: Maximum — 2'b01: Minimum — 2'b10: Updated — 2'b00: Not updated • [3:2]: Coefficient (0) (same encoding as [5:4]) • [1:0]: Coefficient (-1) (same encoding as [5:4]) For more information, refer to 10G BASE-KR LP status report register bits (1.153.5:0) in *Clause 45.2.1.79 of IEEE 802.3-2015*.
	30	RO	LP Receiver ready	When set to 1, the link partner receiver has determined that training is complete and is prepared to receive data. When set to 0, the link partner receiver is requesting that training continue. Values for the receiver ready bit are defined in *Clause 72.6.10.2.4.4*. For more information, refer to 10G BASE-KR LP status report register bits (1.153.15) in *Clause 45.2.1.79 of IEEE 802.3-2015*.
0x4D5	4:0	RO	LT V_{OD} setting	Stores the most recent TX V_{OD} setting trained by the link partner's RX based on the LT coefficient update logic driven by Clause 72. It reflects Link Partner commands to fine-tune the TX pre-emphasis taps.
	13:8	RO	LT Post-tap setting	Stores the most recent TX post-tap setting trained by the link partner's RX based on the LT coefficient update logic driven by Clause 72. It reflects Link Partner commands to fine-tune the TX pre-emphasis taps.
	20:16	RO	LT Pre-tap setting	Store the most recent TX pre-tap setting trained by the link partner's RX based on the LT coefficient update logic driven by Clause 72. It reflects Link Partner commands to fine-tune the TX pre-emphasis taps.
0x4D6	4:0	RW	LT VODMAX ovrd	Override value for the **VMAXRULE** parameter. When enabled, this value substitutes for the **VMAXRULE** to allow channel-by-channel override of the device settings. This only affects the local device TX output for the channel specified. This value must be greater than the **INITMAINVAL** parameter for proper operation. Note this overrides the **PREMAINVAL** parameter value.
	5	RW	LT VODMAX ovrd Enable	When set to 1, enables the override value for the **VMAXRULE** parameter stored in the LT VODMAX ovrd register field.
	12:8	RW	LT VODMIN ovrd	Override value for the **VODMINRULE** parameter. When enabled, this value substitutes for the **VMINRULE** to allow channel-by-channel override of the device settings. This override only effects the local device TX output for this channel. The value to be substituted must be less than the I**NITMAINVAL** parameter and greater than the **VMINRULE** parameter for proper operation.

continued...

Word Addr	Bit	R/W	Register Name	Description
	13	RW	`LT VODMIN ovrd Enable`	When set to 1, enables the override value for the **VODMINRULE** parameter stored in the `LT VODMin ovrd` register field.
	21:16	RW	`LT VPOST ovrd`	Override value for the **VPOSTRULE** parameter. When enabled, this value substitutes for the **VPOSTRULE** to allow channel-by-channel override of the device settings. This override only effects the local device TX output for this channel. The value to be substituted must be greater than the **INITPOSTVAL** parameter for proper operation.
	22	RW	`LT VPOST ovrd Enable`	When set to 1, enables the override value for the **VPOSTRULE** parameter stored in the `LT VPOST ovrd` register field.
	28:24	RW	`LT VPRE ovrd`	Override value for the **VPRERULE** parameter. When enabled, this value substitutes for the **VPOSTRULE** to allow channel-by-channel override of the device settings. This override only effects the local device TX output for this channel. The value to be substituted must be greater than the **INITPREVAL** parameter for proper operation.
	29	RW	`LT VPPRE ovrd Enable`	When set to 1, enables the override value for the **VPRERULE** parameter stored in the `LT VPre ovrd` register field.

6. Interface Signals

Figure 8. Intel Stratix 10 10GBASE-KR PHY Interfaces



Related Information

Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide

6.1. Clock and Reset Signals

Table 11. Clock and Reset Signals

Signal Name	Direction	Description
Clock signals		
tx_serial_clk_10g	Input	High speed clock from the 10G PLL to drive 10G PHY TX PMA. The frequency of this clock is 5.15625 GHz.
rx_cdr_ref_clk_10g	Input	10G PHY RX PLL reference clock. This clock frequency can be 644.53125 MHz or 322.2656 MHz.

continued...

Signal Name	Direction	Description
xgmii_tx_clk	Input	Clock for single data rate (SDR) XGMII TX interface to the MAC. This clock can be connected to the tx_pma_div_clkout. The frequency is 156.25 MHz. The frequencies are the same whether or not you enable FEC.
xgmii_rx_clk	Input	Clock for SDR XGMII RX interface to the MAC. This clock can be connected to the tx_pma_div_clkout. The frequency is 156.25 MHz. The frequencies are the same whether or not you enable FEC.
rx_clkout	Output	XGMII RX clock for the RX parallel data source interface. This clock frequency is 257.81 in 10G mode, and 161.13 MHz with FEC enabled. rx_clkout is a recovered clock. Therefore, the modules using this clock should be held in reset until rx_is_lockedtodata is high for enough time to indicate a stable clock. For more information, refer to *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide*.
tx_clkout	Output	XGMII/GMII TX clock for the TX parallel data source interface. This clock frequency is 257.81 MHz in 10G mode, and 161.13 MHz with FEC enabled.
mgmt_clk	Input	The clock signal that controls the Avalon-MM PHY management interface. This clock is used for both the PHY management interface and transceiver reconfiguration. You must restrict the frequency to a rate between 100 MHz and 161 MHz (inclusive) to meet the specification for the transceiver reconfiguration clock.
rx_div_clk	Output	The divided 33 clock from the received data. It drives the AN and LT logic and is sourced from the Native PHY rx_pma_div_clkout port. The frequency is 156.25 MHz for 10G. This clock is from the PMA and it is not to be used to clock the 10G RX datapath. Use tx_clkout or xgmii_rx_clk for 10G TX datapath clocking.
tx_pma_div_clkout	Output	The divided 33 clock from the TX serializer. You can use this clock for the for xgmii_tx_clk or xgmii_rx_clk. The frequency is 156.25 MHz for 10G. The frequencies are the same whether or not you enable FEC.
rx_pma_div_clkout	Output	The divided 33 clock from CDR recovered clock. The frequency is 156.25 MHz for 10G. The frequencies are the same whether or not you enable FEC. This clock is not used for clocking the 10G RX datapath.

continued...

Signal Name	Direction	Description
		`rx_pma_div_clkout` is a recovered clock. Therefore, the modules using this clock should be held in reset until`rx_is_lockedtodata` is high for enough time to indicate a stable clock. For more information, refer to *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide* .
Reset signals		
`mgmt_clk_reset`	Input	Resets the PHY management interface. This asynchronous signal is active high and level sensitive.
`tx_analogreset`	Input	Resets the analog TX portion of the transceiver PHY. Synchronous to `mgmt_clk`.
`tx_digitalreset`	Input	Resets the digital TX portion of the transceiver PHY. Synchronous to `mgmt_clk`.
`rx_analogreset`	Input	Resets the analog RX portion of the transceiver PHY. Synchronous to `mgmt_clk`.
`rx_digitalreset`	Input	Resets the digital RX portion of the transceiver PHY. Synchronous to `mgmt_clk`
`tx_analogreset_stat`	Output	When asserted, the reset sequence for TX PMA has begun. When deasserted, the reset sequence has finished. Connect to the corresponding signal in the Transceiver PHY Reset Controller IP core, which implements the appropriate reset sequence for the device.
`tx_digitalreset_stat`	Output	When asserted, the reset sequence for TX PCS has begun. When deasserted, the reset sequence has finished. Connect to the corresponding signal in the Transceiver PHY Reset Controller IP core, which implements the appropriate reset sequence for the device.

continued...

Signal Name	Direction	Description
rx_analogreset_stat	Output	When asserted, the reset sequence for RX PMA has begun. When deasserted, the reset sequence has finished. Connect to the corresponding signal in the Transceiver PHY Reset Controller IP core, which implements the appropriate reset sequence for the device.
rx_digitalreset_stat	Output	When asserted, the reset sequence for RX PCS has begun. When deasserted, the reset sequence has finished. Connect to the corresponding signal in the Transceiver PHY Reset Controller IP core, which implements the appropriate reset sequence for the device.
usr_seq_reset	Input	Resets the sequencer. Initiates a PCS reconfiguration, and may restart AN, LT or both if these modes are enabled. Synchronous to mgmt_clk.

6.2. Data Interface Signals

Table 12. XGMII Signals

The MAC drives the TX XGMII signals to the 10GbE PHY. The 10GbE PHY drives the RX XGMII signals to the MAC.

Signal Name	Direction	Clock Domain	Description
xgmii_tx_dc[71:0]	Input	Synchronous to xgmii_tx_clk	XGMII data and control for 8 lanes. Each lane consists of 8 bits of data and 1 bit of control. For interface mapping, refer to *Table: TX XGMII Mapping to Standard SDR XGMII Interface*.
xgmii_tx_clk	Input	Clock signal	Clock for single data rate (SDR) XGMII TX interface to the MAC. It should connect to xgmii_rx_clk. This clock can be connected to the tx_pma_div_clkout; however, Intel recommends that you connect it to a PLL for use with the Triple Speed Ethernet IP function. The frequency is 125 MHz for 1G and 156.25 MHz for 10G. This clock is driven from the MAC. The frequencies are the same whether or not you enable FEC.
xgmii_rx_dc[71:0]	Output	Synchronous to xgmii_rx_clk	RX XGMII data and control for 8 lanes. Each lane consists of 8 bits of data and 1 bit of control. For interface mapping, refer to *Table: RX XGMII Mapping to Standard SDR XGMII Interface*.
xgmii_rx_clk	Input	Clock signal	Clock for SDR XGMII RX interface to the MAC. This clock can be connected to the tx_pma_div_clkout ; however, Intel recommends that you connect it to a PLL for use with the Triple Speed Ethernet IP function. The frequency is 125 MHz for 1G and 156.25 MHz for 10G. This clock is driven from the MAC. The frequencies are the same whether or not you enable FEC.

6.2.1. XGMII Mapping to Standard SDR XGMII Data

Table 13. TX XGMII Mapping to Standard SDR XGMII Interface

The 72-bit TX XGMII data bus format is different than the standard SDR XGMII interface. This table shows the mapping of this non-standard format to the standard SDR XGMII interface.

Signal Name	SDR XGMII Signal Name	Description
xgmii_tx_dc[7:0]	xgmii_sdr_data[7:0]	Lane 0 data
xgmii_tx_dc[8]	xgmii_sdr_ctrl[0]	Lane 0 control
xgmii_tx_dc[16:9]	xgmii_sdr_data[15:8]	Lane 1 data
xgmii_tx_dc[17]	xgmii_sdr_ctrl[1]	Lane 1 control
xgmii_tx_dc[25:18]	xgmii_sdr_data[23:16]	Lane 2 data
xgmii_tx_dc[26]	xgmii_sdr_ctrl[2]	Lane 2 control
xgmii_tx_dc[34:27]	xgmii_sdr_data[31:24]	Lane 3 data
xgmii_tx_dc[35]	xgmii_sdr_ctrl[3]	Lane 3 control
xgmii_tx_dc[43:36]	xgmii_sdr_data[39:32]	Lane 4 data
xgmii_tx_dc[44]	xgmii_sdr_ctrl[4]	Lane 4 control
xgmii_tx_dc[52:45]	xgmii_sdr_data[47:40]	Lane 5 data
xgmii_tx_dc[53]	xgmii_sdr_ctrl[5]	Lane 5 control
xgmii_tx_dc[61:54]	xgmii_sdr_data[55:48]	Lane 6 data
xgmii_tx_dc[62]	xgmii_sdr_ctrl[6]	Lane 6 control
xgmii_tx_dc[70:63]	xgmii_sdr_data[63:56]	Lane 7 data
xgmii_tx_dc[71]	xgmii_sdr_ctrl[7]	Lane 7 control

Table 14. RX XGMII Mapping to Standard SDR XGMII Interface

The 72-bit RX XGMII data bus format is different from the standard SDR XGMII interface. This table shows the mapping of this non-standard format to the standard SDR XGMII interface.

Signal Name	XGMII Signal Name	Description
xgmii_rx_dc[7:0]	xgmii_sdr_data[7:0]	Lane 0 data
xgmii_rx_dc[8]	xgmii_sdr_ctrl[0]	Lane 0 control
xgmii_rx_dc[16:9]	xgmii_sdr_data[15:8]	Lane 1 data
xgmii_rx_dc[17]	xgmii_sdr_ctrl[1]	Lane 1 control
xgmii_rx_dc[25:18]	xgmii_sdr_data[23:16]	Lane 2 data
xgmii_rx_dc[26]	xgmii_sdr_ctrl[2]	Lane 2 control
xgmii_rx_dc[34:27]	xgmii_sdr_data[31:24]	Lane 3 data
xgmii_rx_dc[35]	xgmii_sdr_ctrl[3]	Lane 3 control
xgmii_rx_dc[43:36]	xgmii_sdr_data[39:32]	Lane 4 data
xgmii_rx_dc[44]	xgmii_sdr_ctrl[4]	Lane 4 control
xgmii_rx_dc[52:45]	xgmii_sdr_data[47:40]	Lane 5 data

continued...

Signal Name	XGMII Signal Name	Description
xgmii_rx_dc[53]	xgmii_sdr_ctrl[5]	Lane 5 control
xgmii_rx_dc[61:54]	xgmii_sdr_data[55:48]	Lane 6 data
xgmii_rx_dc[62]	xgmii_sdr_ctrl[6]	Lane 6 control
xgmii_rx_dc[70:63]	xgmii_sdr_data[63:56]	Lane 7 data
xgmii_rx_dc[71]	xgmii_sdr_ctrl[7]	Lane 7 control

6.3. Serial Data Signals

Table 15. Serial Data Signals

Signal Name	Direction	Description
rx_serial_data	Input	RX serial input data
tx_serial_data	Output	TX serial output data

6.4. Avalon-MM Interface Signals

Table 16. Avalon-MM Interface Signals

The Avalon-MM slave interface signals provide access to all registers.

Signal Name	Direction	Clock Domain	Description
mgmt_clk	Input	Clock	The clock signal that controls the Avalon-MM PHY management interface. This clock is used for both the PHY management interface and transceiver reconfiguration. You must restrict the frequency to a rate between 100 MHz and 161 MHz (inclusive) to meet the specification for the transceiver reconfiguration clock.
mgmt_clk_reset	Input	Asynchronous reset	Resets the PHY management interface. This asynchronous signal is active high and level sensitive.
mgmt_addr[10:0]	Input	Synchronous to mgmt_clk	11-bit Avalon-MM address.
mgmt_writedata[31:0]	Input	Synchronous to mgmt_clk	Input data.
mgmt_readdata[31:0]	Output	Synchronous to mgmt_clk	Output data.
mgmt_write	Input	Synchronous to mgmt_clk	Write signal. Active high.
mgmt_read	Input	Synchronous to mgmt_clk	Read signal. Active high.
mgmt_waitrequest	Output	Synchronous to mgmt_clk	When asserted, indicates that the Avalon-MM slave interface is unable to respond to a read or write request. When asserted, control signals to the Avalon-MM slave interface must remain constant.

6.5. Transceiver Reconfiguration Signals

You access the transceiver control and status registers using the transceiver reconfiguration interface. This is an Avalon-MM interface.

The Avalon-MM interface implements a standard memory-mapped protocol. You can connect an Avalon master to this bus to access the registers of the embedded Transceiver PHY IP core.

Table 17. Reconfiguration Interface Ports with Shared Native PHY Reconfiguration Interface

These signals are synchronous to `mgmt_clk`.

Signal Name	Direction	Description
`reconfig_write`	Input	Write enable signal. Signal is active high.
`reconfig_read`	Input	Read enable signal. Signal is active high.
`reconfig_address[10:0]`	Input	Address bus. The lower 10 bits specify address and the upper bit specifies the channel (bit [10] is always 0) .
`reconfig_writedata[31:0]`	Input	A 32-bit data write bus. `reconfig_address` specifies the address.
`reconfig_readdata[31:0]`	Output	A 32-bit data read bus. Drives read data from the specified address. Signal is valid after `reconfig_waitrequest` is deasserted.
`reconfig_waitrequest`	Output	Indicates the Avalon-MM interface is busy. Keep the `reconfig_write` or `reconfig_read` asserted until `reconfig_waitrequest` is deasserted.

Related Information

Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide

6.6. Control and Status Signals

Table 18. Control and Status Signals

Signal Name	Direction	Clock Domain	Description
`rx_block_lock`	Output	Synchronous to `rx_clkout`	When asserted, indicates the block synchronizer has established synchronization.
`rx_hi_ber`	Output	Synchronous to `rx_clkout`	When asserted, indicates the BER monitor block detects a a Sync Header high bit error rate greater than 10^{-4}.
`rx_is_lockedtodata`	Output	Asynchronous signal	When asserted, indicates the RX channel is locked to input data.
`tx_cal_busy`	Output	Synchronous to `mgmt_clk`	When asserted, indicates that the TX channel is being calibrated.
`rx_cal_busy`	Output	Synchronous to `mgmt_clk`	When asserted, indicates that the RX channel is being calibrated.

continued...

Signal Name	Direction	Clock Domain	Description
`lcl_rf`	Input	Synchronous to `xgmii_tx_clk`	When asserted, indicates a Remote Fault (RF).The MAC sends this fault signal to its link partner. This corresponds to bit D13 of the Auto Negotiation Link Codeword Base Page.
`rx_data_ready`	Output	Synchronous to `xgmii_rx_clk`	When asserted, indicates that the MAC can begin sending data to the PHY.
`pcs_mode_rc [5:0]`	Output	Synchronous to `mgmt_clk`	Specifies the PCS mode for reconfiguration. One-hot encoded. This signal has the following valid values: • 6'b000001: Auto-Negotiation mode • 6'b000010: Link Training mode • 6'b000100: 10GBASE-KR data mode • 6'b001000: Reserved • 6'b010000: Reserved • 6'b100000:10G data mode with FEC

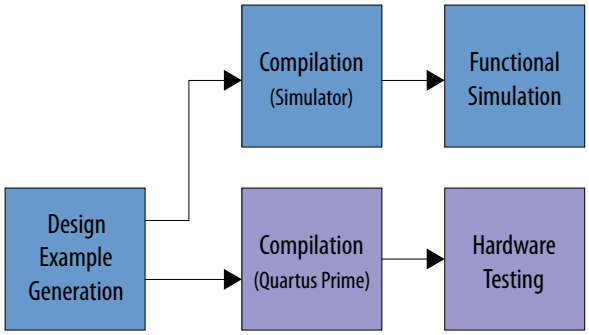
7. Design Example

7.1. Quick Start Guide

The Intel Stratix 10 10GBASE-KR PHY IP core provides a simulation testbench and a hardware design example that supports compilation and hardware testing. When you generate the design example, the parameter editor automatically creates the files necessary to simulate, compile, and test the design in hardware. You can download the compiled hardware design and run it on the Intel Stratix 10 GX Signal Integrity Development Kit. The testbench and example design support all the parameter combination of the 10GBASE-KR PHY IP core.

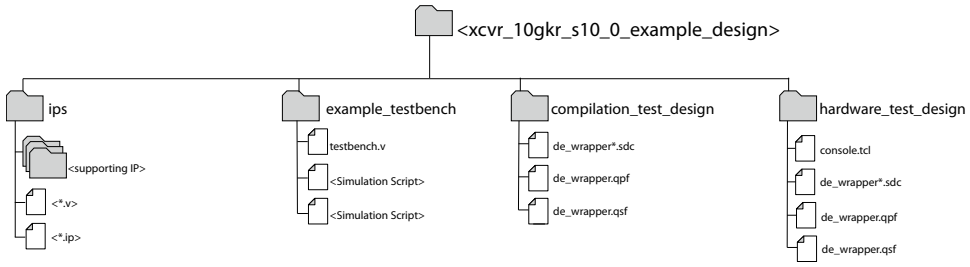
In addition, Intel provides a compilation-only example project that you can use to quickly estimate IP core area and timing.

Figure 9. Design Example Usage



7.1.1. Design Example Directory Structure

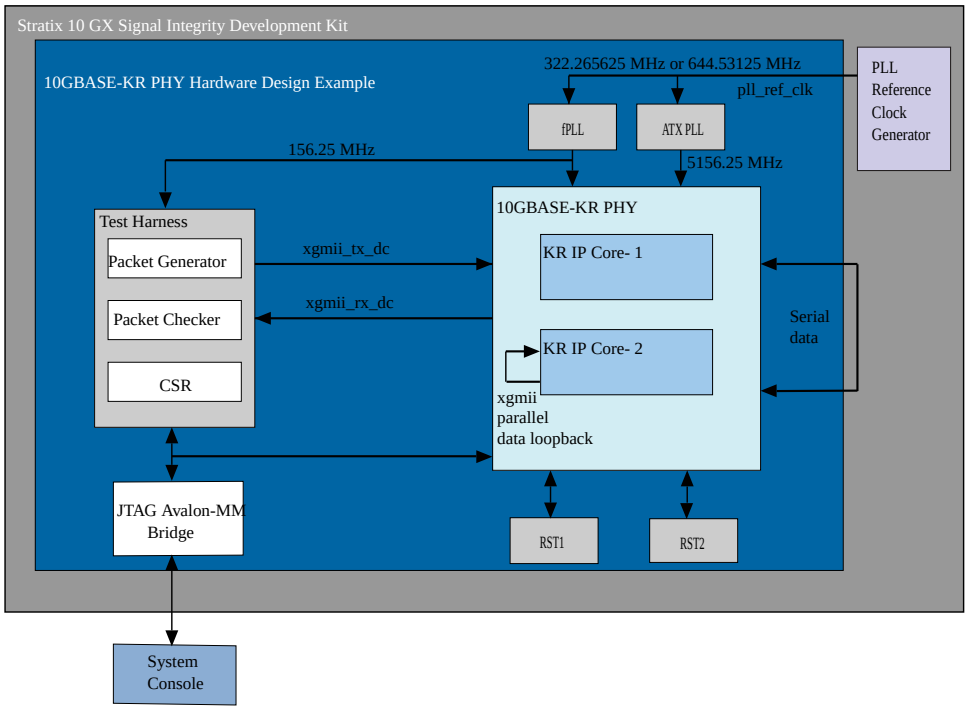
Figure 10. Intel Stratix 10 10GBASE-KR Design Example Directory Structure



The hardware configuration and test files (the hardware design example) are located in <*design_example_dir*>/hardware_test_design. The simulation files (testbench for simulation only) are located in <*design_example_dir*>/example_testbench. The compilation-only design examples is located in <*design_example_dir*>/compilation_test_design.

7.1.2. Hardware Design Example Components

Figure 11. Intel Stratix 10 10GBASE-KR PHY Hardware Design Example High Level Block Diagram



The Intel Stratix 10 10GBASE-KR hardware design example includes the following components:

1. 10GBASE-KR PHY IP core.
2. ATX PLL to generate the high-speed serial clock to drive the device transceiver channel.
3. fPLL to generate XGMII clock.
4. IO-PLL to generate a 125 MHz clock from the 50 MHz oscillator.
5. Packet Generator and Packet Checker.
6. JTAG controller that communicates with System Console. You communicate with the client logic through the System Console.

Table 19. Intel Stratix 10 10GBASE-KR PHY IP Core Hardware Design Example File Descriptions

File Names	Description
de_wrapper.qpf	Intel Quartus Prime project file
de_wrapper.qsf	Intel Quartus Prime project settings file
de_wrapper.sdc, de_wrapper_clk.sdc	Synopsys Design Constraints file. You can copy and modify this file for your own design
console.tcl	Main file for accessing System Console

7.1.3. Simulation Design Example Components

The simulation design example top-level test file is testbench.v.

Table 20. Intel Stratix 10 10GBASE-KR PHY IP Core Testbench File Descriptions

File Name	Description
Testbench and Simulation Files	
testbench.v	Top-level testbench file. The testbench instantiates the DUT and runs Verilog HDL tasks to generate and accept packets.
Testbench Scripts	
run_vsim.do	The Mentor Graphics ModelSim script to run the testbench.
run_vcs.sh	The Synopsys VCS script to run the testbench.
run_ncsim.sh	The Cadence NCSim script to run the testbench.

7.1.4. Generating the Design Example

Figure 12. Procedure

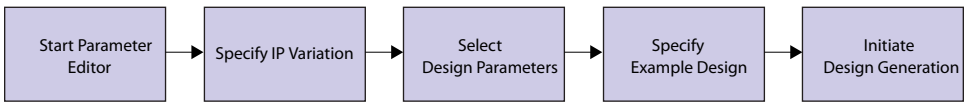
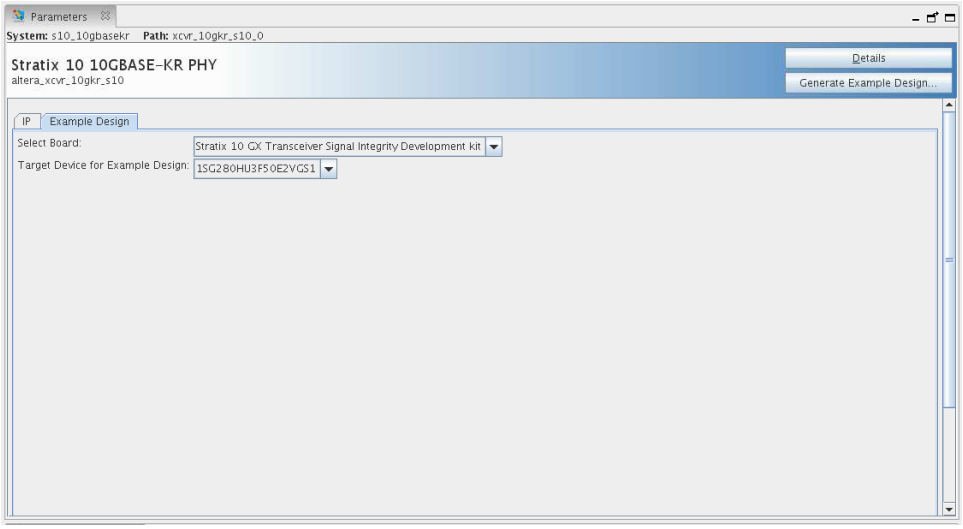


Figure 13. Example Design Tab in the Intel Stratix 10 10GBASE-KR Parameter Editor



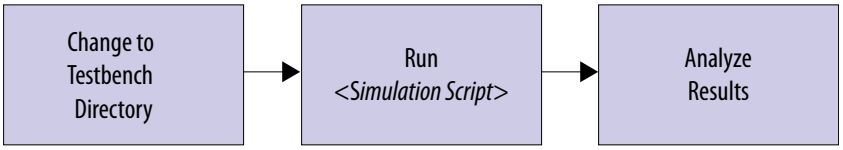
Follow these steps to generate the hardware design example and testbench:

1. In the Intel Quartus Prime Pro Edition, click **File ➤ New Project Wizard** to create a new Intel Quartus Prime project, or **File ➤ Open Project** to open an existing Intel Quartus Prime project. The wizard prompts you to specify a device family and device.
2. In the IP Catalog, locate and double-click **Stratix 10 10GBASE-KR PHY**. The **New IP Variant** window appears.
3. Specify a top-level name <*your_ip*> for your custom IP variation. The parameter editor saves the IP variation settings in a file named <*your_ip*>`.ip`.
4. Click **OK**. The parameter editor appears.
5. On the **IP** tab, specify the parameters for your IP core variation.
6. On the **Example Design** tab, for **Select Board** option, select the **Stratix 10 GX Transceiver Signal Integrity Board**, then select **Target Device for Example Design** to match the device on target board.

   If you select **None** for **Select Board** option, then the design example is generated for the device you select when you create a project.
7. Click the **Generate Example Design** button. The **Select Example Design Directory** window appears.
8. If you want to modify the design example directory path or name from the defaults displayed (`xcvr_10gkr_s10_0_example_design`), browse to the new path and type the new design example directory name (<*`design_example_dir`*>).
9. Click **OK**.

7.1.5. Simulating the Intel Stratix 10 10GBASE-KR Design Example Testbench

Figure 14. Procedure



Follow these steps to simulate the testbench:

1. Change to the testbench simulation directory *<design_example_dir>*/example_testbench
2. Run the simulation script for the supported simulator of your choice. The script compiles and runs the testbench in the simulator. Refer to the table "Steps to Simulate the Testbench".
3. Analyze the results. The successful testbench sends and receives XGMII, and displays "END OF TESTING"

Table 21. Steps to Simulate the Testbench

Simulator	Instructions
ModelSim	In the command line, type `vsim -c -do run_vsim.do`
NCSim	In the command line, type `sh run_ncsim.sh`
VCS	In the command line, type `sh run_vcs.sh`

The following sample output illustrates a successful simulation test run:

```
Start frame detected, byteslip 0, time 1362044322
Address 0x0000f002 data 0x00000053
Address 0x0000f004 data 0x000001a2
Address 0x0000f005 data 0x000001a2
Total BASER traffic cycle errors: 0
10G Traffic Test PASSED..!!!
**
END OF TESTING...
**
****************************************
```

7.1.6. Compiling and Configuring the Design Example in Hardware

To compile the hardware design example and configure it on your Intel Stratix 10 device, follow these steps:

1. Ensure hardware design example generation is complete.
2. In the Intel Quartus Prime Pro Edition software, open the Intel Quartus Prime project *<design_example_dir>*/hardware_test_design/de_wrapper.qpf.
3. On the **Processing** menu, click **Start Compilation**.
4. After you generate a SRAM object file (.sof), follow these steps to program the hardware design example on the Intel Stratix 10 device:

a. On the **Tools** menu, click **Programmer**.
b. In the **Programmer**, click **Hardware Setup**.
c. Select a programming device.
d. Select and add the **Intel Stratix 10 Transceiver Signal Integrity Development Kit** to your Intel Quartus Prime session.
e. Ensure that **Mode** is set to **JTAG**.
f. Select the Intel Stratix 10 device and click **Add Device**. The Programmer displays a block diagram of the connections between the devices on your board.
g. In the row with your `.sof`, check the box for the `.sof`.
h. Check the box in **Program/Configure** column.
i. Click **Start**.

Related Information

- Design Compilation
- Programming Intel FPGA Devices

7.1.7. Testing the Hardware Design Example

After you compile the Intel Stratix 10 10GBASE-KR PHY IP core design example and configure it on your Intel Stratix 10 GX device, you can use the System Console to program the IP core and its embedded Native PHY IP core registers.

To turn on the System Console and test the hardware design example, follow these steps:

1. After the hardware design example is configured on the Intel Stratix 10 device, in the Intel Quartus Prime Pro Edition software, on the **Tools** menu, click **System Debugging Tools ➤ System Console**.
2. In the Tcl Console pane, type `cd hardware_test_design` to change directory to `<design_example_dir>/hardware_test_design`.
3. Type `source console.tcl` to open a connection to the JTAG master.

You can program the IP core with the following design example commands:

- `loop_on`: Turns on internal serial loopback.
- `loop_off`: Turns off internal serial loopback.
- `reconfig_read <channel> <addr>`: Returns the IP core register value at <*channel*> and <*addr*>.
- `reconfig_write <channel> <addr> <data>`: Writes <*data*> to the IP core register at <*channel*> and <*addr*>.
- `rst <channel>`: Reset the instance of KR IP.
- `dis_max_wait_timer`: Disables the link training max wait timer.
- `dis_nonce`: Ignores nonce during AN. This allows AN to work if channel is looped back to itself.

- `rd_seq_stat`: Display status from sequencer block.
- `rd_an_stat`: Display status back from AN block.
- `rd_lt_stat`: Display status back from LT block.

Related Information

- Intel Stratix 10 10GBASE-KR PHY Design Example Registers on page 49
- Analyzing and Debugging with System Console

7.2. Design Example Description

The design example demonstrates the functions of the Intel Stratix 10 10GBASE-KR PHY IP core. You can generate the design from the **Example Design** tab in the Intel Stratix 10 10GBASE-KR PHY IP parameter editor.

To generate the design example, you must first set the parameter values for the IP core variation you intend to generate in your end product. Generating the design example creates a copy of the IP core; the testbench and hardware design example use this variation as the DUT.

Related Information

Specifying the IP Core Parameters and Options on page 10

7.2.1. Hardware and Software Requirements

To test the example design, use the following hardware and software:

- Intel Quartus Prime Pro Edition software
- Intel Stratix 10 GX Signal Integrity Development Kit
- System Console
- ModelSim, VCS, NCSim simulator

7.2.2. Design Example Behavior

The testbench sends traffic through the IP core, exercising the transmit side and receive side of the IP core. In the hardware design example, you can program the IP core in internal serial loopback mode and generate traffic on the transmit side that loops back through the receive side.

7.2.3. Design Example Interface Signals

The Intel Stratix 10 10GBASE-KR testbench is self-contained and does not require you to drive any input signals.

Table 22. Intel Stratix 10 10GBASE-KR Hardware Design Example Interface Signals

Signal	Direction	Description
`pll_refclk`	Input	Transceiver reference clock. Drive at 644.53125 or 322.255626 MHz.
`clk50`	Input	System clock input. Drive at 50 MHz. The intent is to drive this from a 50 MHz oscillator on the board.
`cpu_resetn`	Input	Resets the IP core. Active low. Drives the global hard reset `csr_reset_n` to the IP core.
`user_pb[7:0]`	Input	User push buttons. The hardware design example connects these bits to drive push buttons on the target board.
`ch0_rx_serial_data`	Input	Channel 0 Transceiver PHY input serial data.
`ch1_rx_serial_data`	Input	Channel 1 Transceiver PHY input serial data.
`ch0_tx_serial_data`	Output	Channel 0 Transceiver PHY output serial data.
`ch1_tx_serial_data`	Output	Channel 1 Transceiver PHY output serial data.
`user_led[7:0]`	Output	Status signals. The hardware design example connects these bits to drive LEDs on the target board.

Related Information

Interface Signals on page 34

7.2.4. Intel Stratix 10 10GBASE-KR PHY Design Example Registers

Table 23. Intel Stratix 10 10GBASE-KR Hardware Design Example Register Map

Lists the memory mapped register ranges for the hardware design example. You access these registers with the `reconfig_read` and `reconfig_write` functions in the System Console.

Word Offset	Name	Description
0x0000–0x07FF	`CH0_PHY`	Channel 0 Native PHY access
0x0800–0x08FF	`CH0_PHY`	Channel 0 10G-Base-KR IP CSR access
0x1000–0x17ff	`CH1_PHY`	Channel 1 Native PHY access
0x1800–0x18FF	`CH1_PHY`	Channel 1 10G-Base-KR IP CSR access
0xF000–0xFFFF	Test Harness	Refer to the table *Test Harness Register Map*

Note: For an example, to access 0x4B0 address of CH0 IP register, use the absolute address 0x4B0+0x800 that is 0xCB0.

Table 24. Test Harness Register Map

Word Offset	Bit	R/W	Name	Description
0x00	0	RWSC	Start XGMII packets	When set to 1, sends the specified number of XGMII packets.
0x01	0	RW	Reset Hold	When set to 1, holds the channel in reset. This bit must be written to 0 for normal operation.
	8	RW	Generator Reset	When set to 1, holds the XGMII and GMII generators in reset. Bit must be written to 0 for normal operation.
0x02	0	R	rx_data_ready	When asserted, indicates the block synchronizer has successfully established synchronization. The incoming XGMII data block locks the receiver.
	1	R	XGMII checker_pass	When asserted indicates that the received frames are exactly same as the transmitted frames. When XGMII rx_mismatch asserted, this is set to 0.
	2	R	XGMII rx_mismatch	Asserted even if single received frame doesn't match the transmitted frame.
	3	R	XGMII fifo_full	Shows the XGMII FIFO on the TX side is full. When set to 1, indicates error condition.
	4	R	test_done	When asserted indicates that the transmitter sent all 418 frames. Each frame is 64-bit wide data and 2-bit control.
	5	R	XGMII frame_done	When asserted indicates that the transmitter finished sending particular type of frames and then goes low automatically.

continued...

Word Offset	Bit	R/W	Name	Description
	6	R	`XGMII test_pass`	When asserted, XGMII has received all sent packets and there is no mismatch in received data. XGMII status= rx_data_ready & checker_pass & ! rx_mismatch
0x03	Reserved			
0x04	[31:0]	RSC	`XGMII RX frame_count channel 0`	Non-idle frame count on the RX side of channel 0. This is self clearing on read.
0x05–0xFF	Reserved			

Related Information

Intel Stratix 10 10GBASE-KR PHY Registers on page 22

A. Difference between Intel Stratix 10 and Intel Arria® 10 IP Variants

Table 25. Comparison Summary

Feature	Intel Stratix 10 IP variant	Intel Arria® 10 IP variant
GMII support for IGbE	-	Available
IEEE 1588 support	-	Available
Avalon-MM Bus	Separate Avalon-MM bus for IP registers and Native PHY IP core registers.	Single Avalon-MM bus for IP registers and Native PHY IP core registers.
Synopsys Design Constraints (SDC)	Available with IP generation.	Available with design example generation.

B. Intel Stratix 10 10GBASE-KR PHY IP Core User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
17.1	Intel Stratix 10 10GBASE-KR PHY IP Core User Guide

C. Document Revision History for Intel Stratix 10 10GBASE-KR PHY IP Core User Guide

Document Version	Intel Quartus Prime Version	IP Version	Changes
2019.07.19	19.2	19.1.1	• Intel Stratix 10 L-tile device support is now available for this IP in the current of the Intel Quartus Prime software. • Renamed the parameter **Altera Debug Master Endpoint** to **Native PHY Debug Master Endpoint**. • Added the following new parameters: — **VCCR_GXB and VCCT_GXB supply voltage for the transceiver** — **Enable JTAG to Avalon Master Bridge** • Modified the following commands in section *Testing the Hardware Design Example*: — `reg_read` to `reconfig_read` — `reg_write` to `reconfig_write`
2019.04.30	17.1	17.1	• Clarified the supported core speed grade in section *IP Core Speed Grade Support*. • Made the following changes in *Table: Test Harness Register Map*: — Modified registers names: • `XGMII rx_ready` to `rx_data_ready` • `XGMII test_done` to `test_done` — Updated the description of the signals: `rx_data_ready`, `XGMII_checker_pass`, `rx_mismatch`, `XGMII fifo_full`, `XGMII test_done`, and `XGMII frame_done`. — Added new register `XGMII RX frame_count channel 0`

Date	Version	Changes
November 2017	2017.11.06	• Updated for Intel Quartus Prime Pro Edition 17.1 release. • Added new chapter *Getting Started* explaining how to install, generate and integrate IP core in your design. • Added new chapter *Design Example* to demonstrate the functions of the IP core. • Updated device support for Intel Stratix 10 device with L-Tile transceivers in Table: *Intel Stratix 10 10GBASE-KR PHY IP Core Device Family Support*. • Changed chapter title from *About Intel Stratix 10 10GBASE-KR PHY IP Core* to *Datasheet*. • Modified chapter *Datasheet* to document the *Intel Stratix 10 10GBASE-KR PHY IP Core Supported Features*. • Updated description of **Target Stratix-10 transceiver tile**, **Avalon-MM clock frequency**, and **Link fail inhibit time for 10Gb Ethernet** parameters in Table: *Intel Stratix 10 10GBASE-KR PHY IP Core Parameters: IP Tab*. • Added bits 2, 3, 18, 19, [22:20], [27:23], [31:38] to register address 0x4D0. • Corrected encoding for 1000BASE-KX and 10GBASE-KX4 mode of KR `AN Link Ready [5:0]` register. • Changed the register address 0x4B0 [8] to reserved. • Updated description of Tab **PMA parameters** in Table: *Intel Stratix 10 10GBASE-KR PHY IP Core Parameters: IP Tab*. • Corrected description of `lcl_rf` signal in *Control and Status Signals* section. • Removed signal `reconfig_reset` from *Transceiver Reconfiguration Signals* section. • Added new clock signal `rx_div_clk` in *Clock and Reset Signals* section. • Added VHDL simulation model support.
June 2017	2017.06.08	Initial release.