



# **AN 837: Design Guidelines for HDMI Intel FPGA IP**



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## 1. Design Guidelines for HDMI Intel® FPGA IP

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The design guidelines help you implement the High-Definition Multimedia Interface (HDMI) Intel FPGA IPs using FPGA devices.

These guidelines facilitate board designs for the HDMI Intel® FPGA IP video interfaces.

### Related Information

- [HDMI Intel FPGA IP User Guide](#)
- [AN 745: Design Guidelines for Intel FPGA DisplayPort Interface](#)

### 1.1. HDMI Intel FPGA IP Design Guidelines

The HDMI Intel FPGA interface has Transition Minimized Differential Signaling (TMDS) data and clock channels. The interface also carries a Video Electronics Standards Association (VESA) Display Data Channel (DDC).

The TMDS channels carry video, audio, and auxiliary data. The DDC is based on I<sup>2</sup>C protocol. The HDMI Intel FPGA IP core uses the DDC to read Extended Display Identification Data (EDID) and exchange configuration and status information between an HDMI source and sink.

### 1.2. HDMI Intel FPGA IP Board Design Tips

When you are designing your HDMI Intel FPGA IP system, consider the following board design tips.

- Use no more than two vias per trace and avoid via stubs
- Match the differential pair impedance to the impedance of the connector and cable assembly (100 ohm  $\pm$ 10%)
- Minimize inter-pair and intra-pair skew to meet the TMDS signal skew requirement
- Avoid routing a differential pair over a gap in the underneath plane
- Use standard high speed PCB design practices
- Use level shifters to meet electrical compliance at both TX and RX
- Use robust cables, such as Cat2 cable for HDMI 2.0

### 1.3. Schematic Diagrams

The Bitenc schematic diagrams in the provided links illustrate the topology for the Intel FPGA development boards.

Using HDMI 2.0 link topology requires you to meet the 3.3 V electrical compliance. To meet the 3.3 V compliance on Intel FPGA devices, you need to use a level shifter. Use a DC-coupled redriver or retimer as the level shifter for the transmitter and receiver.

The external vendor devices are TMDS181 and TDP158RSBT, both running on DC-coupled links. You need a proper pull-up at CEC lines to ensure functionality when inter-operating with other consumer remote control devices.

The Bitec schematic diagrams are CTS-certified. Certification is, however, product level specific. Platform designers are advised to certify the final product for proper functionality.

#### Related Information

- [Schematic Diagram for HSMC HDMI Daughter Card Revision 8](#)
- [Schematic Diagram for FMC HDMI Daughter Card Revision 11](#)
- [Schematic Diagram for FMC HDMI Daughter Card Revision 6](#)

### 1.4. Hot-Plug Detect (HPD)

The HPD signal depends on the incoming +5V Power signal, for example, the HPD pin may be asserted only when the +5V Power signal from the source is detected.

To interface with an FPGA, you need to translate the 5V HPD signal to the FPGA I/O voltage level (VCCIO), using a voltage level translator such as TI TXB0102, which does not have pull-up resistors integrated. An HDMI source needs to pull down the HPD signal so that it can reliably differentiate between a floating HPD signal and a high voltage level HPD signal.

An HDMI sink +5V Power signal must be translated to FPGA I/O voltage level (VCCIO). The signal must be weakly pulled down with a resistor (10K) to differentiate a floating +5V Power signal when not driven by an HDMI source. An HDMI source +5V Power signal has over-current protection of no more than 0.5A.

### 1.5. HDMI Intel FPGA IP Display Data Channel (DDC)

The HDMI Intel FPGA IP DDC is based on the I<sup>2</sup>C signals (SCL and SDA) and require pull-up resistors.

To interface with an Intel FPGA, you need to translate the 5V SCL and SDA signal level to the FPGA I/O voltage level (VCCIO) using a voltage level translator, such as TI TXS0102 as used in the Bitec HDMI 2.0 daughter card. The TI TXS0102 voltage level translator device integrates internal pull-up resistors so that no on-board pull-up resistors are needed.

## 2. Document Revision History for AN 837: Design Guidelines for HDMI Intel FPGA IP

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| Document Version | Changes                                                                                                                                                                                                                                                                                                                                                                                                                |
|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2019.01.28       | <ul style="list-style-type: none"> <li>Renamed the HDMI IP name as per Intel rebranding.</li> <li>Added the <i>Schematic Diagrams</i> section that describes the Bitec schematic diagrams used with Intel FPGA boards.</li> <li>Added a link to schematic diagram for Bitec FMC HDMI daughter card revision 11.</li> <li>Added more design tips in the <i>HDMI Intel FPGA IP Board Design Tips</i> section.</li> </ul> |

| Date         | Version    | Changes                                                                                                                                                                                                                                                                             |
|--------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| January 2018 | 2018.01.22 | <p>Initial release.</p> <p><i>Note:</i> This document contains HDMI Intel FPGA design guidelines that were removed from <i>AN 745: Design Guidelines for DisplayPort and HDMI Interfaces</i> and renamed <i>AN 745: Design Guidelines for Intel FPGA DisplayPort Interface</i>.</p> |