Intel® FPGA Power and Thermal Calculator User Guide

Updated for Quartus® Prime Design Suite: **24.1**

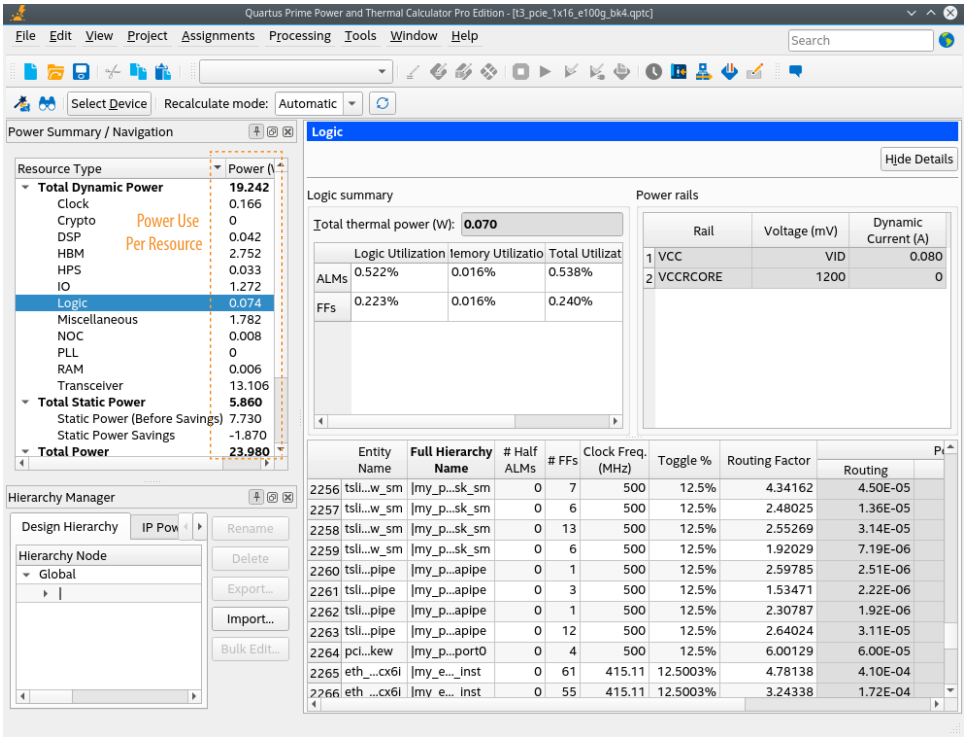
Answers to Top FAQs:

Contents

1. Overview of the Intel® FPGA Power and Thermal Calculator

This document describes how to use the Intel® FPGA Power and Thermal Calculator (PTC). The Intel FPGA PTC estimates your design's power consumption and provides thermal design parameters for Agilex™ 5, Agilex 7 and Stratix® 10 devices.(1) The Intel FPGA PTC allows early analysis of the factors contributing to FPGA power consumption, allowing you to adjust your design for greater power and thermal efficiency.

Figure 1. Intel FPGA Power and Thermal Calculator



(1) The Intel FPGA PTC does not support Arria® 10, Cyclone® 10, and earlier devices. Use the corresponding Early Power Estimator for these devices.

Key abilities of the Intel FPGA PTC include:

- Estimate the power consumption of your design before creating, and at various stages during the design process.
- Determine preliminary thermal assessments of your design.
- Section data input and results along hierarchical boundaries to view and improve power consumption per design hierarchy.
- Export, import, and reuse Intel FPGA PTC data for a particular design hierarchy.

Note: Intel FPGA PTC results are an *estimate* of power consumption and thermal properties, not an exact specification of actual consumption during device operation. You must verify the actual power consumption during device operation because actual consumption is impacted by the device and design input signals. Refer to *Measuring Static Power* for information on how to measure device static power in a way that correlates with the way that Intel FPGA PTC reports static power.

Once your design is ready to compile, switch to the Quartus® Prime Power Analyzer for more accurate power analysis results. The Quartus Prime Power Analyzer produces more accurate results because the Compiler generates more detailed information about your design that influences the analysis tool, such as routing and configuration information that impact power consumption.

1.1. Accessing the Intel FPGA Power and Thermal Calculators

For convenience, the Intel FPGA Power and Thermal Calculator (PTC) is available either as a standalone application, or embedded within the Quartus Prime software. Each version has a different method to access and launch.

Table 1. Power and Thermal Calculator Versions Available

Intel FPGA PTC Version	Description	Access and Run
Embedded Intel FPGA PTC	Launched from within the Quartus Prime software. Populates the Intel FPGA PTC from project settings and compilation results. The PTC assumes the current device selected in the Quartus Prime software. If the current device is not supported by the PTC, it assumes a default device and displays an informative message.	In the Quartus Prime software, click **Tools ➤ Power and Thermal Calculator**, or type the `quartus_ptc` command in the Quartus Prime software command shell.
Standalone Intel FPGA PTC	Runs independently from the Quartus Prime software and includes all features in the embedded Intel FPGA PTC. You input all data manually, or import from a `.ptc` file. Helpful in early design when power and cooling requirements are necessary but RTL is not yet available.	Available from the *Additional Software* tab of the Quartus Prime Pro Edition page of the *Download Center for FPGAs*. • To launch the Windows version, click the icon in the **Start** menu. • To launch the Linux version, type `./ptc` <Enter> in the installation folder.

1.2. Intel FPGA PTC Power Model Status

The Intel FPGA Power and Thermal Calculator (PTC) uses a device power model to calculate estimated power consumption and thermal assessments. Depending on the maturity of the device, the power models in the current version of the Intel FPGA PTC may be in advance, preliminary, or final status. The status of the power models relate to the accuracy of the estimated results.

The **Main** page of the Intel FPGA PTC shows the current power model status for the target device:

- Advance power models— based on simulation results, process model projections, and design targets. Advance power models may change over time.
- Preliminary power models—include post-layout simulation results, process data, and initial silicon correlation results. Preliminary power models may change over time.
- Final power models—correlate to production devices with thousands of designs, and are not expected to change.

The accuracy of the power model is determined on a per-power-rail basis for the Intel FPGA PTC.

- For most Stratix 10 designs, the Intel FPGA Power and Thermal Calculator has the following accuracy, assuming final power models: Within 15% of silicon for the majority of power rails with higher power, assuming accurate inputs and toggle rates.
- For most Agilex FPGA portfolio designs, the Intel FPGA PTC has the following accuracy, assuming final power models: Within 10% of silicon for all power rails, assuming accurate inputs and toggle rates.

For more information about power model accuracy in the Quartus Prime Power Analyzer, refer to the *Quartus Prime Pro Edition User Guide: Power Analysis and Optimization*.

Related Information

Quartus Prime Pro Edition User Guide: Power Analysis and Optimization

1.3. Definitions of Power Terms Used in this Document

The total power consumption of an Agilex or Stratix 10 device consists of the following components:

- **Static power**—the power that the configured device consumes when powered up but no user clocks are operating. Static power is dependent on device size, device grade, power characteristics, and junction temperature. Static power excludes DC bias power of analog blocks, such as I/O and transceiver analog circuitry.
- **Dynamic power**—the additional power consumption of the device due to signal activity or toggling.
- **Standby power**
  - **For Stratix 10 devices only**—Additional power, independent of signal activity or toggling, that is consumed only when specific circuitry is enabled through configuration RAM settings. Standby power includes, but is not limited to, I/O and transceiver DC bias power.
  - **For Agilex FPGA portfolio devices**—This power is included as part of the reported dynamic power.

2. Estimating Power Consumption with the Intel FPGA Power and Thermal Calculator

The Intel FPGA Power and Thermal Calculator (PTC) allows you to estimate power consumption before and during the actual FPGA design cycle.

- **Before Design**—you can estimate the power consumption when you have not yet started creating your design RTL, or when your design is only partially complete, but you need preliminary power and cooling requirements.
- **During Design**—estimating power consumption while creating the FPGA design allows you to adjust the design resources and parameters and see how those changes affect total power consumption. You can populate the Intel FPGA PTC data from actual compilation results rather than manual entry.
- **After Design**—use the Power Analyzer in the Quartus Prime software to obtain the most accurate power analysis results for completed designs. The Power Analyzer uses toggle rates from user assignments and placement-and-routing information to provide more accurate power estimates.

2.1. Estimating Power Before Starting the FPGA Design

Table 2. Advantage and Constraints of Power Estimation before Designing FPGA

Advantage	Constraint
• Obtain power estimates before starting your FPGA design. • Adjust design resources and parameters and see how those changes affect total power consumption.	• Accuracy depends on your inputs and your estimate of the device resources. Where this information may change (during or after your design is complete), your power estimation results are less accurate. • The Intel FPGA Power and Thermal Calculator (PTC) uses averages and not the actual design implementation details. The Power Analyzer has access to the full design details. For example, the Intel FPGA PTC uses average values for ALM configuration, while the Power Analyzer uses an exact configuration for each ALM.

To estimate power consumption with the Intel FPGA PTC before starting your FPGA design, follow these steps:

1. Open Intel FPGA PTC, as Accessing the Intel FPGA Power and Thermal Calculators on page 5 describes.
2. On the **Main** page of the Intel FPGA PTC, select the target device, device grade, package, and transceiver grade from the **Device**, **Device Grade**, **Package**, and **Transceiver Grade** drop-down lists.
3. Enter values for each data entry page in the Intel FPGA PTC. Each page allows you to specify the properties of different power-consuming FPGA resources in your design. To include design hierarchy information, refer to Entering Hierarchy Information Into the Intel FPGA PTC on page 25.

   The calculator displays the total estimated power consumption in the **Total Power** cell of the **Power Summary**. By default, the **Total Power** on the **Main** page is calculated using **Maximum Power** with a fixed and uniformly distributed junction

temperature of 25° C. When performing power estimates for power delivery or thermal solution design, it is important to utilize the most accurate power estimation. You can also use the calculation modes on the **Thermal** page.

4. Save the file as <*project_name*>.ptc for later use.

Note: For information on the individual pages of the Intel FPGA PTC, refer to the Power and Thermal Calculator Pages chapter.

2.2. Estimating Power While Creating the FPGA Design

If your FPGA design is partially complete, you can import a .qptc file (<*revision name*>.qptc) generated by the Quartus Prime software into the Intel FPGA Power and Thermal Calculator. After importing the information from the .qptc file into the Intel FPGA PTC, you can edit the Intel FPGA PTC data to reflect the device resource estimates for your final design.

If you have run the Quartus Prime Power Analyzer (QPA), it produces a .qptc file. (See the **Processing ➤ Start ➤ Start Power Analyzer** menu in the Quartus Prime software.)

By default, this file has a name that matches the project revision name. If you want to specify a custom name for the .qptc file, you can do so either through the Quartus Prime software (see **Assignments ➤ Settings ➤ Power Analyzer Settings ➤ Power and Thermal Calculator export file name**) or use the following assignment in the .qsf file:

```
set_global_assignment -name POWER_AND_THERMAL_CALCULATOR_EXPORT_FILE <filename>
```

When you open the Intel FPGA PTC with an Quartus Prime project (either from the **Tools** menu, or if you specified a project on the quartus_ptc command line) the PTC looks for this .qptc file and attempts to open it. If the .qptc file is not found, an error message occurs. After dismissing the error message, you are free to use the Intel FPGA PTC to enter design information manually.

Table 3. Advantages and Constraints of Power Estimation if your FPGA Design is Partially Complete

Advantage	Constraint
• You can perform power estimation early in the FPGA design cycle. • You can adjust design resources and parameters and see how those changes affect total power consumption. • Provides the flexibility to automatically populate the Intel FPGA PTC based on the Quartus Prime software compilation results.	• Accuracy depends on your inputs and your estimate of the device resources; where this information may change (during or after your design is complete). Your power estimation results may be less accurate. • Unlike the Power Analyzer, which has access to the full design details, the Intel FPGA PTC uses averages and not the actual design implementation. For example, the Intel FPGA PTC uses average values for ALM configuration, while the Power Analyzer uses an exact configuration for each ALM.

Importing a File

Importing a .qptc file saves you time and effort otherwise spent on manually entering all the information into the Intel FPGA PTC. You can also manually change any of the values after importing a file. You can create a .qptc file for an Agilex FPGA

portfolio devices-based or Stratix 10-based design, by running the Quartus Prime Power Analyzer (see the **Processing ➤ Start ➤ Start Power Analyzer** menu in the Quartus Prime software).

Importing Data into the Intel FPGA Power and Thermal Calculator

You must import the `.qptc` file into the Intel FPGA PTC before modifying any information. Also, you must verify all your information after importing a file. Importing a file from the Quartus Prime software populates all input values based on your design and design settings that were specified in the Quartus Prime software. Alternatively, you can import values exported from an earlier version of the Intel FPGA PTC.

To import data into the Intel FPGA PTC, follow these steps:

1. On the **File** menu, click **Open** and then Browse to an existing Intel FPGA `.qptc` file generated by the current or earlier version of the Intel FPGA PTC or the Quartus Prime software. Click **Open**.
2. After the file is imported into the Intel FPGA PTC, the cursor changes from busy to normal. If a problem occurs during import, the Intel FPGA PTC displays the **PTC Import Warnings** dialog box. Analyze each unexpected warning to understand the cause. Manually modify the corresponding fields in the Intel FPGA PTC after the import completes.

Importing .qptc Data for Stratix 10 Devices into the Intel FPGA Power and Thermal Calculator for Agilex FPGA Portfolio Devices

If you want to import a data file originally exported from the Quartus Prime software for a design targeting Stratix 10 devices, for use in the Agilex FPGA portfolio devices version of the Intel FPGA Power and Thermal Calculator, follow these steps:

1. In the Stratix 10 version of the Power and Thermal Calculator, open the existing `.qptc` file generated by the Quartus Prime software based on a design targeting an Stratix 10 device.
2. Save the file as a `.ptc` file, and exit the Stratix 10 Power and Thermal Calculator.
3. Launch the Power and Thermal Calculator, select **Open an existing PTC design file**, navigate to the `.ptc` file created in step 2, and click the **Override family in design file**..

Figure 2. Override Device Selection

4. Select the appropriate Agilex FPGA portfolio device and modify resources and other settings to reflect your planned design targeting the Agilex FPGA portfolio devices.

Importing an Early Power Estimator file from an Earlier Version to the Intel FPGA Power and Thermal Calculator (For Stratix 10 devices only)

If you want to import a `.csv` file originally exported from the Quartus Prime software version 19.4, or from the Early Power Estimator spreadsheet version 19.4, for a design targeting an Stratix 10 device, for use in the Stratix 10 version of the Power and Thermal Calculator version 20.3 or later, follow these steps:

1. Open the Early Power Estimator `.csv` file exported from the 19.4 version of the Quartus Prime software or Early Power Estimator spreadsheet in the Stratix 10 version of the Power and Thermal Calculator.
2. Save the file as a `.ptc` file, and exit the Stratix 10 Power and Thermal Calculator.

Appending an Imported .ptc or .qptc File to An Existing Design in the Intel FPGA Power and Thermal Calculator

With a design open in the PTC, you can use the **File ➤ Import Design** command to import an external `.ptc` or `.qptc` file and append the imported content to the current file.

Unlike the **File ➤ Open** command, **File ➤ Import Design** does not overwrite existing content; rather, imported rows are appended as new rows in the relevant tables.

Tables that cannot have multiple rows are not affected, even if they are specified in the imported profile; the PTC displays a warning message if a single-value row in the imported profile is different from the value in the PTC before the **Import Design** operation was performed.

Note: Some general guidelines about the import process:

- A `.qptc` file created for an Agilex FPGA portfolio device or Stratix 10 design, can always be imported into the Intel FPGA PTC for use with the same device family.
- A `.ptc` file created for an Stratix 10 design can be imported into the Intel FPGA PTC for use with the similar design targeting an Agilex FPGA portfolio device.
- A `.qptc` file created for an Agilex FPGA portfolio device design, cannot be imported into the Intel FPGA PTC for use with an Stratix 10 design.
- Some power-consuming resources — such as transceivers — of an original Stratix 10 design might not be carried through the import process.

Related Information

Quartus Prime Pro Edition User Guide: Power Analysis and Optimization

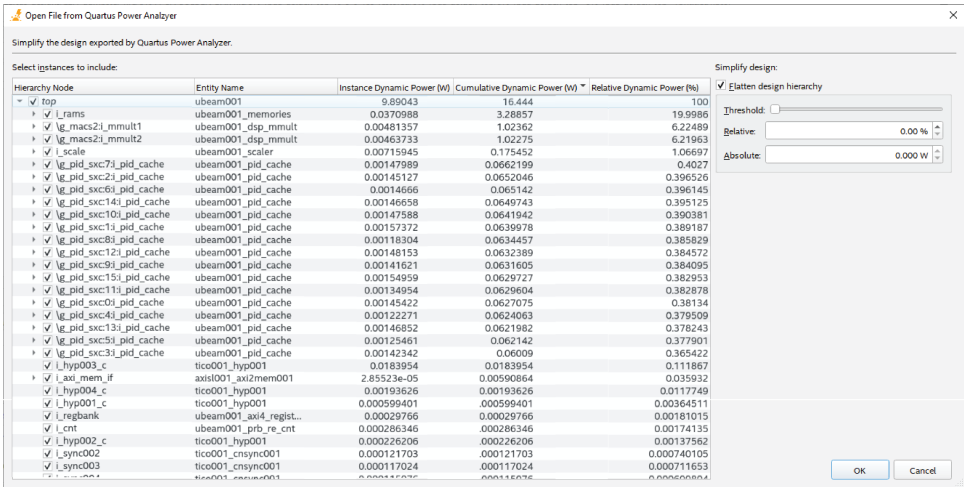
2.2.1. Importing a `.qptc` File Generated in the Quartus Prime Power Analyzer

If your design is partially complete and you have run the Quartus Prime Power Analyzer, it has created a `.qptc` file, which you can import into the Quartus Prime Power Analyzer.

You can invoke the **Import** dialog box, by clicking **File ➤ Import**, or by clicking the **Import** button in the **Hierarchy Manager**.

The **Import** operation appends the imported data to all existing sheets, as appropriate. To *overwrite* an existing design, use **File ➤ Open**.

Figure 3. Import File from Quartus Power Analyzer Dialog Box



Hierarchy Node	Entity Name	Instance Dynamic Power (W)	Cumulative Dynamic Power (W)	Relative Dynamic Power (%)
top	ubeam001	9.89043	16.444	100
i_rams	ubeam001_memories	0.0370988	3.28857	19.9986
\g_macs2:i_mmult1	ubeam001_dsp_mmult	0.00481357	1.02362	6.22489
\g_macs2:i_mmult2	ubeam001_dsp_mmult	0.00463733	1.02275	6.21963
i_scale	ubeam001_scaler	0.00715945	0.175452	1.06697
\g_pid_sxc:7:i_pid_cache	ubeam001_pid_cache	0.00147989	0.0662199	0.4027
\g_pid_sxc:2:i_pid_cache	ubeam001_pid_cache	0.00145127	0.0652046	0.396526
\g_pid_sxc:6:i_pid_cache	ubeam001_pid_cache	0.0014666	0.065142	0.396145
\g_pid_sxc:14:i_pid_cache	ubeam001_pid_cache	0.00146658	0.0649743	0.395125
\g_pid_sxc:10:i_pid_cache	ubeam001_pid_cache	0.00147588	0.0641942	0.390381
\g_pid_sxc:1:i_pid_cache	ubeam001_pid_cache	0.00157372	0.0639978	0.389187
\g_pid_sxc:8:i_pid_cache	ubeam001_pid_cache	0.00118304	0.0634457	0.385829
\g_pid_sxc:12:i_pid_cache	ubeam001_pid_cache	0.00148153	0.0632389	0.384572
\g_pid_sxc:9:i_pid_cache	ubeam001_pid_cache	0.00141621	0.0631605	0.384095
\g_pid_sxc:15:i_pid_cache	ubeam001_pid_cache	0.00154959	0.0629727	0.382953
\g_pid_sxc:11:i_pid_cache	ubeam001_pid_cache	0.00134954	0.0629604	0.382878
\g_pid_sxc:0:i_pid_cache	ubeam001_pid_cache	0.00145422	0.0627075	0.38134
\g_pid_sxc:4:i_pid_cache	ubeam001_pid_cache	0.00122271	0.0624063	0.379509
\g_pid_sxc:13:i_pid_cache	ubeam001_pid_cache	0.00146852	0.0621982	0.378243
\g_pid_sxc:5:i_pid_cache	ubeam001_pid_cache	0.00125461	0.062142	0.377901
\g_pid_sxc:3:i_pid_cache	ubeam001_pid_cache	0.00142342	0.06009	0.365422
i_hyp003_c	tico001_hyp001	0.0183954	0.0183954	0.111867
i_axi_mem_if	axisl001_axi2mem001	2.85523e-05	0.00590864	0.035932
i_hyp004_c	tico001_hyp001	0.00193626	0.00193626	0.0117749
i_hyp001_c	tico001_hyp001	0.000599401	.000599401	0.00364511
i_regbank	ubeam001_axi4_regist...	0.00029766	0.00029766	0.00181015
i_cnt	ubeam001_prb_re_cnt	0.000286346	.00028634 6	0.00174135
i_hyp002_c	tico001_hyp001	0.000226206	.00022620 6	0.00137562
i_sync002	tico001_cnsync001	0.000121703	.00012170 3	0.000740105
i_sync003	tico001_cnsync001	0.000117024	.00011702 4	0.000711653

The name rendered in italics at the top of the **Hierarchy Node** column is the name of the file to be imported. The remainder of the rows are populated with the contents of the file exported from the Quartus Prime Power Analyzer.

You can expand or collapse the display of a given hierarchy level by clicking on the arrow to the left of its hierarchy node name or by pressing the left or right arrow keys on your keyboard.

The check box to the left of each hierarchy name allows you to include or exclude that hierarchy level from being imported into the PTC. Turn on a given check box to include its corresponding hierarchy level, or turn off the check box to exclude its level.

Note:

1. If you turn on (check) a given hierarchy node, then *all* of its descendant nodes are also turned on.
2. If you turn off (uncheck) a given node, then *none* of its descendants are turned on.
3. If you turn on *some* of a given node's descendant nodes, then the parent node is *partially* turned on.
4. Turning a given node on or off *does* affect the status of its descendants, and *might* affect the status of its parents.

Table 4. Import File from Quartus Power Analyzer Information

Column Heading	Description
Hierarchy Node	Shows the names of the instances in the imported design, in a nested hierarchy.
Entity Name	Shows the entity name of the corresponding instance from the *Hierarchy Node* column.
Instance Dynamic Power (W)	Shows the estimated dynamic power of this entity instance, not including the power consumed by its descendants.

continued...

Column Heading	Description
Cumulative Dynamic Power (W)	Shows the estimated dynamic power of this entity instance, including the power consumed by its descendants.
Relative Dynamic Power (%)	Shows the estimated dynamic power of this entity instance, including the power consumed by its descendants, as a percentage of the design's total power. The relative dynamic power of the top-level instance is 100%.
Note: You can click on any of the column headings to sort the table by the values in that column.	

When you import a `.qptc` file, the Entity Name and Full Hierarchy Name of any blocks associated with a design hierarchy are automatically imported into those fields in the PTC.

Controls to Simplify the Imported Design

The controls at the right side of the dialog box allow you to flatten the imported design, effectively shrinking the design hierarchy to simplify the way it is represented in the PTC.

Table 5. Import File from Quartus Power Analyzer Controls

Control	Description
Flatten design hierarchy	Click this check box to enable and disable design flattening. When this box is disabled, the controls below it are also disabled. *Note: Design flattening* is a process by which hierarchical instances with cumulative power below a specified threshold are merged into their parent instances, thereby simplifying the design imported into the PTC, and making it easier for the PTC to model the design.
Threshold	Provides a visual control for setting the flattening threshold. Move the slider fully to the left for no flattening, or fully to the right for maximum flattening.
Relative	Allows you to specify a flattening threshold as a percentage of cumulative power.
Absolute	Allows you to specify a flattening threshold in terms of absolute dynamic power, measured in watts. The valid range of values is from 0 W to the full dynamic power estimate included in the Quartus Prime Power Analyzer report.

For more information about generating a `.qptc` file in the Quartus Prime Power Analyzer, refer to the *Quartus Prime Pro Edition User Guide: Power Analysis and Optimization*.

Related Information

Quartus Prime Pro Edition User Guide: Power Analysis and Optimization

2.3. Estimating Power After Completing the FPGA Design

If your design is complete, Intel strongly recommends that you do not use the Intel FPGA Power and Thermal Calculator (PTC). Instead, use the Power Analyzer in the Quartus Prime software. The Power Analyzer uses toggle rates from simulation, user assignments, and placement-and-routing information to provide more accurate power estimates.

Related Information

Quartus Prime Pro Edition User Guide: Power Analysis and Optimization

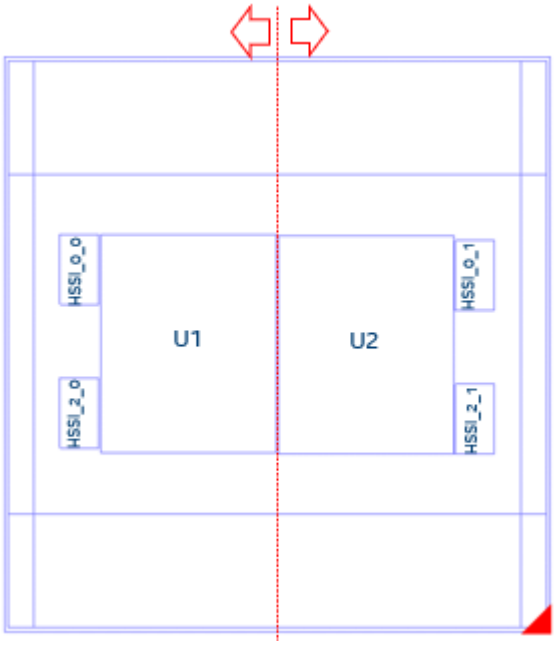
2.4. Estimating Power for Dual-Core Devices

Devices such as the Stratix 10 1SG10M contain two core dies, and are not directly supported by the Intel FPGA PTC. Power estimation for these devices requires a separate calculator, together with outputs from the Intel FPGA PTC and some transceiver data.

Package Details

The device package contains two core fabric dies, each with two associated transceivers. In the figure below, *U1* and *U2* identify the two core fabric tiles, with *HSSI_** identifying their respective transceivers.

Figure 4. Dual-core Package Layout



Generating a PTC File and Importing the Data Into the Intel FPGA PTC

1. In the Quartus Prime software, generate a PTC file for your design for the U1 tile.
2. Create a script file for U1 (for example, *design_u1.epe_script*) containing the following lines:

```
import,<U1_name>.ptc
       export_output_fields, <U1_name>.epe_dump
```

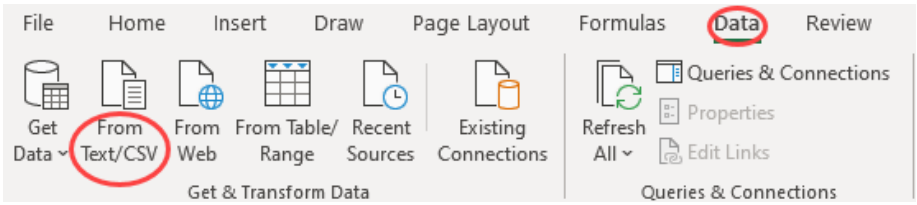
3. Generate an epe_dump file for U1, by running the following command:

```
quartus_ptc --epe_test_command=runscript --epe_input=design_u1.epe_script --
family=nadder
```

4. Download the *1SG10M_Calculator* spreadsheet from the Power Estimators and Power Analyzer page.
5. Open the *1SG10M_Calculator* spreadsheet.

6. Import the `.epe_dump` file into the spreadsheet, by clicking on **Data** in the spreadsheet menu bar, and then selecting the **From Text/CSV** icon.

Figure 5. Spreadsheet Menu Bar



7. Select the *<U1_name>.epe_dump* file that you generate in step 3, and click **Import**.
8. Ensure that *Comma* is selected in the **Delimiter** field, and click **Load**, as Specifying Comma Delimiters shows.
9. After the `.epe_dump` file loads, copy all the data from the generated worksheet and paste it into the U1 worksheet, replacing any existing data there, as Newly Generated Worksheet shows.
10. Repeat the above steps for the U2 die, as Content Copied Into U1 Worksheet shows.

Figure 6. Specifying Comma Delimiters

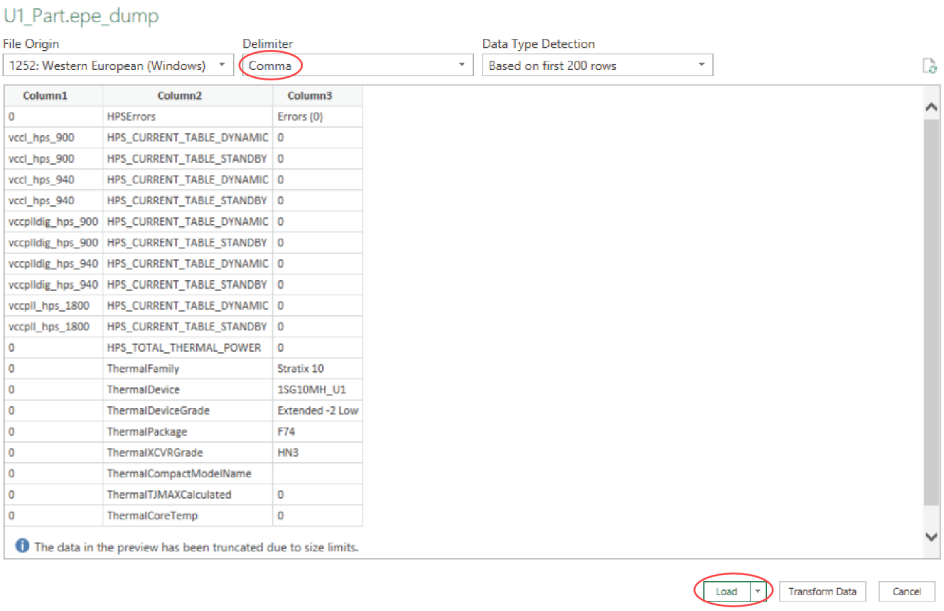
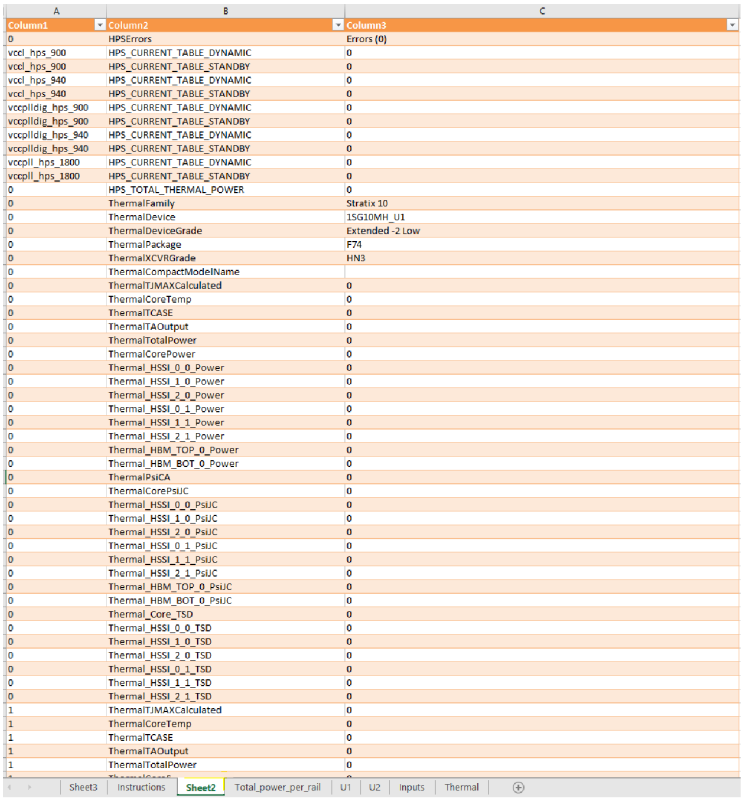


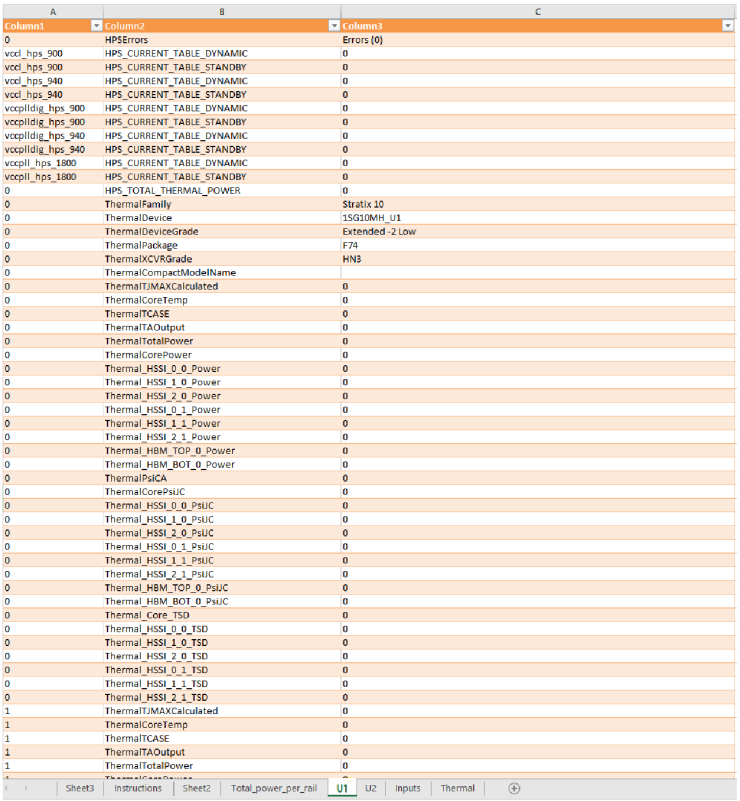
Figure 7. Newly Generated Worksheet



	A	B	C
	Column1	Column2	Column3
	0	HPSErrors	Errors (0)
	vccl_hps_900	HPS_CURRENT_TABLE_DYNAMIC	0
	vccl_hps_900	HPS_CURRENT_TABLE_STANDBY	0
	vccl_hps_940	HPS_CURRENT_TABLE_DYNAMIC	0
	vccl_hps_940	HPS_CURRENT_TABLE_STANDBY	0
	vccplldig_hps_900	HPS_CURRENT_TABLE_DYNAMIC	0
	vccplldig_hps_900	HPS_CURRENT_TABLE_STANDBY	0
	vccplldig_hps_940	HPS_CURRENT_TABLE_DYNAMIC	0
	vccplldig_hps_940	HPS_CURRENT_TABLE_STANDBY	0
	vccpll_hps_1800	HPS_CURRENT_TABLE_DYNAMIC	0
	vccpll_hps_1800	HPS_CURRENT_TABLE_STANDBY	0
	0	HPS_TOTAL_THERMAL_POWER	0
	0	ThermalFamily	Stratix 10
	0	ThermalDevice	1SG10MH_U1
	0	ThermalDeviceGrade	Extended -2 Low
	0	ThermalPackage	F74
	0	ThermalXCVRGrade	HN3
	0	ThermalCompactModelName	
	0	ThermalTJMAXCalculated	0
	0	ThermalCoreTemp	0
	0	ThermalTCASE	0
	0	ThermalTAOutput	0
	0	ThermalTotalPower	0
	0	ThermalCorePower	0
	0	Thermal_HSSI_0_0_Power	0
	0	Thermal_HSSI_1_0_Power	0
	0	Thermal_HSSI_2_0_Power	0
	0	Thermal_HSSI_0_1_Power	0
	0	Thermal_HSSI_1_1_Power	0
	0	Thermal_HSSI_2_1_Power	0
	0	Thermal_HBM_TOP_0_Power	0
	0	Thermal_HBM_BOT_0_Power	0
	0	ThermalPsiCA	0
	0	ThermalCorePsiJC	0
	0	Thermal_HSSI_0_0_PsiJC	0
	0	Thermal_HSSI_1_0_PsiJC	0
	0	Thermal_HSSI_2_0_PsiJC	0
	0	Thermal_HSSI_0_1_PsiJC	0
	0	Thermal_HSSI_1_1_PsiJC	0
	0	Thermal_HSSI_2_1_PsiJC	0
	0	Thermal_HBM_TOP_0_PsiJC	0
	0	Thermal_HBM_BOT_0_PsiJC	0
	0	Thermal_Core_TSD	0
	0	Thermal_HSSI_0_0_TSD	0
	0	Thermal_HSSI_1_0_TSD	0
	0	Thermal_HSSI_2_0_TSD	0
	0	Thermal_HSSI_0_1_TSD	0
	0	Thermal_HSSI_1_1_TSD	0
	0	Thermal_HSSI_2_1_TSD	0
	1	ThermalTJMAXCalculated	0
	1	ThermalCoreTemp	0
	1	ThermalTCASE	0
	1	ThermalTAOutput	0
	1	ThermalTotalPower	0

Sheet3 | Instructions | Sheet2 | Total_power_per_rail | U1 | U2 | Inputs | Thermal

Figure 8. Content Copied into U1 Worksheet



A	B	C
Column1	Column2	Column3
0	HPSErrors	Errors (0)
vccl_hps_900	HPS_CURRENT_TABLE_DYNAMIC	0
vccl_hps_900	HPS_CURRENT_TABLE_STANDBY	0
vccl_hps_940	HPS_CURRENT_TABLE_DYNAMIC	0
vccl_hps_940	HPS_CURRENT_TABLE_STANDBY	0
vccplldig_hps_900	HPS_CURRENT_TABLE_DYNAMIC	0
vccplldig_hps_900	HPS_CURRENT_TABLE_STANDBY	0
vccplldig_hps_940	HPS_CURRENT_TABLE_DYNAMIC	0
vccplldig_hps_940	HPS_CURRENT_TABLE_STANDBY	0
vccpll_hps_1800	HPS_CURRENT_TABLE_DYNAMIC	0
vccpll_hps_1800	HPS_CURRENT_TABLE_STANDBY	0
0	HPS_TOTAL_THERMAL_POWER	0
0	ThermalFamily	Stratix 10
0	ThermalDevice	1SG10MH_U1
0	ThermalDeviceGrade	Extended -2 Low
0	ThermalPackage	F74
0	ThermalXCVRGrade	HN3
0	ThermalCompactModelName	
0	ThermalTJMAXCalculated	0
0	ThermalCoreTemp	0
0	ThermalTCASE	0
0	ThermalTAOutput	0
0	ThermalTotalPower	0
0	ThermalCorePower	0
0	Thermal_HSSI_0_0_Power	0
0	Thermal_HSSI_1_0_Power	0
0	Thermal_HSSI_2_0_Power	0
0	Thermal_HSSI_0_1_Power	0
0	Thermal_HSSI_1_1_Power	0
0	Thermal_HSSI_2_1_Power	0
0	Thermal_HBM_TOP_0_Power	0
0	Thermal_HBM_BOT_0_Power	0
0	ThermalPsICA	0
0	ThermalCorePsiJC	0
0	Thermal_HSSI_0_0_PsiJC	0
0	Thermal_HSSI_1_0_PsiJC	0
0	Thermal_HSSI_2_0_PsiJC	0
0	Thermal_HSSI_0_1_PsiJC	0
0	Thermal_HSSI_1_1_PsiJC	0
0	Thermal_HSSI_2_1_PsiJC	0
0	Thermal_HBM_TOP_0_PsiJC	0
0	Thermal_HBM_BOT_0_PsiJC	0
0	Thermal_Core_TSD	0
0	Thermal_HSSI_0_0_TSD	0
0	Thermal_HSSI_1_0_TSD	0
0	Thermal_HSSI_2_0_TSD	0
0	Thermal_HSSI_0_1_TSD	0
0	Thermal_HSSI_1_1_TSD	0
0	Thermal_HSSI_2_1_TSD	0
1	ThermalTJMAXCalculated	0
1	ThermalCoreTemp	0
1	ThermalTCASE	0
1	ThermalTAOutput	0
1	ThermalTotalPower	0

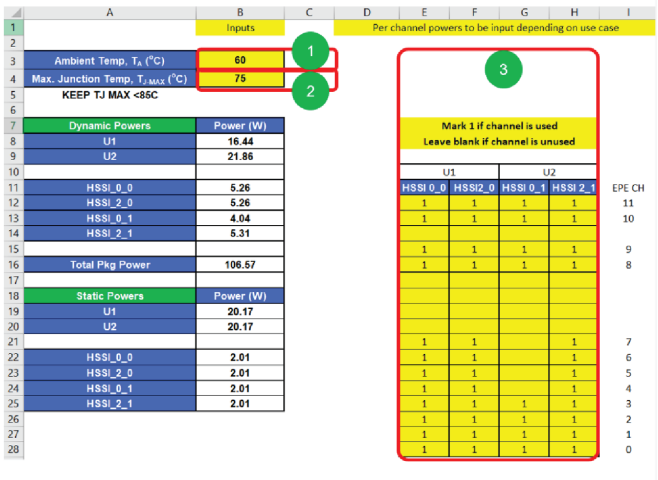
Sheet3 | Instructions | Sheet2 | Total_power_per_rail | U1 | U2 | Inputs | Thermal

Interpreting the Spreadsheet

The **Total_power_per_rail** worksheet shows the power summary for both U1 and U2 — in this case, 1SG10M as a whole device. On the **Inputs** worksheet, you need to provide the **Ambient Temp**, **Max Junction Temp**, **$T_{J\text{-}MAX}$**, and **HSSI** information.

Figure 9. Input Tab

Inputs-
1. Ambient temperature
2. Max Tj at which U1 and U2 are generated
3. HSSI channels that are in use
   - Mark '1' if channel is in use
   - Leave cell blank if channel is not in use



	A	B	C	D	E	F	G	H	I
1		Inputs		Per channel powers to be input depending on use case					
2									
3	Ambient Temp, T_A (°C)	60	1						
4	Max. Junction Temp, $T_{J\text{-}MAX}$ (°C)	75	2						
5	KEEP TJ MAX <85C								
6									
7	Dynamic Powers	Power (W)							
8	U1	16.44							
9	U2	21.86							
10									
11	HSSI_0_0	5.26							
12	HSSI_2_0	5.26							
13	HSSI_0_1	4.04							
14	HSSI_2_1	5.31							
15									
16	Total Pkg Power	106.57							
17									
18	Static Powers	Power (W)							
19	U1	20.17							
20	U2	20.17							
21									
22	HSSI_0_0	2.01							
23	HSSI_2_0	2.01							
24	HSSI_0_1	2.01							
25	HSSI_2_1	2.01							
26									
27									
28									

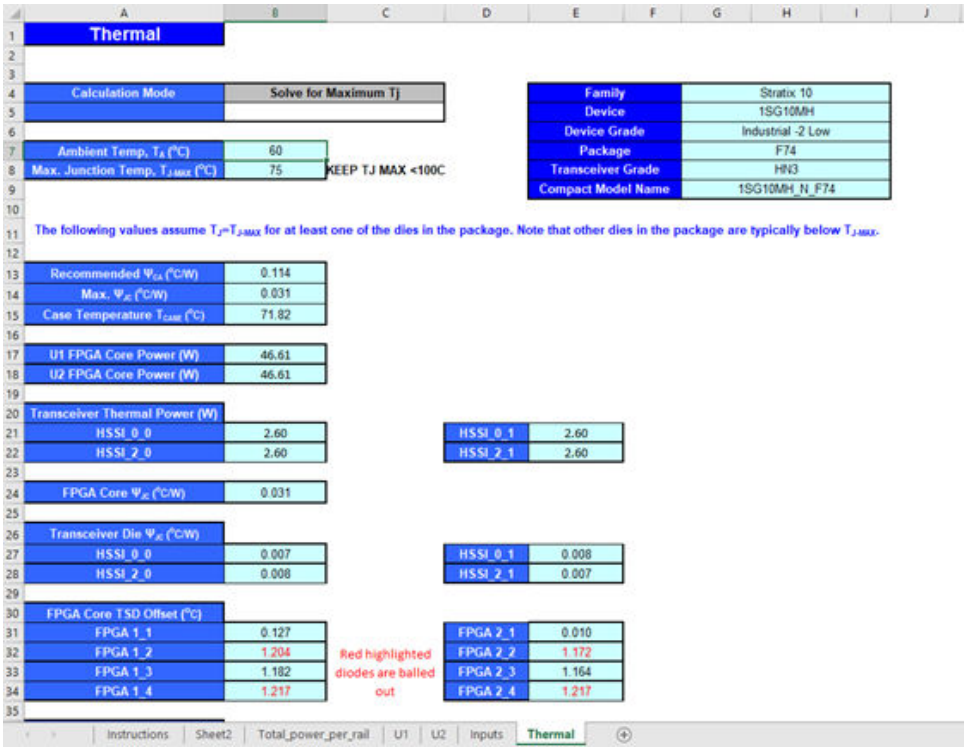
3

Mark 1 if channel is used
Leave blank if channel is unused

U1		U2		
HSSI 0_0	HSSI2_0	HSSI 0_1	HSSI 2_1	EPE CH
1	1	1	1	11
1	1	1	1	10
1	1	1	1	9
1	1	1	1	8
1	1		1	7
1	1		1	6
1	1		1	5
1	1		1	4
1	1	1	1	3
1	1	1	1	2
1	1	1	1	1
1	1	1	1	0

The **Thermal** worksheet shows the summary for Ψ values and TSD offset values.

Figure 10. Thermal Worksheet



3. Intel FPGA Power and Thermal Calculator Graphical User Interface

The Intel FPGA Power and Thermal Calculator (PTC) includes a GUI that allows you to enter information about your design, and view the resulting power and thermal calculations. The following section describes the Intel FPGA PTC GUI in detail.

3.1. Intel FPGA PTC Select Family Dialog Box

When you launch the Intel FPGA Power and Thermal Calculator (PTC) standalone, or without an open Quartus Prime project, the **Select Family** dialog box appears automatically to allow you to select the Intel FPGA family for your Intel FPGA PTC calculations.

When you launch the Intel FPGA PTC embedded version with an open Quartus Prime project, the Intel FPGA PTC obtains the device information from the project. Alternatively, you can turn on **Open an existing PTC file** in this dialog box to load the power data for a previously saved design hierarchy.

Figure 11. Select Family Dialog Box

Select the desired device family, and click **OK**.

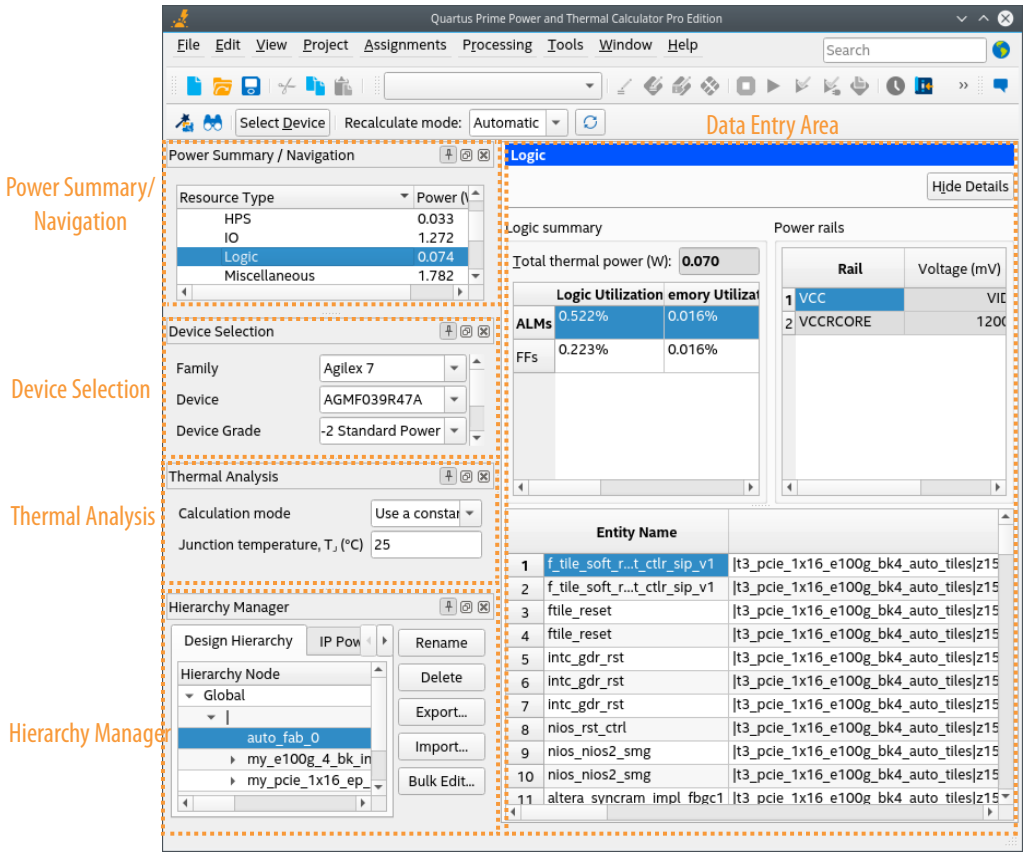
Note:

- Once you select a device family to model, you cannot change that selection unless you start a new Intel FPGA PTC instance.
- Currently, the Intel FPGA PTC supports the Agilex 5, Agilex 7 and Stratix 10 FPGA device families. The Intel FPGA PTC pages have some differences, depending on the device family you select.

3.2. Intel FPGA PTC Primary GUI Components

The Intel FPGA Power and Thermal Calculator (PTC) GUI is divided into the following major areas for entering power data about your design and viewing Intel FPGA PTC results.

Figure 12. Intel FPGA PTC Graphical User Interface (GUI)



Power Summary/Navigation

The **Power Summary/Navigation** window allows you to choose the current data entry page and shows the calculated power consumption of various types of resources, based on the current values that you specify in the data entry pages. You cannot directly edit the **Power Summary/Navigation** window.

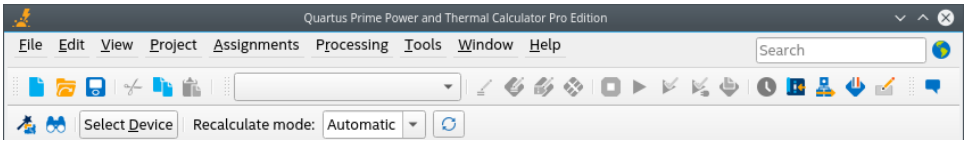
Device Selection and Thermal Analysis Windows

The **Device Selection** and **Thermal Analysis** windows summarize device characteristics and presumed thermal operating conditions, respectively. This information is also available on the **Main** and **Thermal** data entry pages.

Not all dockable windows may be visible by default. You can change which of the dockable windows are visible using the **View** menu.

Additionally, you can click the **Device Select** button on the PTC menu to view the **Device Selection** window and modify your device selection.

Figure 13. Device Selection Option on the PTC Menu

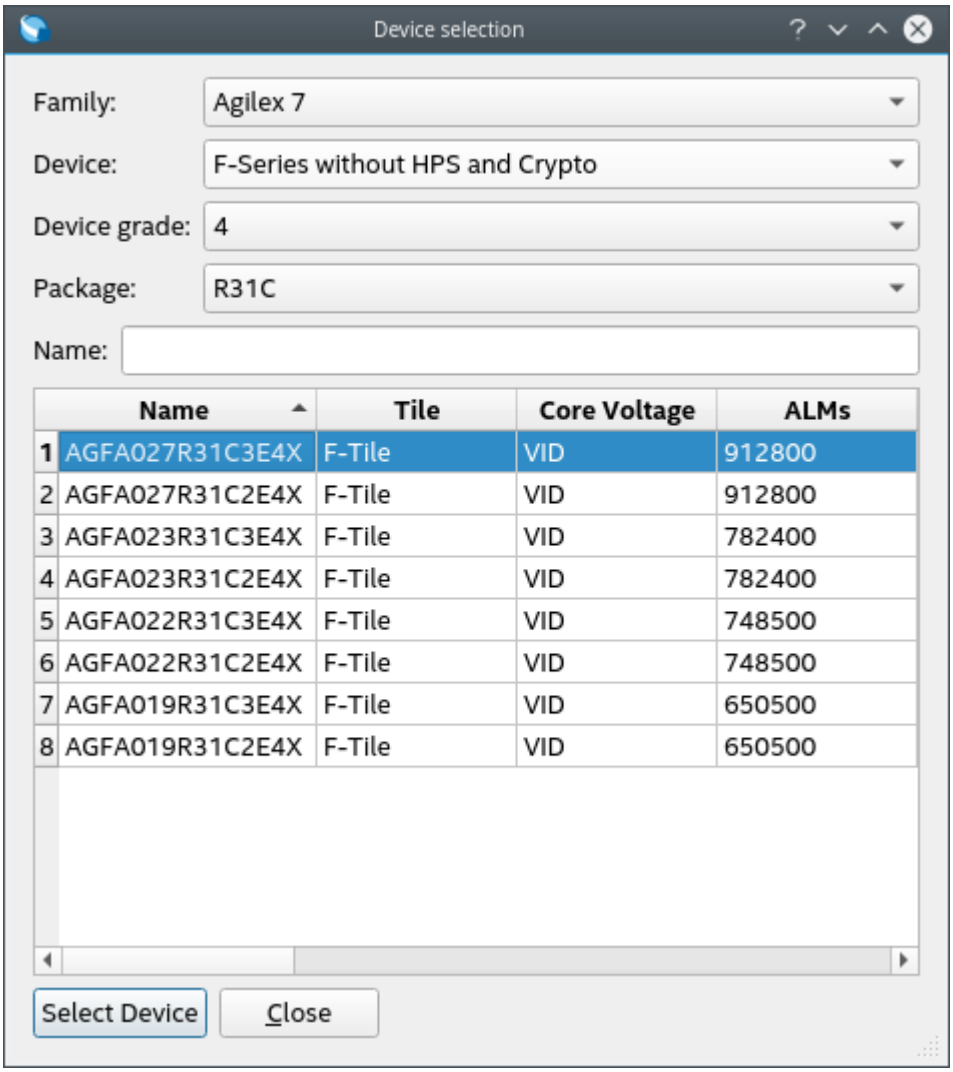


In the **Device Selection** dialog, you can select a device in the following ways:

- Use the drop-down options to filter the table.
- Directly select the desired device from the table.
- Type the partial name of the device in the **Name** field.

Upon clicking the **Select Device** button, PTC updates to use the selected device specifications.

Figure 14. Device Selection Window



Design Hierarchy

The **Design Hierarchy** tab in the **Hierarchy Manager** displays the hierarchy of the design as you enter it in the Intel FPGA PTC data entry pages. The **Design Hierarchy** allows you to enter and modify hierarchy names, import and export hierarchies, and delete unneeded hierarchy levels.

IP Power Summary

The **IP Power Summary** tab in the **Hierarchy Manager** displays each IP instance along with its power in the PTC design. You can edit each IP instance and replace it with the reinstantiated IP using the IP Wizard.

Data Entry Area

You enter values for the parameters that impact power calculation in the data entry area. The data entry area displays a named GUI page that corresponds to the various device architecture features included in the Intel FPGA PTC power model.

3.2.1. Intel FPGA PTC Data Entry Pages

On the data entry pages you enter information about your design that informs the power estimation calculations. The Intel FPGA Power and Thermal Calculator (PTC) uses the values that you specify on the data entry pages to calculate the power consumption and other data.

There are differences in the data entry page contents, depending on whether you are targeting an Agilex FPGA portfolio device or an Stratix 10 device.

The following data entry pages are available in the Intel FPGA PTC:

Table 6. PTC Data Entry Pages

PTC Data Page	Description
Main	Allows you to specify device, package, and cooling information, and displays thermal analysis information pertaining to constant junction temperatures.
Logic	Allows you to specify the properties of logic resources for all entities in your design.
RAM	Allows you to specify the properties of design entities implemented in RAM blocks. Specify the RAM type, data width, RAM depth (if applicable), RAM mode, and port parameters for these entities in your design.
DSP	Allows you to specify the properties of DSP design entities. Specify the DSP configuration, clock frequency, toggle percentage, and register usage for the DSPs in your design.
Clock	Allows you to specify the properties of the clock networks of separate clock domains in your design. Specify the clock domain name, clock frequency, total fan-out, and other properties about the clocks in your design.
PLL	Allows you to specify the properties of one or more PLLs in your design.
I/O	Allows you to specify the properties of design entities using general-purpose I/O pins. This page does not apply to transceiver I/O pins. Specify I/O standard, input termination, current strength or output termination, data rate, clock frequency, output enable static probability, and capacitive load for the I/O in your design.
Transceiver	Allows you to specify the transceiver resources and their settings for your design entities.
HPS	Allows you to specify the properties of entities that include a hard processor system (HPS). Specify the HPS entity and full hierarchy name, the voltage, CPU frequency, CPU application, and number of CPU cores.

continued...

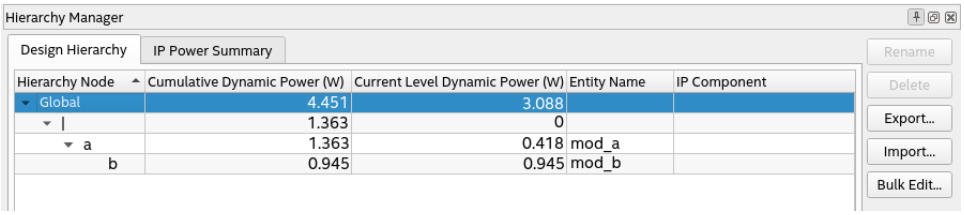
PTC Data Page	Description
Crypto	Allows you to specify the properties of crypto resources and their settings for all entities in your design, such as the entity name, full hierarchy name, and number of instances. (Agilex FPGA portfolio devices with crypto blocks only).
NOC	The dynamic power consumed by the network-on-chip system (NoC). (Agilex 7 M-Series devices only.)
HBM	Allows you to specify the properties of high-bandwidth memory (HBM) entities in your design. (Stratix 10 devices with HBM blocks only)
Thermal	Allows you to specify the temperature requirements for your design and displays thermal power and thermal analysis information.
Report	Reports the per-rail currents that the Intel FPGA Power and Thermal Calculator (PTC) calculates.

3.2.2. Intel FPGA PTC Design Hierarchy

The **Design Hierarchy** tab in the **Hierarchy Manager** displays the dynamic power consumption for each hierarchy of the design, as entered in the Intel FPGA Power and Thermal Calculator (PTC) data entry pages. It also lists the IP instances of your PTC design, and you can identify the instances using the **IP Components** column.

The **Design Hierarchy** allows you to enter and modify hierarchy names, import and export hierarchies, and delete unneeded hierarchy levels.

Figure 15. Intel FPGA PTC Design Hierarchy



The **Design Hierarchy** includes the following buttons and controls:

Table 7. Design Hierarchy Buttons and Controls

Button or Control	Description
Rename Button	Allows you to specify a new name for the currently selected design hierarchy.
Delete Button	Allows you to delete the currently selected design hierarchy.
Export Button	Allows you to export the currently selected hierarchy to a `.ptc` file. The exported `.ptc` can be imported into a higher level of the design, or shared with another designer. The `.ptc` includes all data relevant to the selected hierarchy and below. The exported `.ptc` file includes device selection settings, but does not include settings that are global to the design, such as thermal analysis settings. To save the complete design, including all global settings, use **File ➤ Save**.
Import Button	Allows you to import a previously generated Power and Thermal Calculator file, such as a `.ptc` file. The import appends the imported data to all existing sheets, as appropriate. To overwrite an existing design, use **File ➤ Open**. *Note:* If any imported global design settings conflict with the current design settings, the imported settings are ignored and an import warning message appears.

continued...

Button or Control	Description
Duplicate command (right-click)	Allows you to right-click a hierarchy and create a duplicate copy of the hierarchy.
Bulk Edit button	Allows you to modify parameters of a specific hierarchical level and below if selected. All pages of the Intel FPGA Power and Thermal Calculator reflect these changes. For additional information, refer to Bulk Editing Hierarchies in the Intel FPGA PTC on page 28.
Edit in IP Wizard	Displays the IP Wizard to select, configure, and instantiate IP blocks, which are appended to your current design. For additional information about how to use the IP Wizard, refer to Intel FPGA PTC - IP Wizard on page 33.

3.2.2.1. Using Design Hierarchies in the Intel FPGA Power and Thermal Calculator

The Intel FPGA Power and Thermal Calculator (PTC) supports the hierarchical structure of your design RTL, allowing you to enter hierarchy information and report power data for each level of your design's hierarchy. This granularity of reporting allows you to make more targeted and effective improvements to power and thermal conditions.

In addition, the Intel FPGA PTC supports export and import of power results from PTC for a particular design hierarchy, allowing you to export and reuse the Intel FPGA PTC data in a higher level of the design, or to share the power data for import by other team members.

3.2.2.2. Entering Hierarchy Information Into the Intel FPGA PTC

If you want Intel FPGA Power and Thermal Calculator (PTC) estimation to reflect your design hierarchy, you must first enter (or import from a prior PTC session) your design's power data and hierarchy level information into the Intel FPGA PTC data entry pages. The Intel FPGA PTC then reports, in watts, the subtotals of the power consumed by each architectural feature, for each level of design hierarchy.

When entering levels of hierarchy in the Intel FPGA PTC, the pipe character (|) denotes a level of hierarchy. For example, the following notation indicates three levels of hierarchy. Hierarchy a is the highest level. Hierarchy b is the second level. Hierarchy c is the third level.

```
a|b|c
```

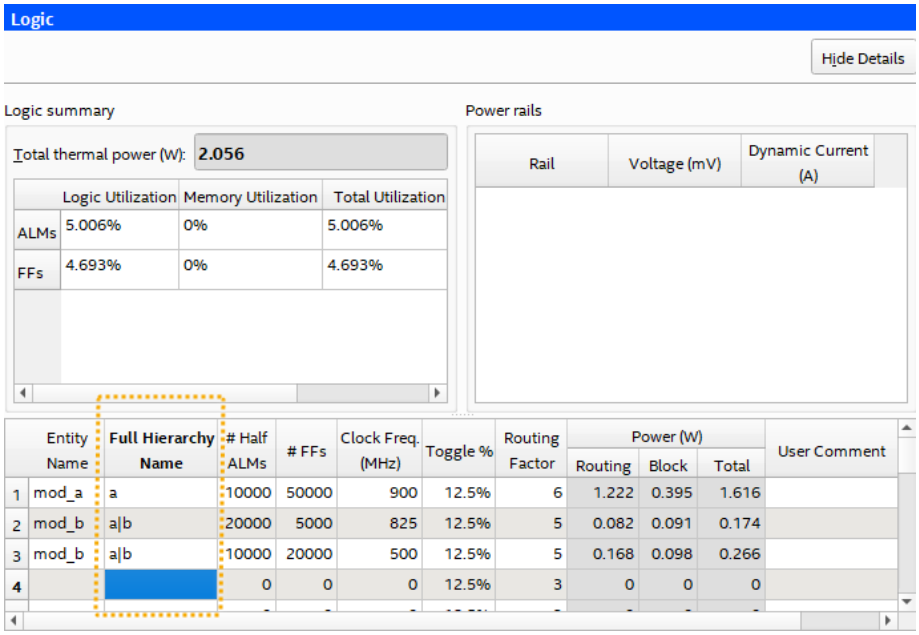
Instance paths may, optionally, begin with a leading pipe character (|). But regardless of whether a leading pipe is is there or not, paths are treated the same.

When you enter an entity name for a given hierarchy, the Intel FPGA PTC automatically updates the entity name in the **Design Hierarchy** tab of the Hierarchy Manager and on all data-entry pages that include that hierarchy.

To enter design hierarchy information into the Intel FPGA PTC, follow these steps:

1. Open your version of the Intel FPGA PTC, as Accessing the Intel FPGA Power and Thermal Calculators on page 5 describes.
2. Click the **View** menu and select one of the Intel FPGA PTC pages, such as the **Logic** page.

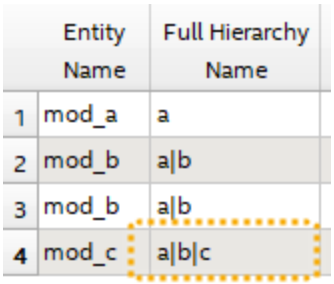
Figure 16. Intel FPGA PTC Logic Page



3. In the **Full Hierarchy Name** cell, type the hierarchical name of a hierarchy in your design, using the pipe character (|) as the hierarchy level delimiter. For example, the following defines the b level of hierarchy that is child of hierarchy a:

```
a|b
```

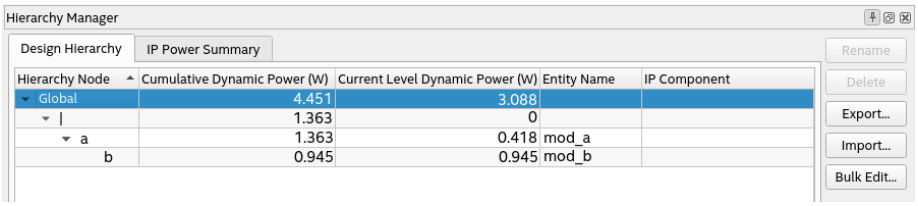
Figure 17. Entering Full Hierarchy Name in Intel FPGA PTC



4. In the **Entity Name** cell, enter the name of the design entity. If a newly entered hierarchy name already exists in the design, the **Entity Name** cell is already populated. Also, changing the entity name for a particular hierarchy name changes it for all_occurrences of that hierarchy name.
5. Specify values for the **#Half ALMs**, **#FF**s, **Clock Freq.** (MHz), **Toggle %** and **Routing Factor** cells for each hierarchy. Repeat appropriate entries for design hierarchies on other pages.

   The instance appears hierarchically in the **Design Hierarchy** in the Intel FPGA PTC, showing the dynamic power estimate for each hierarchy level, and the cumulative power for all instances and hierarchy levels.

Figure 18. Intel FPGA PTC Design Hierarchy



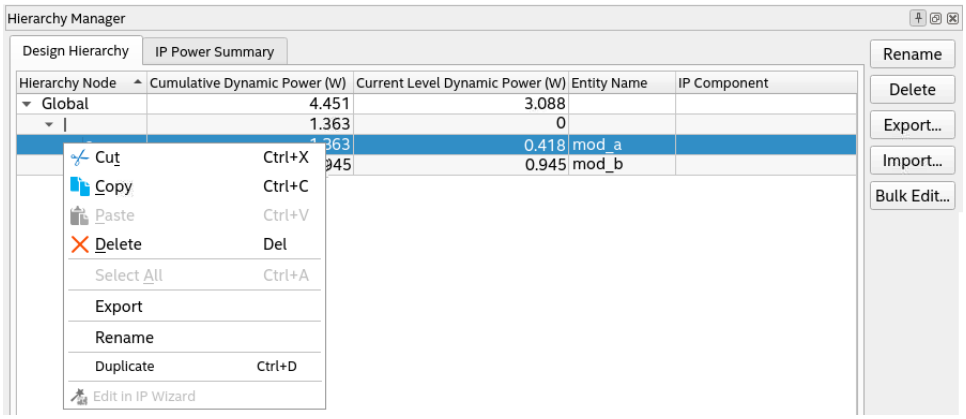
6. In the **Design Hierarchy**, you can right-click any instance to **Rename**, **Duplicate**, or **Export** the Intel FPGA PTC data for the levels of hierarchy that you define.

3.2.2.3. Exporting, Importing, Duplicating, Renaming, and Deleting Hierarchies in the Intel FPGA PTC

To export, import, duplicate, rename, and delete design hierarchies in the Intel FPGA Power and Thermal Calculator (PTC) using the **Hierarchy Manager**, follow these steps:

1. Click **View ➤ Hierarchy Manager** to display the **Hierarchy Manager** if not already displayed.
2. For any hierarchy in **Design Hierarchy** tab of the **Hierarchy Manager**, perform any of the following:
   - To duplicate a hierarchy, right-click the hierarchy and select **Duplicate**.
   - To export the hierarchy data to a `.ptc` file, select a hierarchy and click the **Export** button. Exporting a hierarchy does not export complete design data, only the selected hierarchy and a minimum set of device-selection fields to allow the exported instance to be opened properly on its own in the PTC.
   - To import hierarchy data from a `.ptc` file, click the **Import** button. Importing prepends the imported file name to any imported instance paths.
   - To rename a hierarchy, click the **Rename** button. The new hierarchy name can include the pipe character (|) to create new levels of hierarchy.
   - To delete a selected hierarchy, click the **Delete** button. Delete operations cannot be undone, so the PTC prompts you to confirm the delete operation.
   - You can also modify the design hierarchy using the **Cut**, **Copy**, and **Paste** commands in the Hierarchy Manager.

Figure 20. Hierarchy Manager Controls



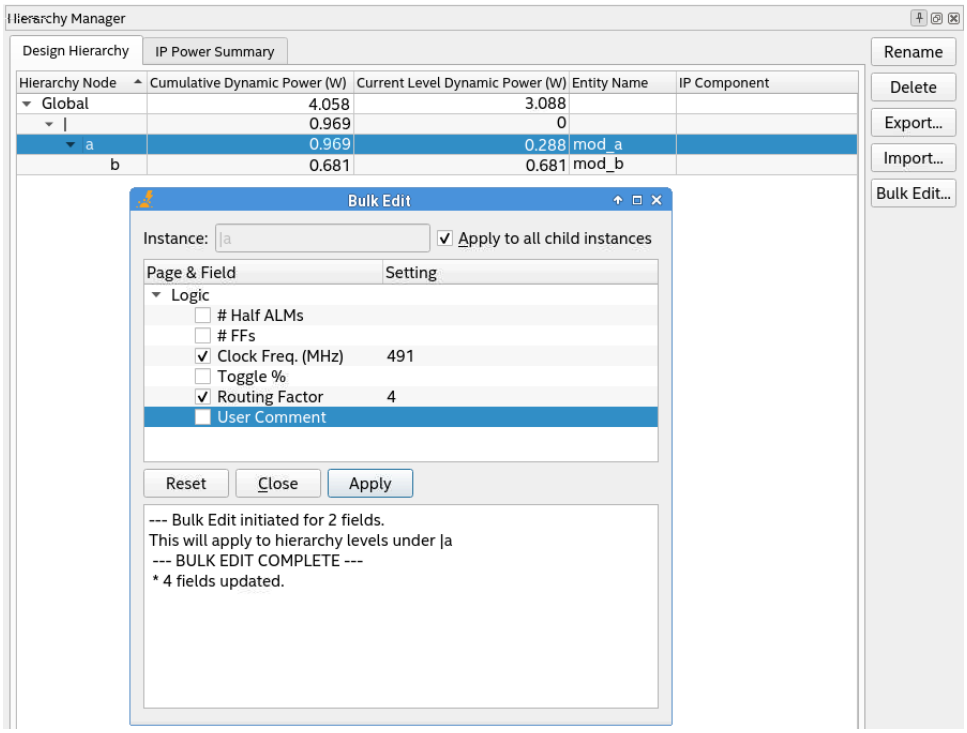
3.2.2.4. Bulk Editing Hierarchies in the Intel FPGA PTC

The **Bulk Edit** button in the **Hierarchy Manager** allows you to modify parameters of a specific hierarchical level and below if selected. All pages of the Intel FPGA Power and Thermal Calculator reflect these changes.

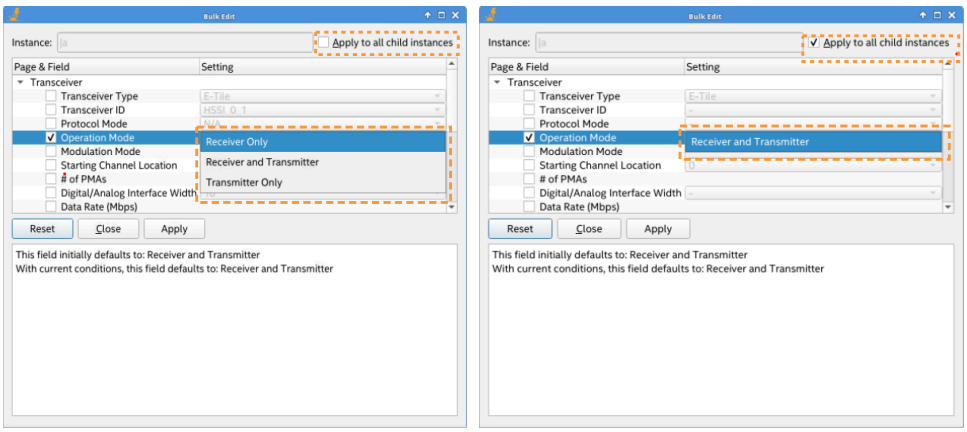
Follow these steps to perform bulk edits:

1. Select the desired hierarchy level in the **Design Hierarchy** tab.
2. Click **Bulk Edit** to view the Bulk Edit dialog.
3. Select **Apply to all child instances** checkbox if you want to apply changes to the currently selected hierarchical level and its children below.
4. Select the desired entries under the **Page & Field** column that you want to modify.
5. Double-click the corresponding field in the **Setting** column and enter the desired value.
6. Click **Apply** to apply the changes.

Figure 21. Bulk Editing in the Hierarchy Manager



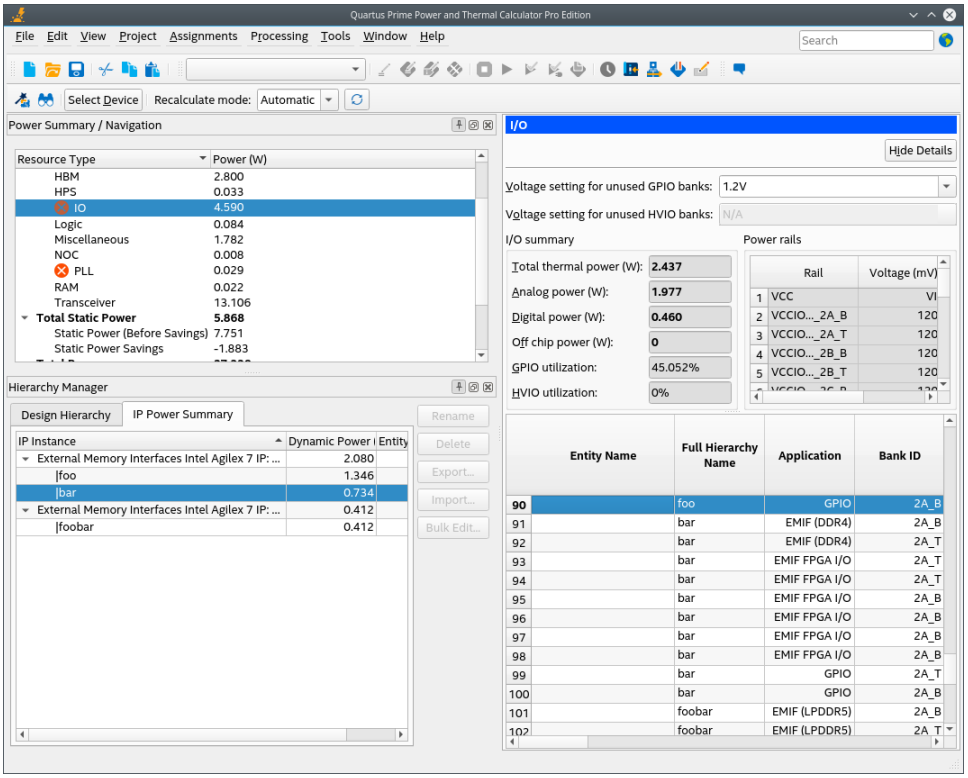
Note: When you click **Bulk Edit** and check **Apply to all child instances**, the drop-down fields show values that apply to both parent and child rows commonly. This means that values that apply only to the parent level or child-levels stay hidden. Consider the following examples:



3.2.3. Intel FPGA PTC IP Power Summary

The **IP Power Summary** tab in the **Hierarchy Manager** displays all IP instances created using the IP Wizard, along with the dynamic power of the instances. The tab is implemented as a floatable and dockable widget and you can control its visibility through PTC's **View** menu. In the **IP Power Summary** tab, you can edit and replace each IP instance with the reinstantiated IP using the IP Wizard.

Figure 22. Intel FPGA PTC IP Power Summary Tab



Editing an IP Instance

To edit an IP instance, right-click on it and select **Edit in IP Wizard**. The IP Wizard displays with the previously selected values. You can modify the existing values in the IP Wizard, click **Next** and **OK**, the new configurations are added to the IP Power Summary tab and all related resource pages.

Renaming or Deleting an IP Instance

To rename or delete an instance, switch to the **Design Hierarchy** tab and click either **Rename** or **Delete** button, respectively. You can also find these options on the context-sensitive menu. You can also right-click and edit an IP instance through the Design Hierarchy tab using the context-sensitive menu.

Once you rename or delete an IP instance, it reflects in all related resource pages and the IP Power Summary tab.

Note: PTC does not allow renaming or deleting arbitrary rows of IP instances in the resource pages or in the IP Power Summary tab since they all belong to an IP.

3.2.4. Intel FPGA PTC Field Types

The Intel FPGA Power and Thermal Calculator (PTC) data entry pages include input fields that allow you to specify the properties of your design that impact power estimation.

The shading of the editable input fields alternates between white and light gray. Double-click in the field and select a value from the list or type the value.

Figure 23. Intel FPGA PTC Data Entry Page Field Types

	Entity Name	Full Hierarchy Name	# Half ALMs	# FFs	Clock Freq. (MHz)	Toggle %	Routing Factor	Power (W)		
								Routing	Block	Total
1	mod_a	a	10000	50000	900	12.5%	6	1.222	0.395	1.616
2	mod_b	a|b	20000	5000	825	12.5%	5	0.082	0.091	0.174
3	mod_b	a|b	10000	20000	500	12.5%	5	0.168	0.098	0.266
4			0	0	0	12.5%	3	0	0	0

Input Fields (Editable)

Output Fields (Not Editable)

The output fields in the data entry pages report calculated values, and appear in darker gray. Fixed input fields, and fields that are not applicable have dimmed text.

3.2.4.1. Intel FPGA PTC Input Field Dependencies

The value you specify for some input fields affect the allowed values for other fields.

Specified Values Affect the Allowed Values

For example, the device package that you select may determine what transceiver grades are selectable. If you change the selected device package, and the currently selected transceiver grade is still legal for the new package, the **Transceiver Grade** value does not change. However, if the currently selected transceiver grade is not compatible with the selected device package, the **Transceiver Grade** value automatically changes to one of the legal values.

Hierarchy Changes To One Data Entry Page Affect All Pages

Adding, changing, or deleting hierarchy information on one data entry page is reflected on all other pages that contain that same level of hierarchy. For example, if the **Logic** page contains hierarchical entry of a|b|c, updating the **Module** field results in module name update of all data entry pages that contain the hierarchy of a|b|c. In addition, the **Design Hierarchy** tab of the **Hierarchy Manager** updates with this new information.

Similarly, deletion of a level of hierarchy in the **Hierarchy Manager** results in removal of all entries on all data entry pages with that same level of hierarchy and below.

Changes To One Data Entry Page May Affect Values On Other Pages

Changes that you make on one data entry page may affect values on another page because of dependencies between input fields. For example, if you select a device that does not support the current I/O standard specified in the I/O page, that I/O standard automatically changes to one of the I/O standards supported by the new device.

In general, the Intel FPGA Power and Thermal Calculator (PTC) does not automatically change an input value unless it is necessary to preserve the legality of the input. Changes in one field have minimal impact on other fields, while ensuring that overall combination of field values are legal. However, this can sometimes lead to unanticipated results. Consider the following example:

Assume that **Dev1** is selected in the Main page, and I/O standard **IO1** is selected in the I/O page. Assume also that device **Dev1** supports I/O standards **IO1** and **IO2**. Suppose that you change the device selection to **Dev2**, which supports only one I/O standard, **IO2**. As a result of you changing the device selection, the I/O standard in the I/O page changes to **IO2**. If you then reverted the device selection back to **Dev1**, the I/O standard does not change, because **IO2** is a legal I/O standard value for the device **Dev1**. The important point to note, is that the changing of device from **Dev1** to **Dev2** and back again, had the—potentially unintended—consequence of changing the I/O standard in the I/O page.

Note: In most cases, field dependencies are limited to the same page, and often even within the same row. However, device, device grade, package and transceiver grade selection can have a much wider impact, as illustrated above. A simple way to verify that no unintended changes resulted from changing a device is to use the **File ➤ Save As** function to export the Intel FPGA PTC state before and after the change in device selection. You can then compare the two `.ptc` files using a third-party *diff* utility to identify any fields that have changed.

3.2.5. Intel FPGA PTC Data Entry Error Messages

If you enter an invalid value in the data entry fields, the Intel FPGA Power and Thermal Calculator (PTC) displays an error message. The message may indicate the conditions under which a value is invalid, or specify a valid range of values.

Error Message Type: Invalid Value

If you enter an invalid value, such as a temperature value that is outside the allowed range for a selected family, device, transceiver grade, device grade and package combination, an error message appears, indicating that the entered value is invalid and stating the allowed range of values. Click **OK** to dismiss the error message, and the field reverts to its previous value.

Error Message Type: Incorrect Format

Some fields require a specific type of data. If the data you enter is not of the type required, an error message appears. For example, if an integer value is expected and you enter a fractional value, the resulting error message indicates that the entered value cannot be converted to a valid value for the input field. After you click **OK**, the field reverts to its previous value.

Similarly, if a numerical value is expected and you enter a text value, the resulting error message indicates that the entered value cannot be converted to a valid value for the input field. After you click **OK**, the field reverts to its previous value.

3.3. Intel FPGA PTC - IP Wizard

The **IP Wizard** of the Intel FPGA Power and Thermal Calculator (PTC) allows you to select, configure, and instantiate IP blocks which are then appended to your current design.

1. You can launch the IP Wizard from the PTC File menu, by clicking **File ➤ IP Wizard** or clicking the IP wizard button on the toolbar.

Figure 24. Launching the IP Wizard

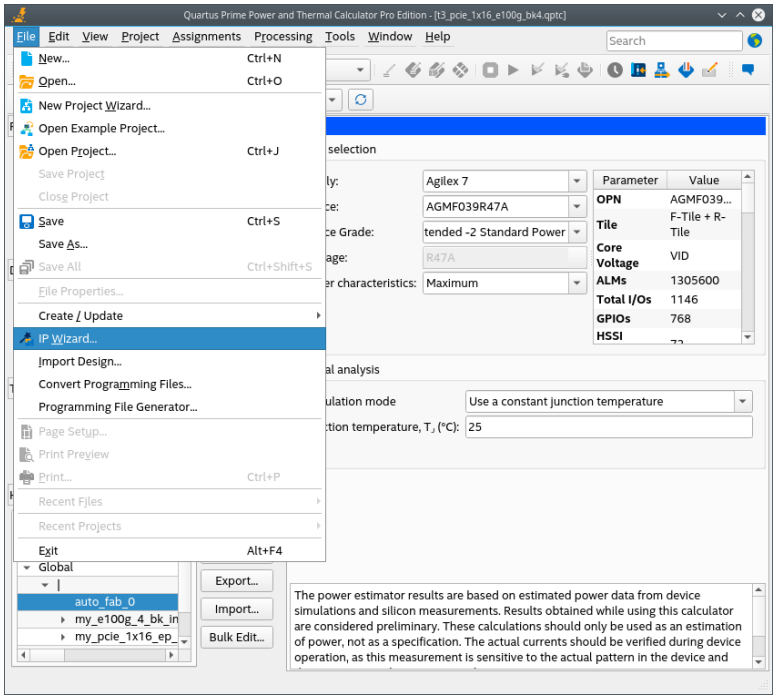
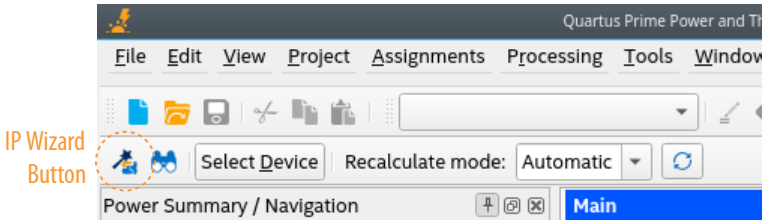


Figure 25. Launching the IP Wizard with button



2. The opening dialog box of the IP Wizard prompts you to select an IP from a pulldown list. Select the IP that you want to add to your design, and click **Next**.
3. The IP Wizard then displays a dialog box for configuring your selected IP. Enter the appropriate information, and click **Next**.

Figure 27. IP Configuration Page

The IP Parameter Configuration page parameters depend on the IP you select. These parameters are a subset of the parameters in IP Catalog wizards. Refer to the appropriate IP User Guide for more details on each IP's parameters.

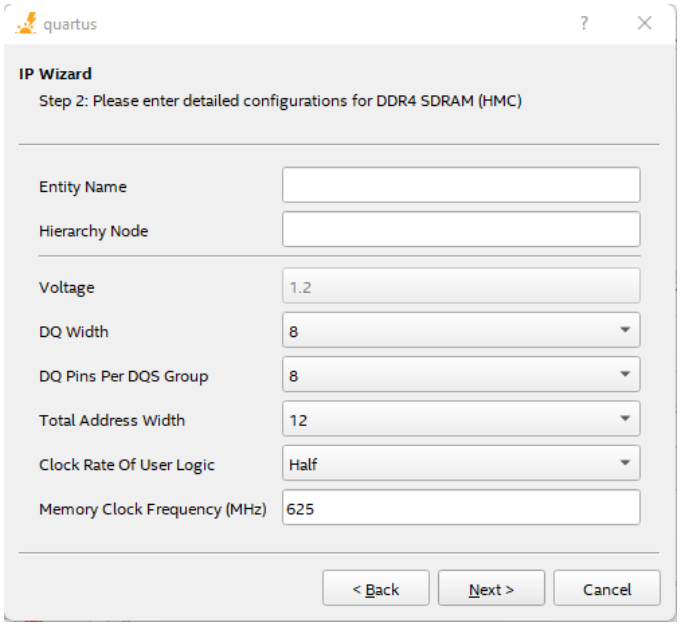


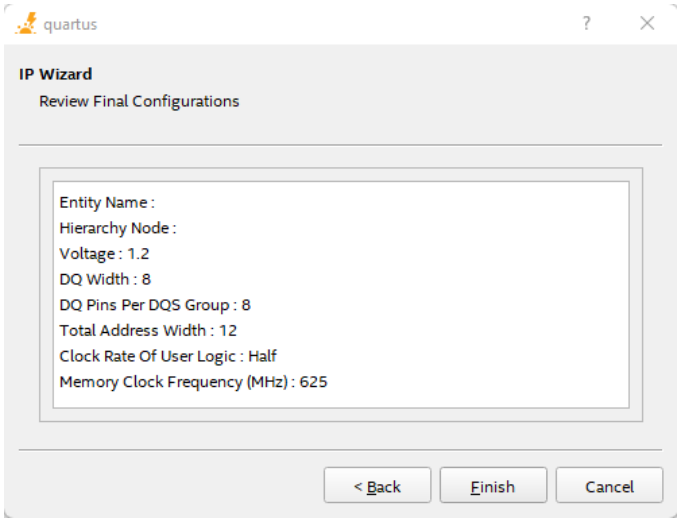
Table 8. IP Configuration Fields

This table is only relevant for EMIF IPs in Intel Stratix 10 devices. .

Column Heading	Description
Entity Name	Specify a name for the entity.
Hierarchy Node	(Mandatory field) Specifies the name of the IP instance.
Voltage	Specifies the I/O voltage of the signaling between periphery device and interface.
Data Width (Bits)	Specifies the interface data width of the specific IP (in bits).
Data Group Width	Specifies the data group width.
Memory Device(s)	Specifies the number of memory devices connected to the interface.
Total Address Width	Specifies the total address width. This value is used to derive the total number of address pins required.
DDR Rate	Specifies the clock rate of user logic. Determines the clock frequency of user logic in relation to the memory clock frequency. For example, if the memory clock sent from the FPGA to the memory device is toggling at 800MHz, a "Quarter rate" interface means that the user logic in the FPGA runs at 200MHz.
PHY Rate	Specifies the clock rate of PHY logic. Determines the clock frequency of PHY logic in relation to the memory clock frequency. For example, if the memory clock sent from the FPGA to the memory device is toggling at 800MHz, a "Quarter rate" interface means that the PHY logic in the FPGA runs at 200MHz.
Memory Clock Frequency (MHz)	Specifies the frequency of memory clock (in MHz).

4. The IP Wizard then displays the configuration details for your review. If you want to change any of the configuration, click **Back**. Otherwise, if you are satisfied with the configuration, click **Finish**.

Figure 28. IP Configuration Review Page



After you exit the IP Wizard, the system appends new rows to the PTC pages (Logic, PLL, I/O, etc.), in accordance with the IP that you have added.

3.4. Intel FPGA PTC Searchable Drop-Down Lists

Starting with the 23.3 release, PTC now supports using partial or full-text string search on all drop-down lists, in all GUI components, including the resource pages.

The following images show examples of searching with a partial string where the drop-down list gets refined and displays a subset of values matching the string:

Figure 29. Example 1: Refining the Device Drop-Down List

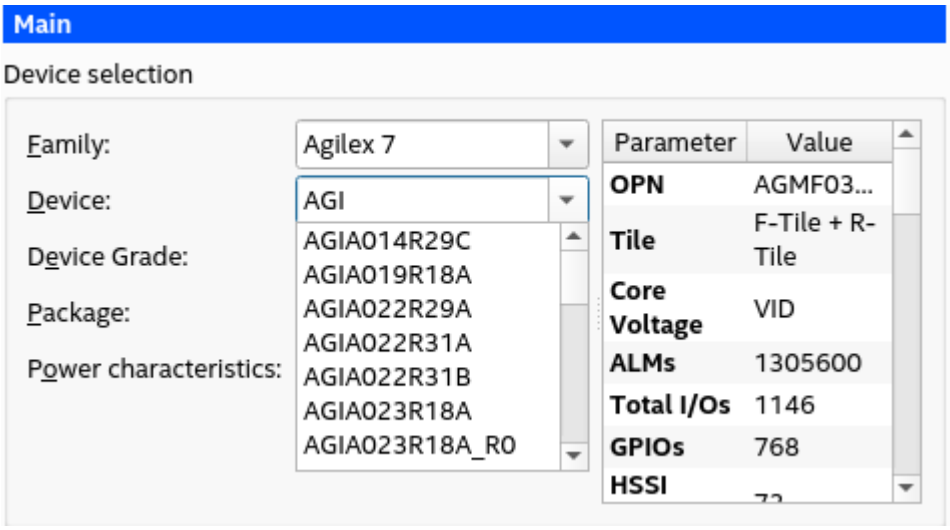
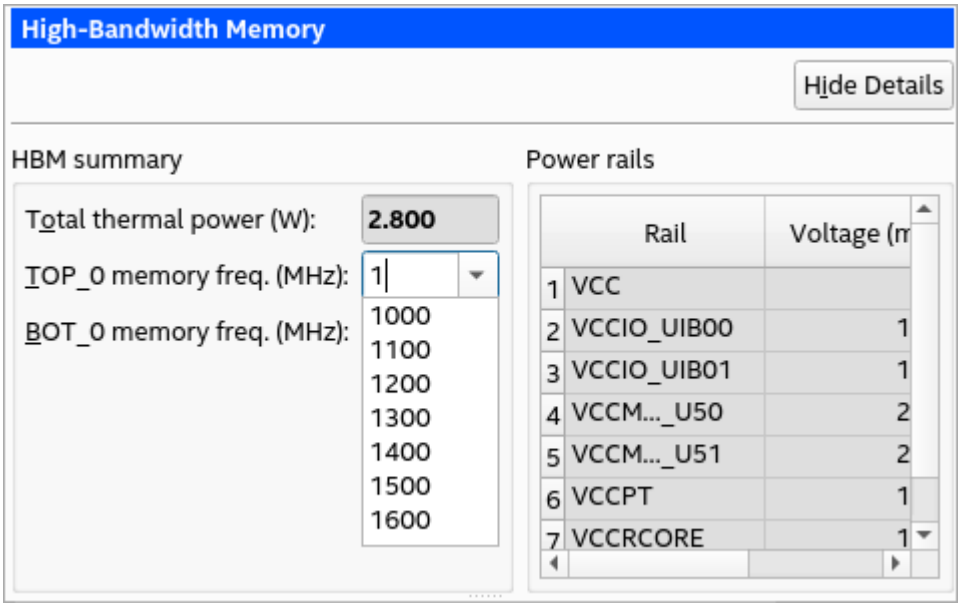


Figure 30. Example 2: Refining the Memory Frequency Drop-down List

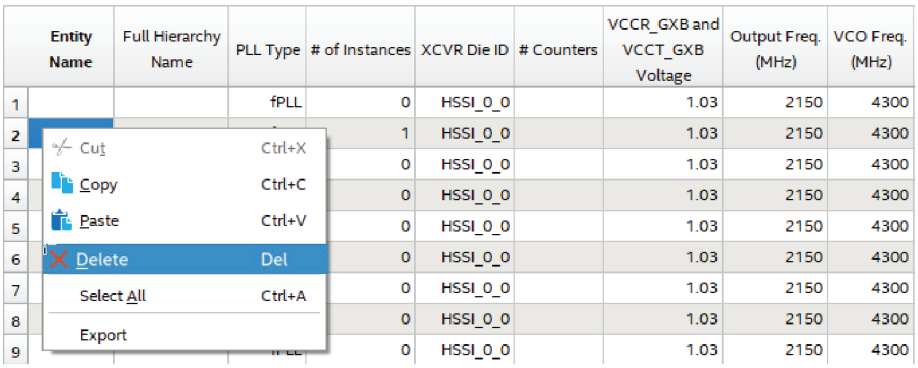


3.5. Deleting Rows from Data Entry Pages

Follow these steps to select and delete a single row, or a contiguous series of two or more rows, from any of the Intel FPGA Power and Thermal Calculator (PTC) data entry pages.

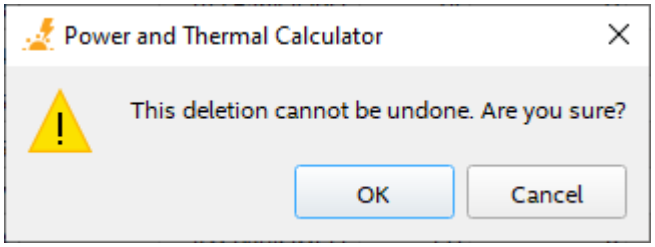
1. To select a row to delete, click on the row number at the left side of the table row. The entire row becomes highlighted. (If you want to delete multiple contiguous rows, hold down the **Ctrl** key while you select additional rows.)
2. To delete the selected row (or rows), right-click and select **Delete** from the context menu, or press the **Delete** key on the keyboard.

Figure 31. Deleting a Row



3. The system displays a dialog box warning that the deletion cannot be undone, and asking you to confirm that you want to proceed with the deletion. Click **OK** to delete the selected rows, or click **Cancel** to abandon the operation.

Figure 32. Confirming a Deletion



Note: When you delete one or more rows from a table, the remaining rows are automatically renumbered accordingly.

3.6. Finding Resources Using the Find Dialog Box

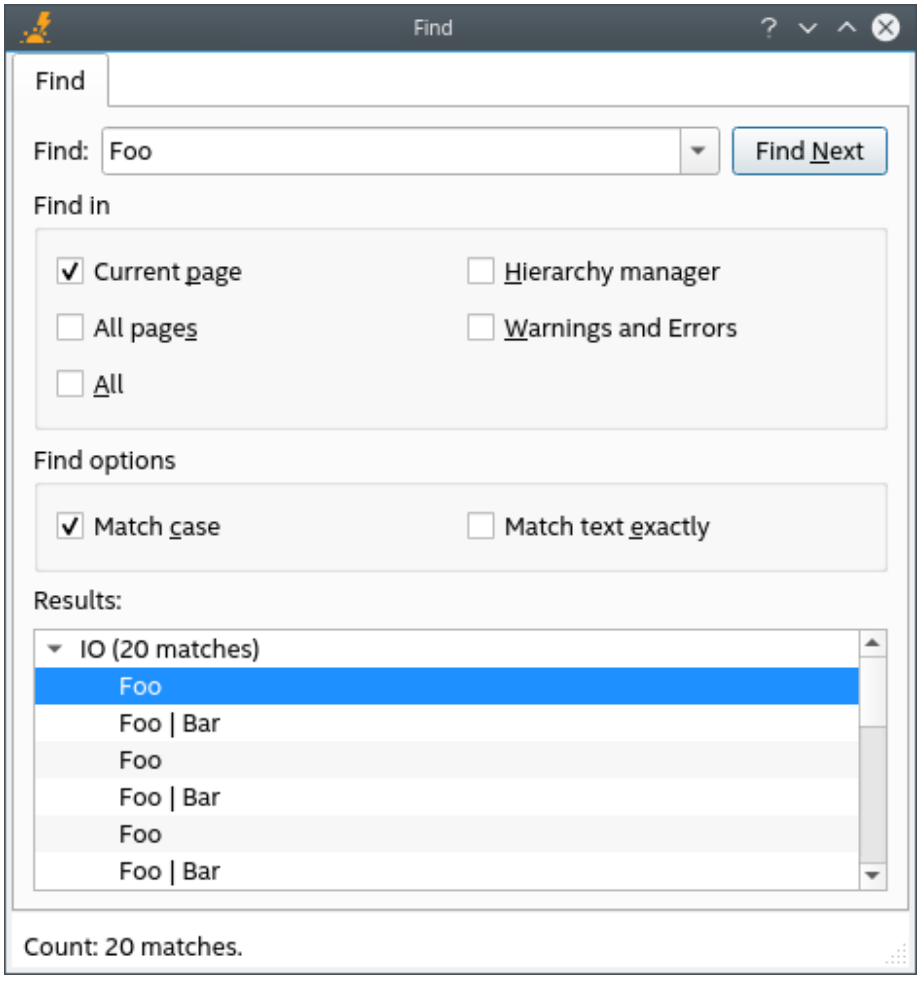
To find your resources in PTC, press the CTRL+F keys on your keyboard to launch the **Find** dialog box. You can also launch this dialog box by clicking on the PTC menu bar or through PTC's **Edit ➤ Find** menu.

The **Find** dialog box supports the following functionalities:

- By default (without selecting any checkbox), you can start searching with partial or full-text keywords for the resource page you are currently viewing and view all resources matching that keyword on the page.

  In the following example, all resources matching the keyword "foo" on the IO resource page are listed:

Figure 33. Find Dialog Box in PTC



- You can use the following checkboxes to broaden or refine your search further:
  - **Find in all pages**: Allows you to search resources on all PTC resource pages.
  - **Match case**: Performs full-text or partial text search with upper or lower case keywords, and the results match the case.
  - **Match text exactly**: Performs a full-text search, and the results match the text exactly.
- Selecting any row of the search result displays and highlights the location of that resource within PTC.
- You can use the scrollbar or Down key on the keyboard to navigate through the search results.
- You can search your design hierarchy by entering your target node's instance path or partial instance path (for example, P|Q node) to locate all rows that are associated with that instance. This is useful in navigating your large design hierarchies.

Figure 34. Instance Path Search

4. Intel FPGA Power and Thermal Calculator Pages

The Intel FPGA Power and Thermal Calculator (PTC) allows you to enter information about your design onto data entry pages named according to potential architectural features in your design. The Intel FPGA PTC then reports, in watts, subtotals of the power consumed by each architectural feature. For more information about each architectural feature refer to the respective page descriptions.

Note: The Intel FPGA PTC supports the Agilex 5, Agilex 7 and Stratix 10 FPGA device families. There are some differences on the Intel FPGA PTC data entry pages, depending on the device family selected.

For information on each Intel FPGA PTC data entry page, refer to the respective topic, below.

4.1. Intel FPGA PTC - Power Summary/Navigation

The **Power Summary/Navigation** tile of the Intel FPGA Power and Thermal Calculator (PTC) displays at all times, and shows the calculated power consumption by resource type.

The values displayed in the **Power Summary/Navigation** update in real time as you change parameters on the data entry pages.

In addition to displaying total power consumption, the **Power Summary/Navigation** displays power consumption for the resource types listed in the following table.

Table 9. Resource Types Displayed in the Power Summary/Navigation

Agilex FPGA Portfolio PTC Power Summary/Navigation	
Resource Type	**Description**
Logic	The dynamic power consumed by adaptive logic modules (ALMs), flipflops (FFs) and routing fabric. *Note:* All routing fabric, including from resources other than logic resources is included here.
RAM	The dynamic power consumed by specialized blocks optimized for data storage and retrieval.
DSP	The dynamic power consumed by specialized blocks optimized for fast math operations.
Clock	The dynamic power consumed by clock networks. The clock dynamic power is affected by the selected device.
PLL	The dynamic power consumed by phase-locked loops (PLLs).
I/O	The dynamic power consumed by I/O pins and I/O subsystems.
Transceiver	The dynamic power consumed by transceiver blocks.
HPS	The dynamic power consumed by the hard processor system (HPS).
Crypto	The dynamic power consumed by the crypto blocks utilized by the design.
NOC	The dynamic power consumed by the network-on-chip (NoC) IP. (This resource type applies only to Agilex 7 M-Series devices.)
HBM	The dynamic power consumed by high-bandwidth memory (HBM) and the universal interface bus (UIB) modules.
Static Power	The power that the configured device consumes when powered up but with no user clocks operating. The static power (P_{STATIC}) is the power dissipated on the chip, independent of design activity. P_{STATIC} includes the static power from all FPGA functional blocks. P_{STATIC} varies with junction temperature and power characteristics (process). P_{STATIC} is also the only power component that varies significantly with selected device.
Static Power Savings	The package static power savings that occur in standard operation mode. Includes the static power reduction that occurs when not all power rails are at their maximum simultaneously.
SmartVID Power Savings	The total power reduction (static and dynamic) resulting from the lower voltage that is made possible by SmartVID. This power reduction is dependent on the user design and device characteristics. The combination of these factors may result in different static and dynamic power savings, so the exact dynamic and static components are not identified separately, and the power reduction reported here is a worst-case result. The reduction reported in this field is already taken into consideration in the Total Power (W) field. The SmartVID Power Savings field applies only to devices that support SmartVID and only when Power Characteristics is set to Maximum.

continued...

Total Power	The total power dissipated as heat from the FPGA. Does not include power dissipated in off-chip termination resistors. Total power dissipation in the FPGA may differ from the sum of power on all rails due to several factors including, but not limited to, power dissipated in off-chip termination resistors.

Note: For Agilex FPGA portfolio devices, power reported in a given row of the **Power Summary/Navigation** may not always match the total power reported on the corresponding Intel FPGA PTC data entry page.

Individual Intel FPGA PTC data entry pages report the total power of resources entered on that page, regardless of the power category to which such power belongs. However, each row of the **Power Summary/Navigation** reports power for *all* pages that contribute power to that category—in addition to any idle power in that category. (Some circuitry on the chip consumes idle power even when the circuitry is unused.)

For example, when implementing an MLAB RAM type on the **RAM** page, the total power reported on the **RAM** page includes the power consumed by the memory itself, the power consumed by any additional registers required to implement the memory, as well as any routing power associated with the memory.

On the other hand, the **Power Summary/Navigation** reports the following (assuming all other pages are empty):

- Under the **RAM** category, power from the RAM page that is due to the memory itself, plus any idle power of all different RAM types in the device.
- Under the **Logic** category, power from the RAM page that is due to registers and routing, plus any idle power of all the ALMs, registers and routing in the device.

Stratix 10 PTC Power Summary/Navigation

Resource Type	Description
Logic	The dynamic power consumed by adaptive logic modules (ALMs), flipflops (FFs) and associated routing.
RAM	The dynamic power consumed by RAMs and associated routing.
DSP	The dynamic power consumed by digital signal processing (DSP) blocks and associated routing.
Clock	The dynamic power consumed by clock networks. The clock dynamic power is affected by the selected device.
PLL	The dynamic and standby power consumed by phase-locked loops (PLLs).
I/O	The dynamic and standby power consumed by I/O pins and I/O subsystems.
Transceiver	The dynamic and standby power consumed by transceiver blocks.
Hard Processor	The dynamic and standby power consumed by the hard processor system (HPS).
High-Bandwidth Memory	The dynamic power consumed by high-bandwidth memory (HBM) and the universal interface bus (UIB) modules.
Static Power	The static power consumed regardless of clock frequency. This includes static power consumed by I/O and transceiver blocks, but does not include standby power.
Total, Before SmartVID Savings	The total power consumption before SmartVID power savings. Includes static power (PSTATIC) and power consumed by different blocks as reported above. Does not include power dissipated in off-chip termination resistors.
SmartVID Savings	The total power reduction (static and dynamic) resulting from the lower voltage that is made possible by SmartVID. This power reduction is dependent on the user design and device characteristics. The combination of these factors may result in different static and dynamic power savings, so the exact dynamic and static components are not identified separately, and the power reduction reported here is a worst-case result. The reduction reported in this field is already taken into consideration in the Total (W) field. The SmartVID Power Savings field applies only to devices that support SmartVID and only when Power Characteristics is set to Maximum.
Total Power	The total power dissipated as heat from the FPGA. Does not include power dissipated in off-chip termination resistors. Total power dissipation in the FPGA may differ from the sum of power on all rails due to several factors including, but not limited to, power dissipated in off-chip termination resistors.

4.2. Intel FPGA PTC - Common Page Elements

The Intel FPGA Power and Thermal Calculator (PTC) is divided into multiple data entry pages, each allowing power data entry for a subset of FPGA resources. The following elements are common to more than one page.

Recalculate mode

The **Recalculate mode** pulldown is available at the top-left corner of the Intel FPGA PTC, regardless of which data entry page is open. The available settings are **Automatic** and **Manual** modes:

- **Automatic**—in **Automatic** mode, the system automatically recalculates all field values whenever you modify an input value. **Automatic** is the default mode.
- **Manual**—in **Manual** mode, output fields are left set to their last known value, as the system does not perform calculations or update the fields automatically. A warning message appears in the message list, and a 'Recalculation Needed' status bar appears beside the **Recalculate mode** pulldown. The status bar indicates that the results are outdated, and provides instructions on how to refresh the design's calculations. To recalculate, click the blue button to the right of the **Recalculate mode** pulldown, press the F9 keyboard key, or switch to **Automatic** mode.

Tip: In **Automatic** mode, the Intel FPGA PTC may appear to become unresponsive while recalculating. If you are making multiple changes, you may find it a better experience to select **Manual** mode, and recalculate only once, after you have entered all your changes.

Total Thermal Power

The Total thermal power field estimates the total thermal power consumed by all FPGA resources on the specific data entry page. Some data entry pages may also provide a breakdown of the components contributing to the total thermal power. The total thermal power displayed in individual pages does not include static power, which is reported in the **Power Summary** for the whole device.

Thermal power is the power dissipated in the device. Total Thermal Power fields on individual data entry pages contain the sum of dynamic and standby thermal power of all the resources used in the device. Total thermal power includes only the thermal component for the **I/O** data entry page and does not include external power dissipation, such as from voltage-referenced termination resistors.

Resource Utilization

Most data entry pages contain one or more fields that provide an estimate of the percentage of resource utilization for the modules in the specific page. The Intel FPGA PTC calculates these values based on the maximum available resources of a given type for a selected device. If resource utilization exceeds 100%, it indicates that the current device may not be able to support the resources entered into the data entry page.

Power Rail Current Consumption

Most data entry pages include a table showing the dynamic current consumption for all power rails used by the FPGA resources in the specific page. The same power rail may appear in multiple pages, and the dynamic currents reported in the **Report** page

are the sums of all corresponding currents for a given rail at a given voltage in individual pages. The **Report** page also includes static currents, which are not reported in individual pages.

Note:

- For Agilex FPGA portfolio devices, the **Power rail** summary is dynamic, and for each individual data entry page shows only those rails in use by the design for resources listed on that page. The **Power rail** summary on the **Report** page shows only the rails for the selected device.
- For Stratix 10 devices, the **Power rail** summaries on the individual data entry pages and on the **Report** page, show all available rails whether actually in use or not.
- For Agilex FPGA portfolio devices, verify that you set the **Power Characteristics** field on the **Main** page to **Maximum**. The Intel FPGA PTC does not report the current for a given power rail when you set **Power Characteristics** to **Typical**.

Why Typical Power Might Appear Larger than Maximum Power (Stratix 10 Devices Only)

Due to the methodologies employed by power modeling, instances can occur where the typical power for an Stratix 10 device may appear to be higher than the maximum power. Every Stratix 10 device is tested during the manufacturing process; this testing includes measuring the maximum static current drawn by each device rail, and total static power consumed across all rails. A given device does not draw maximum current on each rail simultaneously — consequently, the total static power actually consumed by the device in operation, is going to be lower than the sum of the individual maximum static powers measured for each rail.

The Intel FPGA PTC **Report** page (and the Quartus Prime Power Analyzer per-rail report) indicate the maximum per-rail static currents based on actual measurements, to help you choose appropriate voltage regulators. However, when calculating total thermal power and total static power, we make more realistic—and generally lower—assumptions for total static power across all rails.

Maximum power values are helpful for determining the proper regulator size for power delivery, and the proper thermal solution for cooling, to ensure operation to published specifications.

Typical power values are helpful for estimating average battery life or total cost of ownership. Typical values account for variations in process and are not based on real measurements of individual devices — they are not guaranteed values.

Instances can arise where the **Typical** power reported may be larger than the **Maximum** power. This aberration is a consequence of the modeling methods used, and is not indicative of an error.

Register Dynamic Power in Agilex FPGA Portfolio Devices

In Agilex FPGA portfolio devices, register dynamic power includes the power consumed by all of a register's ports, including its clock ports. Because the clock ports consume power, a register with a non-zero clock frequency also has non-zero power consumption, even if you have set the **Toggle %** column value to zero.

Input Device Utilization of Resources as a Percentage

Until the 23.3 release, PTC supported input of resource count as a number for all resources. For example, if you wanted 50% utilization for a Logic component, you had to find the total count available, compute 50% of that count, and input that number. This was particularly difficult for number rounding issues.

Starting with the 23.3 release, you can input resource utilization as a percentage (for example, 10%), and the "%" character informs PTC to appropriately compute and apply the resource count as an integer. This change helps in speeding up the process of estimating dynamic power consumption. DSP, Logic, and RAM resource pages support entering resource utilization as a percentage.

Note: PTC accepts only positive percentage values in the range of 1-100.

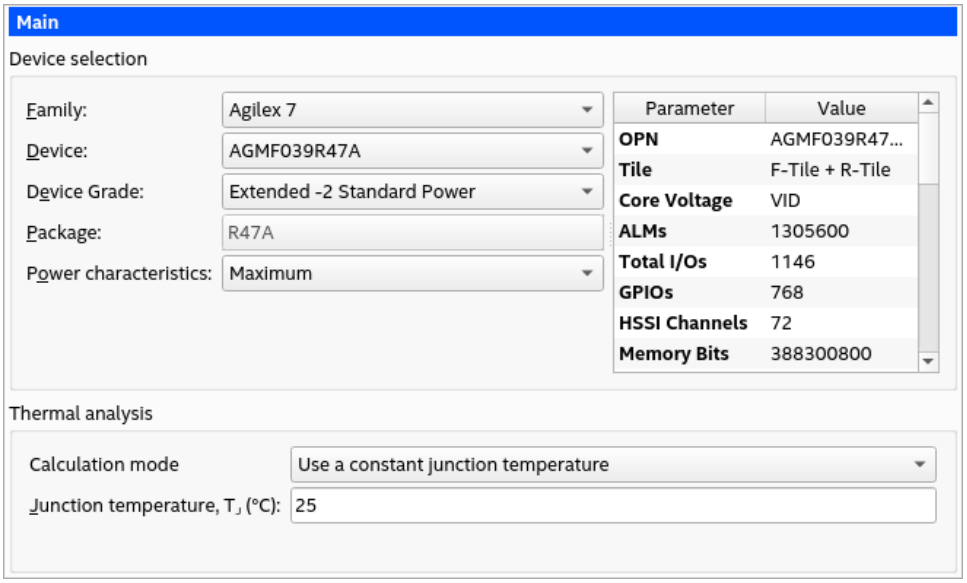
Related Information

Quartus Prime Pro Edition User Guide: Power Analysis and Optimization

4.3. Intel FPGA PTC - Main Page

The **Main** data entry page of the Intel FPGA Power and Thermal Calculator (PTC) allows you to enter device, package, and cooling information, and displays thermal analysis options.

Figure 35. Intel FPGA PTC Main Page



The required parameters depend on whether the junction temperature is manually entered or auto computed.

Table 10. Device Selection Parameters

Parameter	Description
Family	Shows the device family selected at startup, either directly or through the imported file.
Device	Select your device. Larger devices consume more static power and have higher clock dynamic power. All other power components are unaffected by device selection. The parameter and value table on the right side of the PTC main page displays specifications of the currently selected device.
Device Grade	Select the combination of Operating Temperature, Speed Grade, and Power Option used. Refer to the device datasheet for available combinations.
Package	Select the device package. Larger packages provide a larger cooling surface and more contact points to the circuit board; thus they offer lower thermal resistance. Package selection does not affect dynamic power directly.
Power characteristics	Select typical or maximum power. There is a process variation from die-to-die. This variation primarily affects static power consumption. If you choose **Typical** power characteristics, estimates are based on long term projections of average power consumed by typical silicon. For FPGA board power supply design and thermal design, choose **Maximum** for worst-case values. *Note:* **Typical** power characteristics should not be used for regulator sizing or thermal analysis; use **Maximum** power characteristics for these activities.
V_{CC} Voltage (mV)	(This field appears in the Stratix 10 PTC only.)

Note: "Power model status" parameter is now visible as one of the rows in the parameter and value table on the right side of the PTC main page.

The Thermal Analysis section displays the junction temperature (T_J) and other thermal parameters, depending on the thermal analysis mode.

Table 11. Thermal Analysis

Column Heading	Description
Calculation mode	Specifies the calculation mode for the thermal solver to use. The available choices are: • **Use a constant junction temperature**. • **Find cooling solution for maximum junction temperature limit**. • **Find available thermal margin for cooling solution**. • **Find ambient temperature for specified cooling solution**. *Note:* 1. To enable selection of non-constant calculation modes, the **Power characteristics** field in the **Device selection** group box must be set to **Maximum**. 2. For more detailed information on **Calculation mode** settings, refer to *Intel FPGA PTC - Thermal Page*.
Junction temperature, T_J (°C)	Specify the junction temperature for all dies in the package. This field is available when you select **Use a constant junction temperature** as the **Calculation mode**. In this mode, the junction temperatures for all dies in the package are assumed to have the specified value. To automatically compute junction temperatures, select one of the other options in the same field.

Related Information

Intel FPGA PTC - Thermal Page on page 75

4.3.1. Intel FPGA PTC - Device Selection and Thermal Analysis Windows

The **Device Selection** window displays information also available on the **Main** page; the **Thermal Analysis** window displays a subset of the information available on the **Thermal** page.

The **Device Selection** and **Thermal Analysis** pages can be displayed at all times, allowing you to view this information while working on a page other than the **Main** page.

4.4. Intel FPGA PTC - Logic Page

The **Logic** data entry page of the Intel FPGA Power and Thermal Calculator (PTC) allows you to enter logic resource properties for all modules in your design.

Figure 36. Logic Page of the Intel FPGA PTC

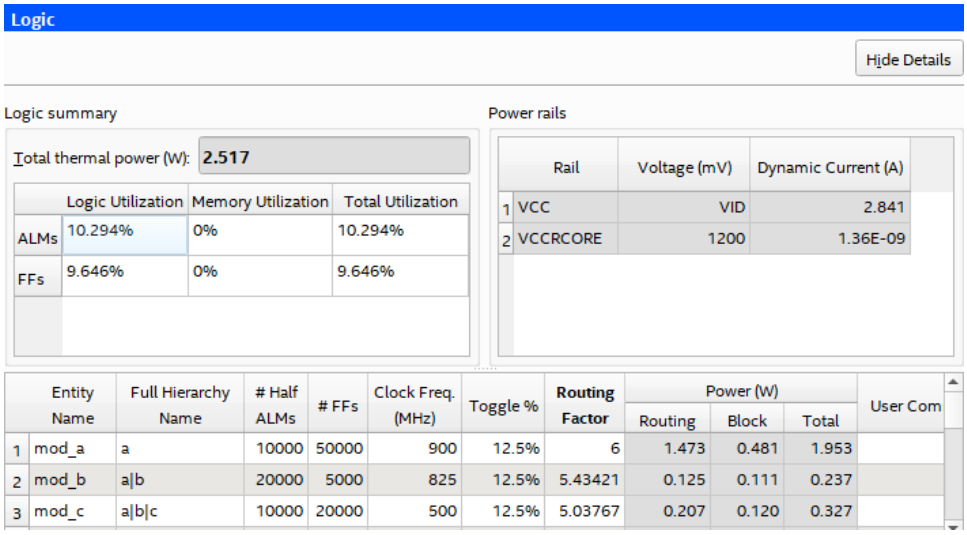


Table 12. Logic Page Information

Column Heading	Description
Entity Name	Specify a name for each entity of the design. This is an optional entry.
Full Hierarchy Name	Specify the hierarchical path relevant to this entry. This is an optional entry. When entering levels of hierarchy, the pipe character (|) denotes a level of hierarchy. (Instance paths may, optionally, begin with a leading pipe character; but regardless of whether a leading pipe is there or not, paths are treated the same.)
#Half ALMs	Enter twice the number of Adaptive Logic Modules (ALMs) used in your design, which you can find in the Compilation Report, by selecting **Fitter ➤ Place Stage ➤ Resource Usage Summary**. For power estimation purposes, the number of ALMs used in your design is the sum of the following values in the Compilation Report: • ALMs used for LUT logic and register circuitry • ALMs used for LUT logic • ALMs used for register circuitry • ALMs adjustment for power estimation The adjustment for power estimation is necessary because some unused ALMs may still consume power due to Fitter optimizations. For more information, refer to Calculating Register Utilization on page 48. *Note:* This field can also accept a percentage (for example, 10%) as an input, which is used to calculate the number of half ALMs. The "%" character informs PTC to appropriately compute and apply the resource count as an integer.
# FFs	Enter the number of **Primary logic registers**, plus **Secondary logic registers**, plus the number of registers reported as **Register control circuitry for power estimation**, all of which you can find in the Compilation Report, by selecting **Fitter ➤ Place Stage ➤**

continued...

Column Heading		Description
		Resource Usage Summary. The **Register control circuitry for power estimation** adjustment is necessary because some unused registers may still consume power due to fitter optimizations. Clock routing power associated with flipflops is calculated separately on the Clock page of the Intel FPGA PTC. *Note:* This field can also accept a percentage (for example, 10%) as an input, which is used to calculate the number of flipflops,
Clock Freq (MHz)		Enter a clock frequency (in MHz). This value is limited by the maximum frequency specification for the device family. For Stratix 10 devices, when you import a design from the Quartus Prime software, some imported half ALMs and flipflops may have a clock frequency of 0 MHz; this can occur for one of two reasons: • The Quartus Prime software did not have sufficient information to determine clock frequency due to incomplete clock constraints. • The Quartus Prime software exported a `.qptc` file containing half ALMs where only flipflops are used. Such ALMs are imported as ALMs with clock frequency of 0 MHz, while their flipflops are imported into a separate row with the correct clock frequency. It is possible that due to the floating point precision used in the tool, the frequency reported may differ slightly from what is reported in the Timing Analyzer.
Toggle %		Enter the average percentage of clock cycles when the block output signals change values. Toggle percentage is multiplied by clock frequency to determine the number of transitions per second. For example, 100 MHz frequency with a 12.5% toggle rate, means that each LUT or flipflop output toggles 12.5 million times per second (100MHz × 12.5%). The toggle percentage ranges from 0 to 100%. Typically, the toggle percentage is 12.5%, which is the toggle percentage of a 16-bit counter. Most logic only toggles infrequently; therefore, toggle rates of less than 50% are more realistic. To ensure you do not underestimate the toggle percentage, use a realistic toggle percentage obtained through simulation. For example, a T flipflop (TFF) with its input tied to VCC has a toggle rate of 100% because its output is changing logic state on every clock cycle. Refer to the 4-Bit Counter Example below for a more detailed analysis. For any rows containing flipflops, toggle percentage cannot exceed 100%. A small portion of ALMs in a design may experience glitching that results in toggle percentage exceeding 100% for such ALMs. Enter such ALMs into a separate row with # FFs set to 0. For Stratix 10 devices in the Intel FPGA PTC, toggle percentage cannot exceed 100% in any rows containing flipflops.
Routing Factor		Indicates the extent of the routing power of the outputs. Characteristics that have a large power impact and are captured by this factor include the following: • The fanout of the outputs • The number of routing resources used • The relative power usage of the different types of routing resources used The default value for this field is typical; the actual value varies between blocks in your design, and depends on the placement of your design. For most accurate results, you should import this value from the Quartus Prime software after compiling your design, because the Quartus Prime software has access to detailed placement and routing information. In the absence of an Quartus Prime design, higher values generally correspond to signals that span large distances on the FPGA and fanout to many destinations, while lower values correspond to more localized signals. You can change this field from its default value to explore possible variations in power consumption depending on block placement. When changing this value, keep in mind that typical designs rarely use extreme values, and only for a small subset of the design.
Power (W)	Routing	Indicates the power dissipation due to estimated routing (in W). Routing power depends on placement and routing, which is a function of design complexity. The values shown are representative of routing power based on observed behavior across more than 100 real-world designs. Use the Quartus Prime Power Analyzer for accurate analysis based on the exact routing used in your design.

continued...

Column Heading		Description
		Note: Only routing power used for Logic resources is included here.
	Block	Indicates the power dissipation due to internal toggling of the ALMs and registers (in W). Logic block power is a combination of the function implemented and the relative toggle rates of the various inputs. The Intel FPGA PTC uses an estimate based on observed behavior across more than 100 real-world designs. Use the Quartus Prime Power Analyzer for accurate analysis based on the exact synthesis of your design.
	Total	Indicates the estimated power (in W), based on information entered into the Intel FPGA PTC. It is equal to the sum of routing power and block power.
User Comment		Enter any comments. This is an optional entry.

Note: To resize columns within a page, first maximize the Intel FPGA PTC window size. You can also resize all columns on all pages by selecting **View ➤ Resize All Columns**, or by pressing F5 on your keyboard.

Calculating ALM Utilization

ALM utilization reported by the Intel FPGA PTC may differ from utilization reported by the Quartus Prime Fitter.

The Fitter counts resources used by design logic, and reports logic utilization to help you understand whether the device has more available room in which to fit additional logic. The Intel FPGA PTC counts resources that require power in the physical silicon implementation.

From a power perspective, the estimate of total ALM utilization includes both the ALMs used by the design logic and other resources not counted by the Fitter that also consume power. The *ALMs adjustment for power estimation* value represents the powered resources not counted by the Fitter.

As an example, for a circuit with two flipflops placed in two different ALM locations, the Fitter reports *one* ALM of logic utilization—because the flipflops could be packed more densely if the chip was more fully utilized. But from the power perspective, the utilization is *two*, because two physical ALMs are consumed and powered on the chip. Because the Intel FPGA PTC tracks the number of half ALMs, you should enter 4 half ALMs into the *#Half ALMs* column.

The following equation represents the calculation of the total number of half-ALMs consuming power:

```
# Half ALMs = (ALMs used for LUT logic and register circuitry + ALMs used for
LUT logic + ALMs used for register circuitry + ALMs adjustment for power
estimation) * 2
```

Calculating Register Utilization

The following equation represents the calculation of the total number of registers consuming power:

```
Total ALM Registers for power estimation = Primary logic registers + Secondary
logic registers + Register control circuitry for power estimation
```

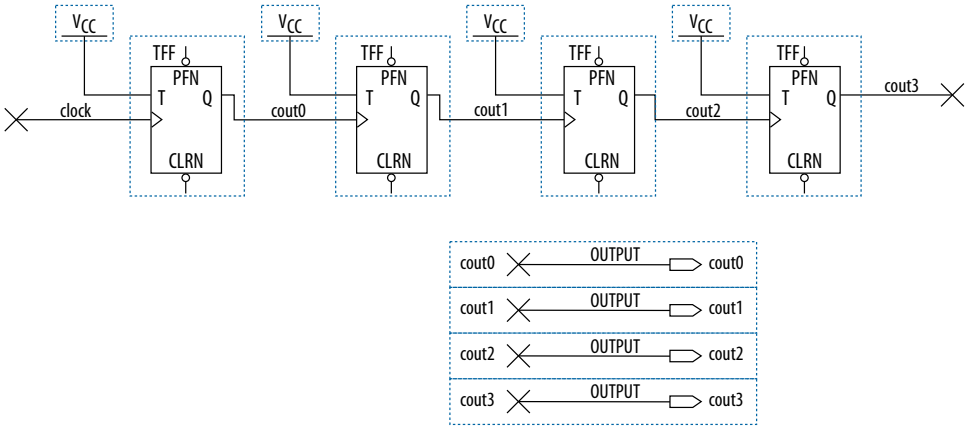
This example illustrates the above equation: The `primary logic registers` and `secondary logic registers` account for the ALM registers used by the design, and are reported by the Fitter.

The `register control circuitry for power estimation` is an adjustment that accounts for the ALM registers bypassed in the design. When Fitter timing optimizations result in a register being retimed from an ALM register location into a Hyper-Register location, the ALM register location is configured to be in "bypass mode," which still consumes power.

Calculating Toggle %

The following example illustrates the calculation of toggle percentage.

Figure 37. 4-Bit Counter Example



The `cout0` output of the first TFF has a toggle percentage of 100% because the signal toggles on every clock cycle. The toggle percentage for the `cout1` output of the second TFF is 50% because the output toggles every two clock cycles. Similarly, the toggle percentage for the `cout2` and `cout3` outputs are 25% and 12.5%, respectively. Therefore, the average toggle percentage for this 4-bit counter is (100 + 50 + 25 + 12.5)/4 = 46.875%.

For more information about logic block configurations, refer to the *Agilex 7 Logic Array Blocks and Adaptive Logic Modules User Guide*.

Related Information

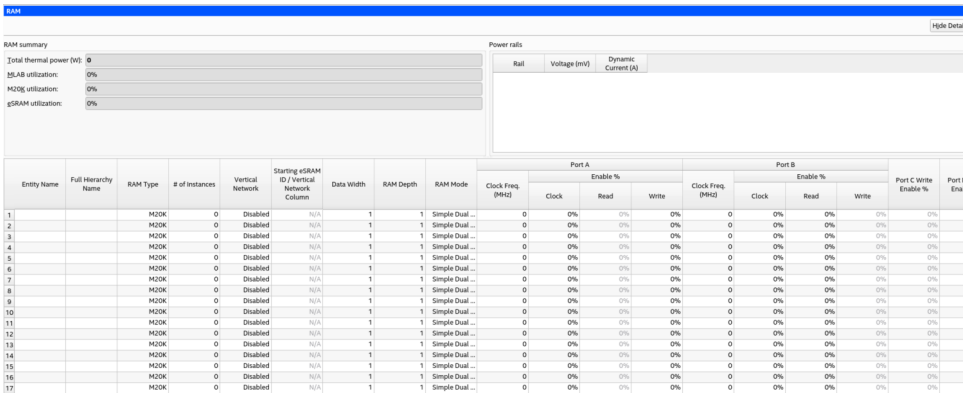
Agilex 7 Logic Array Blocks and Adaptive Logic Modules User Guide

4.5. Intel FPGA PTC - RAM Page

Each row in the **RAM** data entry page of the Intel FPGA Power and Thermal Calculator (PTC) represents a design module with RAM blocks of the same type, same data width, same RAM depth (if applicable), same RAM mode, and the same port parameters.

The Intel FPGA PTC implements each logical RAM module with the minimum number of physical RAM blocks, in the most power-efficient way possible, based on the specified logical width and depth.

Figure 38. RAM Page of the Intel FPGA PTC



You must know how your RAM is implemented by the Quartus Prime Compiler when you are selecting the RAM block mode. For example, if a ROM is implemented with two ports, it is considered a true dual-port memory and not a ROM. Single-port and ROM implementations use only one port. Simple dual-port and true dual-port implementations use both Port A and Port B.

Note:

- The Intel FPGA PTC reports MLAB power in the RAM page as described above, as well as in the *Power Summary* table.
- In the **Power Summary** table, the MLAB power for Agilex FPGA portfolio device families is spread across three categories: RAM, Logic, and Miscellaneous (which includes the dynamic power (W) consumed by other FPGA circuitry). This is done to be consistent with the reporting provided in the Quartus Prime Power Analyzer.
- Some fields on the **RAM** page are not available for all device families.

Table 13. RAM Page Information

Column Heading	Description
Entity Name	Enter a name for the RAM entity in this row. This value is optional.
Full Hierarchy Name	Specify the hierarchical path relevant to this entry. This entry is optional. When entering levels of hierarchy, the pipe character (|) denotes a level of hierarchy.
RAM Type	Select the implemented RAM type. You can find the RAM type in the *Type* column of the Quartus Prime Compilation Report. In the Compilation Report, select **Fitter ➤ Place Stage ➤ Fitter RAM Summary**.
# of Instances	Enter the number of logical RAM instances in the module that use the same memory type and mode and have the same port parameters. *Note:* This field can also accept a percentage (for example, 10%) as an input, which is used to calculate the number of instances. The "%" character informs PTC to appropriately compute and apply the resource count as an integer. The parameters for each port are: • Clock frequency in MHz • Percentage of time the RAM is enabled • Percentage of time the port is writing as opposed to reading You can find the number of RAM blocks in either the *MLAB cells* or *M20K blocks* column of the Quartus Prime Compilation Report. In the Compilation Report, select **Fitter ➤ Place Stage ➤ Fitter RAM Summary**.

continued...

Column Heading	Description
	Note: The value entered into this field represents the number of logical memory blocks. Depending on the specified memory depth and data width, more than one physical memory block may be required to implement one logical block. The Power and Thermal Calculator calculates the number of physical memory blocks based on the specified memory depth and data width, such that the minimum number of physical blocks is used, and assuming the most power efficient physical configuration.
Vertical Network	For M20K RAM Type, this field specifies whether the RAM is used in vertical network. The following options can be selected: • Disabled • Top • Bottom This column is available for Agilex 7 M-series devices only.
Starting eSRAM ID / Vertical Network Column	Specify placement information for thermal modeling. This field is applicable only when **RAM Type** is set to *eSRAM* and **# RAM Blocks** is set to *1*, or when RAM type is set to M20K with vertical network enabled. (This column is available for Agilex FPGA portfolio device families only).
Data Width	Enter the width of the data for the RAM block. This value is limited based on the RAM type. You can find the width of the RAM block in the *Port A Width* or the *Port B Width* column of the Quartus Prime Compilation Report. In the Compilation Report, select **Fitter ➤ Place Stage ➤ Fitter RAM Summary**. For RAM blocks that have different widths for Port A and Port B, use the larger of the two widths.
RAM Depth	Enter the depth of the RAM block in number of words. You can find the depth of the RAM block in the *Port A Depth* or the *Port B Depth* column of the Quartus Prime Compilation Report. In the Compilation Report, select **Fitter ➤ Place Stage ➤ Fitter RAM Summary**.
RAM Mode	For MLAB and eSRAM RAM types, this field has only one possible value: Simple Dual Port. For M20K RAM type, select from the following modes: • Simple Dual Port • True Dual Port • Simple Dual Port with ECC • ROM • Simple Quad Port The mode is based on how the Quartus Prime Compiler implements the RAM. If you are unsure how your memory module is implemented, you can compile a test case in the required configuration in the Quartus Prime software. You can find the RAM mode in the *Mode* column of the Quartus Prime Compilation Report. In the Compilation Report, select **Fitter ➤ Place Stage ➤ Fitter RAM Summary**. A single-port RAM has one port with a read and a write control signal. A simple dual-port RAM has one read port and one write port. A true dual-port RAM has two ports, each with a read and a write control signal. ROMs are read-only single-port RAMs. A simple quad-port RAM has a total of four ports, two read ports and two write ports. *Note:* While you can use MLAB to implement more than just Simple Dual Port memory, the differences for different modes are accounted for indirectly through other input fields. For example, if one of the ports is unused, you should set its clock frequency to 0. Similarly, if MLAB is used in ROM mode, you should set **Port A - Write Enable %** to 0. Also, if additional registers are used for MLAB output, you should specify those on the **Logic** page.
Port A - Clock Freq (MHz)	Enter the clock frequency for Port A of the RAM blocks (in MHz). This value is limited by the maximum frequency specification for the RAM type and device family.

continued...

Column Heading		Description
Port A - Clock Enable %		The average percentage of time the Port A clock enable is active, regardless of activity on RAM data and address inputs. This number must be a percentage between 0% and 100%. RAM power is consumed primarily when a clock event occurs. Using a clock enable signal to disable a port when no read or write operation is occurring can result in significant power savings.
Port A - Read Enable %		Enter the percentage of time Port A of the RAM block is in read mode. This field is applicable only for true dual port RAMs. This value must be a percentage number between 0 and 100%.
Port A - Write Enable %		Enter the average percentage of time Port A of the RAM block is in write mode. This field applies only for dual port, true dual port, and quad port RAMs. This value must be a percentage number between 0 and 100%.
Port B - Clock Freq (MHz)		Enter the clock frequency for Port B of the RAM blocks (in MHz).
Port B - Clock Enable %		Enter the average percentage of time the input clock enable for Port B is active, regardless of the activity on the RAM data and address inputs. The enable percentage ranges from 0 to 100%. RAM power is consumed primarily when a clock event occurs. Using a clock-enable signal to disable a port when no read or write operation is occurring can result in significant power savings.
Port B - Read Enable %		Enter the percentage of time Port B of the RAM block is in read mode. This field is applicable only to dual port, true dual port, and quad port RAMs and ROMs. This value must be a percentage number between 0 and 100%.
Port B - Write Enable %		Enter the percentage of time Port B of the RAM block is in write mode. This field is available only for true dual-port mode. This value must be a percentage number between 0 and 100%.
Port C - Write Enable %		Enter the percentage of time the RAM block is writing to this port. In Simple Quad-Port Mode, clock and clock enable for all parts are shared and the same as Port A. This value must be a percentage number between 0 and 100%.
Port D - Read Enable %		Enter the percentage of time the RAM block is reading on this port. In Simple Quad-Port Mode, clock and clock enable for all parts are shared and the same as Port A. This value must be a percentage number between 0 and 100%.
Vertical Network Port – Read From External Memory Enable %		Enter the percentage of time the data is read from external memory into M20K blocks. This value must be a percentage number between 0 and 100%. This column is available for Agilex 7 M-Series devices only.
Vertical Network Port – Clock Enable %		Enter the average percentage of time the vertical network port clock enable is active, regardless of activity on data and address input. This value must be a percentage number between 0 and 100%. This column is available for Agilex 7 M-Series devices only.
Toggle %		The percentage of clock cycles when the block output signal changes value. This value is multiplied by the clock frequency and the enable percentage to determine the number of transitions per second. This value affects only routing power. 50% corresponds to a randomly changing signal, since half the time the signal holds the same value and thus not transition. This is considered the highest meaningful toggle rate for a RAM block.
Power (W)	Routing Power (W)	Indicates the power dissipation due to estimated routing (in W). Routing power depends on placement and routing, which is a function of design complexity. The values shown represent the routing power estimate based on observed behavior across more than 100 real-world designs. Use the Quartus Prime Power Analyzer for accurate analysis based on the exact routing used in your design.
	Block Power (W)	Indicates the power dissipation due to internal toggling of the RAM (in W).

continued...

Column Heading		Description
		Use the Quartus Prime Power Analyzer for accurate analysis based on the exact RAM modes in your design.
	Total Power (W)	Indicates the estimated power (in W), based on information entered into the Intel FPGA PTC. Total power is equal to the sum of routing power and block power.
User Comments		Enter any comments. This is an optional entry.

Related Information

Agilex 7 Embedded Memory User Guide

4.6. Intel FPGA PTC - DSP Page

Each row in the **DSP** data entry page of the Intel FPGA Power and Thermal Calculator (PTC) represents a DSP design module where all instances have the same configuration, clock frequency, toggle percentage, and register usage.

Figure 39. DSP Page of the Intel FPGA PTC

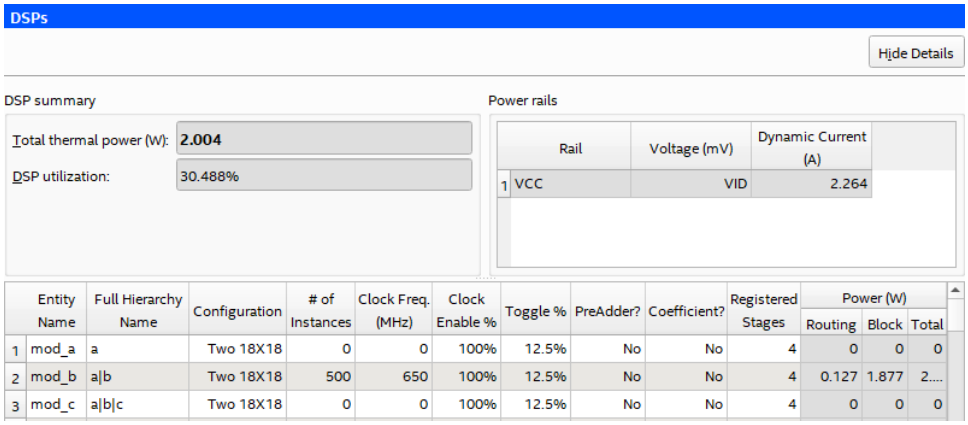


Table 14. DSP Page Information

Column Heading	Description
Entity Name	Enter a name for the DSP entity in this column. This is an optional value.
Full Hierarchy Name	Specify the hierarchical path relevant to this entry. This is an optional entry. When entering levels of hierarchy, the pipe character (|) denotes a level of hierarchy.
Configuration	Select the DSP block configuration for the module.
# of Instances	Enter the number of DSP block instances that have the same configuration, clock frequency, toggle percentage, and register usage. *Note:* This field can also accept a percentage (for example, 10%) as an input, which is used to calculate the number of instances. The "%" character informs PTC to appropriately compute and apply the resource count as an integer. This value is not necessarily equal to the number of dedicated DSP blocks you use. For example, it is possible to use two 18 × 18 simple multipliers that are implemented in the same DSP block in the FPGA devices. In this case, the number of instances would be two.

continued...

Column Heading		Description
		To determine the maximum number of instances you can fit in the device for any particular mode, follow these steps: 1. Open the "Variable Precision DSP Blocks" chapter of the appropriate device family handbook. 2. In the "Number of DSP Blocks" table, take the maximum number of DSP blocks available in the device for the mode of operation. 3. Divide the maximum number by the "# of Mults" for that mode of operation from the "DSP Block Operation Modes" table. The resulting value is the maximum number of instances supported by the device.
Clock Freq (MHz)		Enter the clock frequency for the module (in MHz). This value is limited by the maximum frequency specification for the device family.
Clock Enable %		Specifies the percentage of time that the DSP block is enabled. (Agilex FPGA portfolio only.)
Toggle %		Enter the average percentage of DSP data outputs toggling on each clock cycle. The toggle percentage ranges from 0 to 50%. The default value is 12.5%. For a more conservative power estimate, use a higher toggle percentage. 50% corresponds to a randomly changing signal, since half the time the signal holds the same value and thus not transition. This is considered the highest meaningful toggle rate for a DSP block.
Preadder?		Select **Yes** if the PreAdder function of the DSP block is turned on.
Coefficient?		Select **Yes** if the Coefficient function of the DSP block is turned on.
Registered Stages		Select number of the registered stages. Permitted values depend on the selected mode; some modes, such as floating-point multiply and accumulate cannot have 0 register stages.. • 0—None • 1—Input • 2—Input and Output • 3—Input, Output, and Multiplier • 4— Input, Output, Multiplier, and Pipeline Stage 2 • 5—Input, Output, Multiplier, Pipeline Stage 2, and Floating-Point Adder
Power (W)	Routing	Indicates the power dissipation due to estimated routing (in W). Routing power depends on placement and routing, which is a function of design complexity. The values shown represent the routing power estimate based on observed behavior across more than 100 real-world designs.
	Block	Indicates the estimated power consumed by the DSP blocks (in W).
	Total	Indicates the estimated power (in W), based on information entered into the Intel FPGA PTC. It is the total power consumed by the DSP blocks and is equal to the routing power and block power.
User Comments		Enter any comments. This is an optional entry.

Related Information

Agilex 7 Variable Precision DSP Blocks User Guide

4.7. Intel FPGA PTC - Clock Page

Each row in the **Clock** page of the Intel FPGA Power and Thermal Calculator (PTC) represents a clock network or a separate clock domain in the design.

Agilex 5, Agilex 7, and Stratix 10 devices support global, regional, and periphery clock networks. The Intel FPGA PTC does not distinguish between global or regional clocks because the difference in power is not significant.

Figure 40. Clock Page of the Intel FPGA PTC

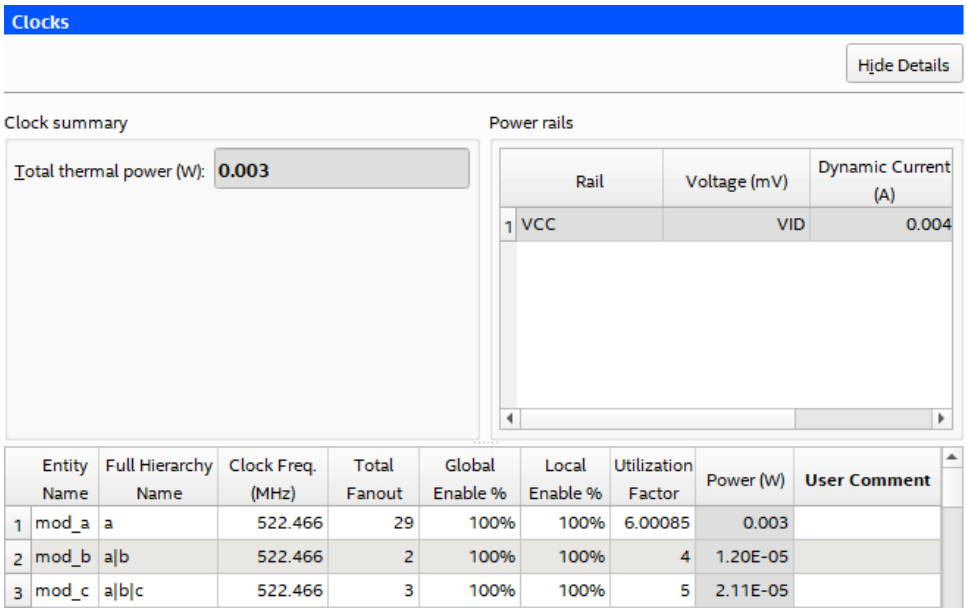


Table 15. Clock Page Information

Column Heading	Description
Entity Name	Enter a name for the clock entity in this column. This is an optional value.
Full Hierarchy Name	Enter the full hierarchy name for the entity represented in this row. Delimit levels of hierarchy with a vertical bar (|) symbol, for example: a|b|c.
Clock Freq (MHz)	Enter the frequency of the clock domain. This value is limited by the maximum frequency specification for the device family. *Note:* When you import a design from the Quartus Prime software, some imported clocks may have a frequency of 0 MHz, due to either of the following reasons: • The Quartus Prime software did not have sufficient information to determine clock frequency due to incomplete clock constraints. • Clock resources were used to route a reset signal, which toggles infrequently, so its frequency is reported as 0 MHz.
Total Fanout	Enter the total number of flipflops, hyper-registers, RAMs, digital signal processing (DSP) blocks, and I/O pins fed by this clock. The number of resources driven by every global clock and regional clock signal is reported in the *Fan-out* column of the Quartus Prime Compilation Report. In the Compilation Report, select **Fitter** and click **Place Stage**. Select **Global & Other Fast Signals Summary** and observe the *Fan-out* value.

continued...

Column Heading	Description
	Note: Power consumed by Stratix 10 MLAB clocks is accounted for in the RAM page; therefore, clock fanout on this page does not include any MLABs driven by this clock domain, for Stratix 10 devices. For Agilex FPGA portfolio devices, MLAB is included in the fanout.
Global Enable %	Enter the average percentage of time that the entire clock tree is enabled. Each global clock buffer has an enable signal that you can use to dynamically shut down the entire clock tree.
Local Enable %	Enter the average percentage of time that clock enable is high for destination flipflops. Local clock enables for flipflops in ALMs are promoted to LAB-wide signals. When a given flipflop is disabled, the LAB-wide clock is disabled, cutting clock power and the power for down-stream logic. This page models only the impact on clock tree power.
Utilization Factor	Represents the impact of the clock network configuration on power. Characteristics that have a large impact on power and are captured by this factor include the following: • Whether the network is widely spread out • Whether the fanout is small or large • The clock settings within each LAB The default value for this field is typical; the actual value varies between clocks in your design, and depends on the placement of your design. For most accurate results, you should import this value from the Quartus Prime software after compiling your design, because the Quartus Prime software has access to detailed placement information. In the absence of an Quartus Prime design, higher values generally correspond to signals that span large distances on the FPGA and fanout to many destinations, while lower values correspond to more localized signals. You can change this field from its default value to explore possible variations in power consumption depending on block placement. When changing this value, keep in mind that typical designs rarely use extreme values, and only for a small subset of the design.
Power (W)	Indicates the total power dissipation due to clock distribution (in W).
User Comments	Enter any comments. This is an optional entry.

Note: The **Domain** column which appeared in earlier versions of the PTC, is now the **Full Hierarchy Name** column. If you import a design file from a previous version of the PTC, any **Domain** entries will now appear in the **Full Hierarchy Name** column.

For more information about the clock networks of Agilex 7 devices, refer to the *Agilex 7 Clocking and PLL User Guide*.

Related Information

- Agilex 7 Clocking and PLL User Guide: F-Series and I-Series
- Agilex 7 Clocking and PLL User Guide: M-Series

4.8. Intel FPGA PTC - PLL Page

Each row in the **PLL** data entry page of the Intel FPGA Power and Thermal Calculator (PTC) represents one or more PLLs in the device.

Supported PLL types are family dependent, as outlined in the *PLL Page Information* table:

Figure 41. PLL Page

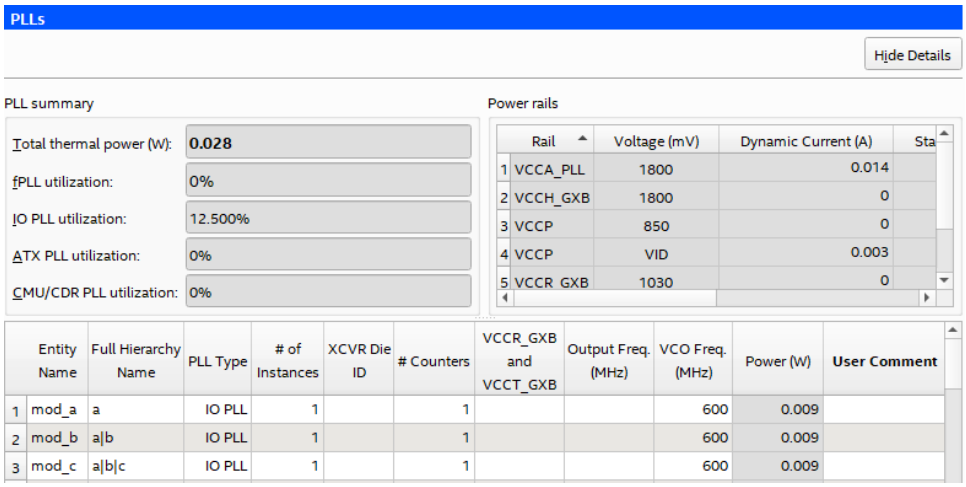


Figure 42. PLL Page (Agilex FPGA Portfolio Devices)

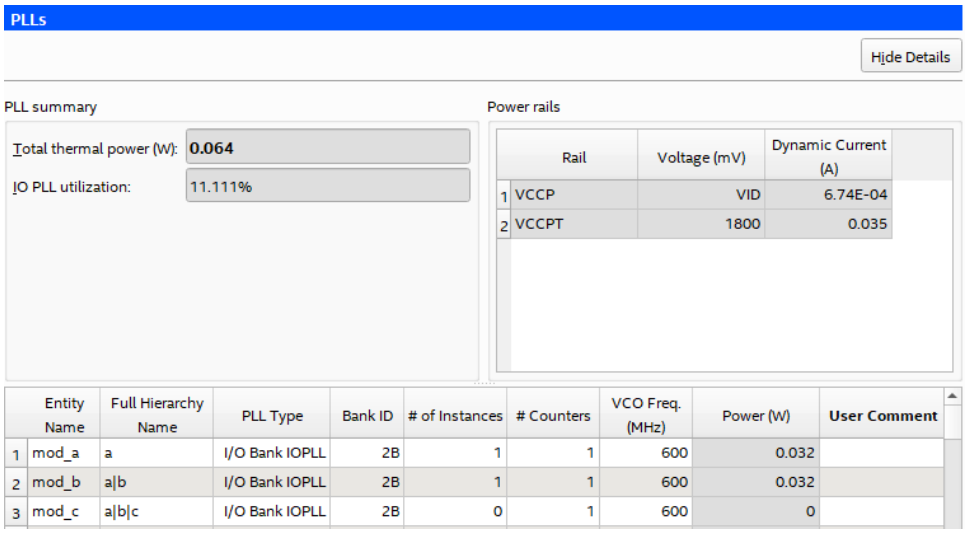


Table 16. PLL Summary Information

Column Header	Description
Total thermal power (W)	Reports the total thermal power (in W).
fPLL utilization	Reports the percentage of fPLL utilization. (This field is available for Stratix 10 devices only.)
IO PLL utilization	Reports the percentage of I/O PLL utilization.

continued...

Column Header	Description
ATX PLL utilization	Reports the percentage of ATX PLL utilization. (This field is available for Stratix 10 devices only.)
CMU/CDR PLL utilization	Reports the percentage of CMU/CDR PLL utilization. (This field is available for Stratix 10 devices only.)
Power rails	Indicated the voltage (mV), dynamic current (A), and standby current (A), for various power rails.

Table 17. PLL Page Information

Column Heading	Description
Entity Name	Specify a name for the PLL entity in this column. This is an optional value.
Full Hierarchy Name	Specify the hierarchical path relevant to this entry. This is an optional entry. When entering levels of hierarchy, the pipe character (|) denotes a level of hierarchy.
PLL Type	Specifies the type of PLL, which may include the following: • Fabric-feeding IOPLLs • I/O bank IOPLLs • fPLLs • CMU PLLs • I/O PLLs • ATX PLLs (The availability of some PLL types depends on the selected device.)
# of Instances	The number of logical PLL instances with this type, counter, voltage, and frequency combination.
Bank ID	The I/O bank ID for this row. A bank location can be assigned to PLLs to change how the PLLs are placed, affecting thermals and utilization. (This column is available for Agilex FPGA portfolio devices only.)
# PLL Blocks	Enter the number of PLL blocks with the same combination of parameters.
XCVR Die ID	Specify the transceiver die on which PLLs on this row are located. This field is not applicable for I/O PLLs, nor fabric-feeding I/O PLLs.
# Counters	Enter the number of counters of the PLL.
V_{CCR_GXB} and V_{CCT_GXB} Voltage	Specify the voltage of the V_{CCR_GXB} and V_{CCT_GXB} rails. This field is not applicable for I/O PLLs, nor fabric-feeding I/O PLLs.
Output Freq (MHz)	Specify the output frequency for CMU and ATX PLLs.
VCO Freq (MHz)	Specify the internal VCO operating frequency for PLLs.
Total Power (W)	Shows the total estimated power for this row (in W).
User Comments	Enter any comments. This is an optional entry.

For more information about the PLLs available in Agilex FPGA portfolio devices, refer to the *Agilex 7 Clocking and PLL User Guide* and *Agilex 5 Clocking and PLL User Guide*.

Related Information

- Agilex 7 Clocking and PLL User Guide: F-Series and I-Series
- Agilex 7 Clocking and PLL User Guide: M-Series

4.9. Intel FPGA PTC - I/O Page

Each row in the **I/O** data entry page of the Intel FPGA Power and Thermal Calculator (PTC) represents a design module with I/O pins that have the same I/O standard, input termination, current strength or output termination, data rate, clock frequency, output enable static probability, and capacitive load.

The Intel FPGA PTC assumes that you are using external termination resistors as recommended for SSTL and high-speed transceiver logic HSTL. If your design does not use external termination resistors, choose the LVTTL/ LVCMOS I/O standard with the same VCCIO and similar current strength as the terminated I/O standard.

To use on-chip termination (OCT), select the **Current Strength/Output Termination** option in the Intel FPGA PTC.

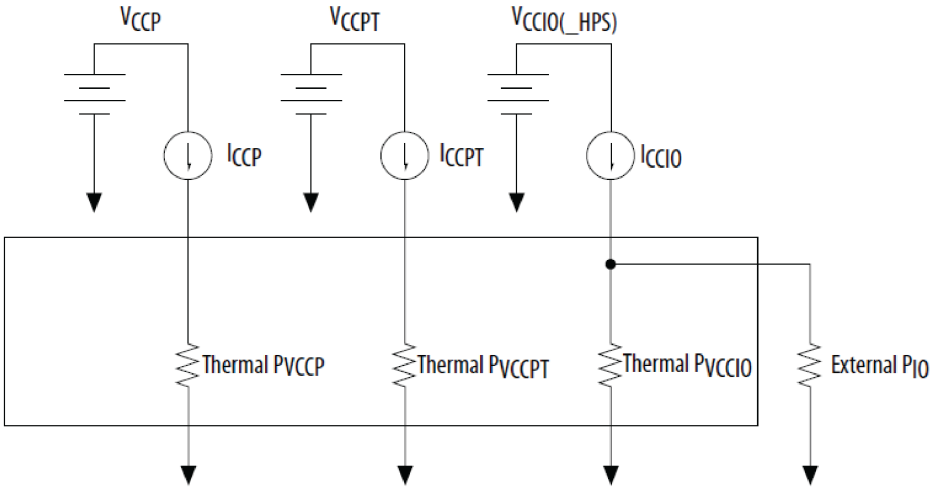
The power reported for the I/O signals includes thermal and external I/O power. The total thermal power is the sum of the thermal power consumed by the device from each power rail, as shown in the following equation.

Figure 43. Total Thermal Power

$$\text{thermal power} = \text{thermal } P_{VCCP} + \text{thermal } P_{VCCPT} + \text{thermal } P_{VCCIO}$$

The following figure shows the I/O power consumption. The I_{CCIO} power rail includes both the thermal P_{IO} and the external P_{IO}:

Figure 44. I/O Power Representation



The VREF pins consume minimal current (typically less than 10 µA), which is negligible when compared with the current consumed by the general purpose I/O (GPIO) pins; therefore, the Intel FPGA PTC does not include the current for VREF pins in the calculations.

Figure 45. I/O Page of the Intel FPGA PTC for Agilex FPGA Portfolio Devices

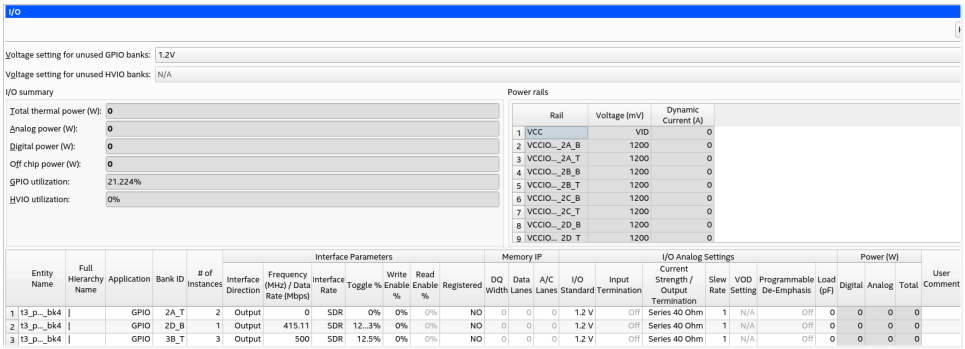


Table 18. I/O Page Information for Agilex FPGA Portfolio Devices

Column Heading		Description
Voltage setting for unused GPIO banks		Select a value to calculate voltage of unused GPIO banks. Available values are **1.0V**, **1.05V**, **1.1V**, **1.2V**, **1.3V**, **1.5V**, and **Power Down Unused GPIO Banks**. *Note:* The availability of some voltage settings depend on the device selected.
Voltage setting for unused HVIO banks		Select a value to calculate voltage of unused HVIO banks. This field applies only to Agilex 5 devices. Available values are **1.8V**, **2.5V**, **3.3V**, and **Power Down Unused GPIO Banks**.
Entity Name		Specify an entity name in this column. This is an optional value.
Full Hierarchy Name		Specify the full hierarchy name for this row, with hops delimited by the pipe character (|). If this filed is left blank, this row is assigned to the root instance. Leading, training, and duplicate vertical bars are ignored. Leading and trailing whitespace is ignored.
Application		Specify the application for this I/O row. Using this field: • For Agilex 7 E-Series, F-Series, and I-Series devices, GPIO, EMIF, and SerDes interface can be instantiated. For Agilex 7 M-Series devices, GPIO, SERDES, EMIF DDR4, DDR5, and LPDDR5 can be instantiated. • For Agilex 5 devices, GPIO, SERDES, EMIF DDR4, LPDDR4, LPDDR5, HVIO, and RGMII can be instantiated.
Bank ID		The I/O bank ID for this row. A bank location can be assigned to I/O pins to change how the I/O resources are placed, affecting thermals and utilization. If one row uses more I/O resources than available in the assigned bank, resources overflow to the next available bank.
# of Instances		Enter the number of SerDes channels, IO Pins or IO PHY Lanes in this module.
Interface Parameters	Interface Direction	Specifies the direction of pins/SerDes channels. For SerDes, the DPA mode in which the SerDes channels are operating can also be specified.
	Frequency (MHz) / Data Rate (Mbps)	• For EMIF application, this field represents the frequency of the memory clock (in MHz). • For GPIO Pin, this field represents the pin frequency. • For SerDes application, this field represents the max data rate (in Mbps). For example, 100 MHz clock with a 12.5% toggle rate means that each IO pin toggles 12.5 million times per second (100Mhz × 12.5%)
	Interface Rate	Specifies the interface data rate, the clock ratio between the external interface to the FPGA.

continued...

Column Heading		Description
		• For GPIO applications, this field indicates whether I/O value changes once (Single Data Rate) or twice (Double Data Rate). • For SerDes applications, this field represents the serialization factor, or the number of parallel data bits for each serial data bit. • For EMIF applications, this field only supports full-rate (1), half-rate (2), or quarter-rate (4).
	Toggle %	Percentage of clock cycles when the I/O signal changes value. This value is multiplied by clock frequency to determine the number of transitions per second. If DDR is selected, the toggle rate is multiplied by an additional factor of two.
	Write Enable %	When Input Termination is set to **OFF**, enter the average percentage of time that: • Output I/O is enabled • Bidirectional I/O is an output and enabled For EMIF applications where this field is enabled, enter the average percentage of time that the data lanes are sending write data. Input Termination is set to **ON**, enter the average percentage of time that On-Chip Termination is not active.
	Read Enable %	Enter the average percentage of time that: • Output I/O is enabled • Bidirectional I/O is an output and enabled For EMIF applications where this field is enabled, enter the average percentage of time that the data lanes are receiving read data. *Note:* If you are using Agilex 5 or Agilex 7 M-Series devices, you can modify this field for all applications except HVIO.
	Registered	Indicates whether the application is registered or not.
Memory IP Parameters	DQ Width	Enter the number of DQ pins in this module.
	Data Lanes	Enter the number of I/O lanes used as data lanes in this module. You must first specify the number of DQ pins, to enable this field.
	A/C Lanes	Enter the number of I/O lanes used as address/command lanes in this module.
I/O Analog Settings	I/O Standard	Specifies the I/O standard used by the I/O pins in this module.
	Input Termination	Specifies the input termination setting for the input and bidirectional pins in this module.
	Current Strength/ Output Termination	Specifies the current strength or output termination setting for the output and bidirectional pins in this module. Current strength and output termination are mutually exclusive.
	Slew Rate	Specifies the slew rate setting for the output and bidirectional pins in this module. Using a lower slew rate setting helps reduce switching noise but may increase delay.
	V_{OD} Setting	Specifies the differential output voltage (V_{OD}) for the output and bidirectional pins in the module. A smaller number indicates a smaller V_{OD}, which reduces static power.
	Programmable De-Emphasis	Specifies the de-emphasis setting for the output and bidirectional pins in this module. A larger number indicates a smaller pre-emphasis, which reduces dynamic power.
	Load (pF)	Specifies pin loading external to the chip (in pF). Applies only to outputs and bidirectional pins. Pin and package capacitance is already included in the I/O model. Include only off-chip capacitance.
Power (W)	Digital	Power dissipated in the digital domain of the I/O-subsystem including GPIO, EMIF controller, and SerDes controller.

continued...

Column Heading		Description
	Analog	Power dissipated in the analog domain of the I/O-subsystem, for example, I/O buffers.
	Total	Specifies the total power dissipation (in W). Sum of analog and digital power.
User Comments		Enter any comments. This is an optional entry.

Figure 46. I/O Page of the Intel FPGA PTC for Stratix 10 Devices

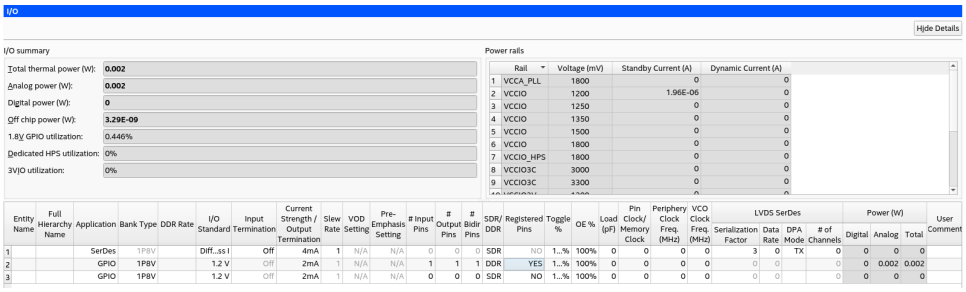


Table 19. I/O Page Information for Stratix 10 Devices

Column Heading	Description
Entity Name	Specify a name for the I/O in this column. This is an optional value.
Full Hierarchy Name	Specify the hierarchical path relevant to this entry. This is an optional entry. When entering levels of hierarchy, the pipe character (|) denotes a level of hierarchy.
Application	Specify the application for this I/O row. GPIO and SerDes interfaces can be instantiated using this field. Use the IP Wizard to instantiate external memory interface (EMIF) interfaces.
Bank Type	Specifies the type of I/O bank for this row. • 1P8V banks support I/O standards up to 1.8V as well as LVDS I/O standards. • 3VIO banks support CMOS I/O standards up to 3.0V. • HPS banks include dedicated HPS pins. • HPS-1P8V banks are similar to 1P8V banks in terms of supported I/O standards; these banks can serve as either general purpose I/Os or as EMIF interfaces in HPS applications.
DDR Rate	Specifies the clock rate of PHY logic. Determines the clock frequency of PHY logic in relation to the memory clock frequency. For example, if the memory clock sent from the FPGA to the memory device is toggling at 800MHz, a "Quarter Rate" interface means that the PHY logic in the FPGA runs at 200MHz.
I/O Standard	Specifies the I/O standard used by the I/O pins in this module.
Input Termination	Specifies the input termination setting for the input and bidirectional pins in this module.
Current Strength/ Output Termination	Specifies the current strength or output termination setting for the output and bidirectional pins in this module. Current strength and output termination are mutually exclusive.
Slew Rate	Specifies the slew rate setting for the output and bidirectional pins in this module. Using a lower slew rate setting helps reduce switching noise but may increase delay.
V_{OD} Setting	Specifies the differential output voltage (V_{OD}) for the output and bidirectional pins in the module. A smaller number indicates a smaller V_{OD}, which reduces static power.
Pre-Emphasis Setting	Specifies the pre-emphasis setting for the output and bidirectional pins in this module. A smaller number indicates a smaller pre-emphasis, which reduces dynamic power.

continued...

Column Heading		Description
# Input Pins		Specifies the number of input-only I/O pins in this module. Differential pin pairs count as one pin.
# Output Pins		Specifies the number of output-only I/O pins in this module. Differential pin pairs count as one pin.
# Bidir Pins		Specifies the number of bidirectional I/O pins in this module. Differential pin pairs count as one pin. The I/O pin is treated as an output when its output enable signal is active and is treated as an input when the output enable signal is disabled. An I/O pin configured as a bidirectional pin, but used only as an output, consumes more power than if it were configured as an output-only pin, due to the toggling of the input buffer every time the output buffer toggles (they share a common pin).
SDR/DDR		Indicates whether I/O value changes once (Single Data Rate) or twice (Double Data Rate) For GPIO and SerDes applications.
Registered Pins		Indicates whether the application is registered or not.
Toggle %		Percentage of clock cycles when the I/O signal changes value. This value is multiplied by clock frequency to determine the number of transitions per second. If DDR is selected, the toggle rate is multiplied by an additional factor of two.
OE %		For modules with Input Termination set to **OFF**, enter the average percentage of time that: • Output I/O is enabled • Bidirectional I/O is an output and enabled During the remaining time: • Output I/O is tri-stated • Bidirectional I/O is an input Input Termination cannot be active while the Output I/O is enabled, so for modules with Input Termination not set to **OFF**, enter the average percentage of time that On-Chip Termination is inactive (that is 1-percentage that the On-Chip Termination is active). This number must be a percentage between 0% and 100%.
Load (pF)		Specifies pin loading external to the chip (in pF). Applies only to outputs and bidirectional pins. Pin and package capacitance is already included in the I/O model. Include only off-chip capacitance.
Pin Clock / Memory Clock Freq (MHz)		Clock frequency (in MHz). For example, 100 MHz with a 12.5% toggle percentage means that each I/O pin toggles 12.5 million times per second (100 MHz * 12.5%).
Periphery Clock Freq (MHz)		The I/O subsystem internal PHY clock frequency. This is an output-only field. • In SerDes applications, the PHY clock frequency is a function of the SerDes rate and serialization factor. • In external memory interface (EMIF) applications, the PHY clock frequency is a function of the memory clock frequency and DDR rate of the EMIF IP.
VCO Clock Freq (MHz)		The internal VCO operating frequency. This is an output-only field. • In SerDes applications, VCO frequency is a function of SerDes Data rate. • In external memory interface (EMIF) applications, the VCO frequency is a function of the memory clock frequency of the EMIF IP. • In GPIO mode, the VCO frequency is not applicable.
LVDS SerDes	Serialization Factor	Number of parallel data bits for each serial data bit. Used for SerDes-DPA.
	Data Rate (Mbps)	The maximum data rate of the SerDes channels in Mbps.
	Mode	The DPA mode in which the SerDes channels are operating.
	# of Channels	The number of channels running at the data rate of this SerDes domain.
Power (W)	Digital	Power dissipated in the digital domain of the I/O-subsystem including GPIO, EMIF controller and SerDes controller.

continued...

Column Heading		Description
	Analog	Power dissipated in the analog domain of the I/O-subsystem, for example, I/O buffers.
	Total	Specifies the total power dissipation (in W). Sum of analog and digital power.
User Comments		Enter any comments. This is an optional entry.

For more information about the I/O standard termination schemes, refer to *I/O and High Speed I/Os in Agilex 7 Devices*.

Related Information

- Agilex 7 General-Purpose I/O User Guide: F-Series and I-Series
- Agilex 7 General-Purpose I/O User Guide: M-Series

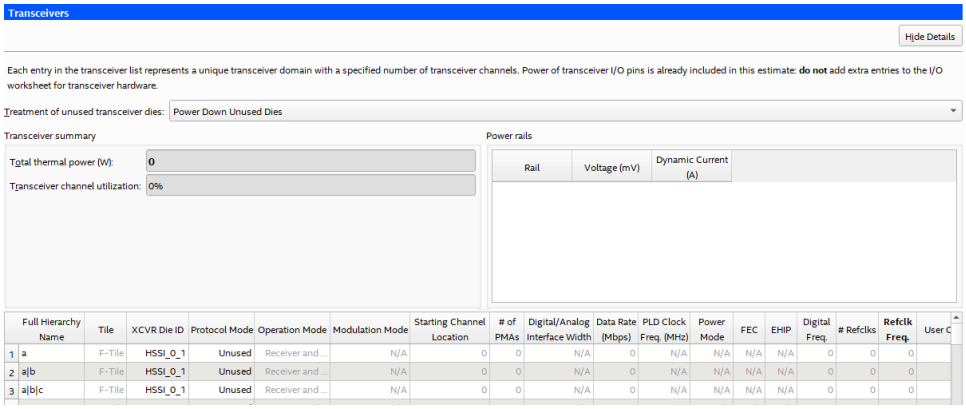
4.10. Intel FPGA PTC - Transceiver Page

The **Transceiver** data entry page of the Intel FPGA Power and Thermal Calculator (PTC) allows you to enter transceiver resources and their settings for all modules in your design. The power of transceiver I/O pins is included on this page.

Table 20. General Settings in the Transceiver Page

Input Parameter	Description
Total Thermal Power (W)	Total power dissipated in all modules on this page (in watts).
Treatment of unused transceivers (Agilex FPGA portfolio Designs Only)	For Agilex FPGA portfolio device designs, specifies how unused transceivers, or used transceivers with unused channels, should be treated. The following options are available: • **Power Down Unused Transceivers**—the power rails of unused transceivers are set to 0V. Not applicable to devices with P-tile and E-tile. • **Power Up Unused Transceivers**—the power rails of unused transceivers are set to a non-zero voltage. • **Preserve Unused Channels on Used and Unused Transceivers**—the power rails of unused transceivers are set to a non-zero voltage and all unused PMA lanes on transceivers are preserved. Selecting **Preserve Unused Channels on Used and Unused Transceivers** results in the same behavior on the tiles as using the following global `.qsf` assignment: `set_global_assignment -name PRESERVE_UNUSED_XCVR_CHANNEL ON`
Treatment of Unused HSSI Dies (Stratix 10 Designs Only)	For Stratix 10 devices, if you use no transceiver channels or PLLs on an HSSI die, you can power down the die or the die can remain powered. You can select the voltage of unused dies that are powered to minimize static power, or to minimize the number of power supply voltages required. For example, if active H-tile transceiver channels use VCCR_GXB=1.12V, selecting **Minimize Leakage** assumes that the unused-but-powered H-tile dies use VCCR_GXB=1.03V, which is the lowest supported voltage, thus minimizing leakage. Selecting **Minimize Number of Supply Voltages** assumes that the unused-but-powered banks use VCCR_GXB=1.12V, which is the voltage used by active channels, thus eliminating the need for the 1.03V power supply on VCCR_GXB. The Intel FPGA PTC uses information in the **XCVR Die ID**, **Starting Channel Location**, and **# of Channels** columns on the **XCVR** page, along with the **# PLL Blocks** and **XCVR Die ID** columns on the **PLL** page to determine whether dies are actively used. This setting does not apply to E-tile nor P-tile transceivers, because these transceiver dies can never be powered down.

Figure 47. Transceiver Page of the Intel FPGA PTC (For Stratix 10 Designs Only)



Each row in the Transceiver page represents a separate transceiver domain. Enter the following parameters for each transceiver domain:

Table 21. Transceiver Page Information (For Stratix 10 Designs Only)

Column Heading	Description
Entity Name	Specifies a name for the entity. This is an optional value.
Full Hierarchy Name	Specify the hierarchical path relevant to this entry. This is an optional entry. When entering levels of hierarchy, the pipe character (|) denotes a level of hierarchy.
Tile	Specifies the type of transceiver die on which transceiver channels are located. Some devices may include more than one type of transceiver die. This field changes depending on the device options that you choose on the **Main** page.
XCVR Die ID	Specify the transceiver die on which transceiver channels on this row are located.
Protocol Mode	Specifies the mode in which the PCS, HIP, and PCIE blocks operate. This mode depends on the XCVR tile and the communication protocol or standard that the channels on this row implement.
Operation Mode	Specifies whether the hardware is configured in full duplex transceiver mode (receiver and transmitter), Receiver Only mode, or Transmitter Only mode. Allowed values depend on the selected tile and protocol mode.
Modulation Mode	Specify the data modulation mode of transceiver channels. This field is applicable only to E-Tile transceivers. When you select *High Data Rate PAM4* for this field, 2 physical channels are paired to represent 1 logical channel. When specifying # of Channels, enter the number of physical channels (that is, in multiples of 2).
Starting Channel Location	Specify the starting location within the die for the channels specified in this row. For example, if a given row contains 3 channels, and starting location is specified to be 12, channels are assumed to be in locations 12, 13, and 14. Location 0 denotes the bottom-most channel on the transceiver die.
# of PMAs	Specifies the number of physical medium attachments (PMAs) used in this transceiver domain. Each row represents one transceiver domain. These PMAs are grouped together in one transceiver bank, or two or more adjacent transceiver banks and clocked by one or more common transmitter PLLs. For E-tile transceivers, if the selected modulation mode is *High Data Rate PAM4*, enter 2 physical channels to represent 1 logical channel. (Agilex 7 devices only.) For F-tile transceivers: • Each PMA with a Digital/Analog Interface Width of less than 40 uses 1 stream. • Each PMA with a Digital/Analog Interface Width of 60 uses 2 streams. • Each PMA with a Digital/Analog Interface Width of 128 uses 4 streams.

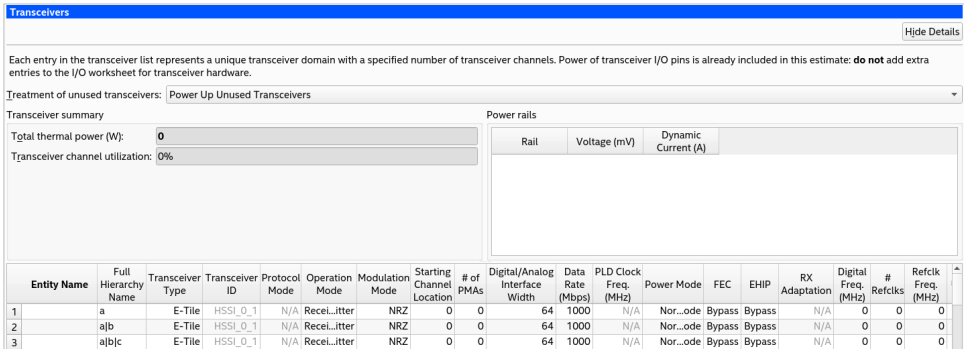
continued...

Column Heading	Description
	For more information about PMAs and streams, refer to the F-tile Architecture and PMA and FEC Direct PHY IP User Guide.
# of Channels	Specifies the number of channels used in this transceiver domain. Each row represents one transceiver domain. These channels are grouped together in one transceiver bank, or two or more adjacent transceiver banks and clocked by one or more common transmitter PLLs. For E-tile transceivers, if the selected modulation mode is *High Data Rate PAM4*, enter 2 physical channels to represent 1 logical channel. (Stratix 10 devices only.)
Digital/Analog Interface Width	Specify the width of the parallel data bus between PCS and PMA. For E-tile PMA Direct, set to PMA parallel data width, even if FPGA FIFO widens the interface. As an example, for 25 Gbps PMA Direct you would typically set this value to 32. When the FEC or EHIP is used, you would set this value to 32 for NRZ mode and 64 for PAM4 mode.
Data Rate (Mbps)	Specifies the data rate (in Mbps) for the transceiver. Allowed values depend on the selected protocol mode and selected device.
PLD Clock Frequency (MHz)	Specifies the PLD clock frequency. This is applicable only to P-tile transceivers, and when the selected protocol is PCIe gen4.
Power Mode	E-tile transceivers can operate at either Normal Power Mode or Low Power Mode. For thermal analysis and regulator sizing, you must set the E-tile transceivers in the Normal Power Mode, because your board design must take into consideration the maximum power conditions. Refer to the E-tile Transceiver PHY User Guide for information on how to switch transceivers from Normal Power Mode to Low Power Mode.
FEC	Specify the Forward Error Correction setting. This field is applicable only to E-Tile transceivers.
EHIP	Specify the Ethernet Hard IP protocol. This field is applicable only to E-Tile and F-Tile transceivers.
Digital Frequency (MHz)	Specify the digital frequency at which the digital portion of the transceiver (including FEC and EHIP) operates. This field is applicable only to E-tile transceivers.
# Refclks	Specify the number of reference clocks in use. If another interface on this tile is using the same reference clock, and you have already entered this clock in another row, enter 0 in this row to avoid double counting. This field is applicable only to E-Tile transceivers.
Refclk Frequency (MHz)	Specify the reference clock frequency. This field is applicable only to E-Tile and F-Tile transceivers.
Application	Specify the application type, which determines values for advanced channel options. Select Custom to enable manual editing of advanced channel options for the current row. This field is applicable only to L-tile and H-tile transceivers.
V_{CCR_GXB} and V_{CCT_GXB} Voltage	Specifies the voltage of the V_{CCR_GXB} and V_{CCT_GXB} rails. Allowed values depend on the selected device and selected data rate. This field is applicable only to L-tile and H-tile transceivers.
V_{OD} Setting	The output differential voltage (V_{OD}) setting of the transmitter channel PMA. To enable this setting, select **Custom** in the **Application** column. This field is applicable only to L-tile and H-tile transceivers.
V_{OD} Voltage	The output differential voltage (V_{OD}) of the transmitter channel PMA (in mV). This voltage depends on the V_{OD} setting and the V_{CCT_GXB} voltage. This field is applicable only to L-tile and H-tile transceivers.
First Pre-Tap	Specifies the pre-emphasis setting used by the transmitter channel PMA. Set to Off if the tap value is 0; otherwise, set to On. If pre-emphasis settings are set to On, power consumption does not depend on the magnitude nor the sign (positive or negative) of individual taps. To enable these settings, select **Custom** in the **Application** column.
First Post-Tap	
DFE	Specify mode of the decision feedback equalizer (DFE). Allowed values depend on the selected data rate. To enable this setting, select **Custom** in the **Application** column. This field is applicable only to L-tile and H-tile transceivers.

continued...

Column Heading	Description
Adaptation	Specify if the adaptation feature is used. This option should be enabled if the channels use either CTLE adaptation or DFE adaptation. To enable this setting, select **Custom** in the **Application** column. This field is applicable only to L-tile and H-tile transceivers.
Transmitter High-Speed Compensation	Specifies if the power distribution network (PDN) induced inter-symbol interference (ISI) compensation is enabled in the TX driver. To enable this setting, select **Custom** in the **Application** column. This field is applicable only to L-tile and H-tile transceivers.
User Comments	Enter any comments. This is an optional entry.

Figure 48. Transceiver Page of the Intel FPGA PTC (For Agilex FPGA Portfolio Designs Only)



Each row in the Transceiver page represents a separate transceiver domain. Enter the following parameters for each transceiver domain:

Table 22. Transceiver Page Information (For Agilex Designs Only)

Column Heading	Description
Entity Name	Specifies a name for the entity. This is an optional value.
Full Hierarchy Name	Specify the hierarchical path relevant to this entry. This is an optional entry. When entering levels of hierarchy, the pipe character (|) denotes a level of hierarchy.
Transceiver Type	Specifies the type of transceiver on which transceiver channels are located. Some devices may include more than one type of transceiver. This field changes depending on the device options that you choose on the **Main** page.
Transceiver ID	Specify the transceiver on which transceiver channels on this row are located. The first index indicates bottom (0), middle (1) or top (2), and the second index indicates right (0) or left (1), in package top view with pin A1 at the top-left. For example, HSSI_0_0 is placed at the bottom-right of the package, and HSSI_2_1 is placed at the top-left.
Protocol Mode	Specifies the mode in which the PCS, HIP, and UPI blocks operate. This mode depends on the transceiver and the communication protocol or standard that the channels on this row implement.
Operation Mode	Specifies whether the hardware is configured in full duplex transceiver mode (receiver and transmitter), Receiver Only mode, or Transmitter Only mode. Allowed values depend on the selected transceiver type and protocol mode.
Modulation Mode	Specify the data modulation mode of transceiver channels. When you select *High Data Rate PAM4* for this field, two physical channels are paired to represent one logical channel. When specifying the number of channels, enter the number of physical channels (that is, in multiples of 2). This field is applicable only to E-Tile and F-Tile transceivers.

continued...

Column Heading	Description
Starting Channel Location	Specify the starting location within the transceiver for the channels specified in this row. For example, if a given row contains three channels, and starting location is specified to be 12, channels are assumed to be in locations 12, 13, and 14. Location 0 denotes the bottom-most channel on the transceivers.
# of PMAs	Specifies the number of physical medium attachments (PMAs) used in this transceiver domain. Each row represents one transceiver domain. These PMAs are grouped together in one transceiver bank, or two or more adjacent transceiver banks and clocked by one or more common transmitter PLLs. For E-tile transceivers, if the selected modulation mode is *High Data Rate PAM4*, enter two physical channels to represent one logical channel. For F-tile transceivers: • Each PMA with a PCS/PMA Interface width of less than 40 uses one stream. • Each PMA with a PCS/PMA Interface width of 64 uses two streams. • Each PMA with a PCS/PMA Interface width of 128 uses four streams. For more information about PMAs and streams, refer to the F-tile Architecture and PMA and FEC Direct PHY IP User Guide.
Digital/Analog Interface Width	Specifies the width of the parallel data bus between PCS and PMA. For E-tile, F-Tile, and GTS transceiver PMA Direct, set to PMA parallel data width, even if FPGA FIFO widens the interface. As an example, for 25 Gbps PMA Direct, you would typically set this value to 32. When the FEC or EHIP is used, you would set this value to 32 for NRZ mode and 64 for PAM4 mode.
Data Rate (Mbps)	Specifies the data rate (in Mbps) for the transceiver. Allowed values depend on the selected protocol mode and selected device.
PLD Clock Frequency (MHz)	Specifies the PLD clock frequency. This is applicable only to P-tile transceivers, and when the selected protocol is PCIe gen4.
Power Mode	E-tile transceivers can operate at either Normal Power Mode or Low Power Mode. For thermal analysis and regulator sizing, you must set the E-tile transceivers in the Normal Power Mode, because your board design must take into consideration the maximum power conditions. Refer to the E-tile Transceiver PHY User Guide for information on how to switch transceivers from Normal Power Mode to Low Power Mode.
FEC	Specify the Forward Error Correction setting. This field is applicable only to E-Tile, F-Tile, and GTS transceivers.
EHIP	Specify the Ethernet Hard IP protocol. This field is applicable only to E-Tile, F-Tile, and GTS transceivers.
RX Adaptation	Specify if RX auto adaptation must be enabled.
Digital Frequency (MHz)	Specify the digital frequency that the digital portion of the transceiver (including FEC and EHIP) operates at (in MHz). Typically, this value is equal to data rate (in Mbps) divided by 64 for E-Tile, or divided by 32 for F-Tile and GTS transceiver. For example, for data rate of 25781.25 Mbps, typical digital frequency is 402.8 MHz (25781.25/64 = 402.8) for E-Tile, or 805.7 MHz (25781.25/32 = 805.7) for F-Tile and GTS transceiver. This frequency has a minimum requirement of data rate (in Mbps) divided by 2 * PCS/PMA interface width for E-Tile, or divided by PCS/PMA interface width for F-Tile and GTS transceiver. For example, for data rate of 25781.25 Mbps and interface width of 64, the minimum digital frequency is 201.4 MHz (25781.25/(2*64) = 201.4) for E-Tile, or 402.8 MHz (25781.25/64 = 402.8) for F-Tile and GTS transceiver.
# Refclks	Specify the number of reference clocks in use. If another interface on this transceiver is using the same reference clock, and you have already entered this clock in another row, enter 0 in this row to avoid double counting.
Refclk Frequency (MHz)	Specify the reference clock frequency. This field is applicable only to E-Tile and F-Tile transceivers.
User Comments	Enter any comments. This is an optional entry.

For more information about the transceiver architecture of the supported device families, refer to the appropriate *Transceiver PHY User Guide* for Agilex FPGA portfolio devices.

Related Information

- E-Tile Transceiver PHY User Guide
- L- and H-Tile Transceiver PHY User Guide

4.10.1. Estimating E-Tile Channel PLL Power with the Intel Power and Thermal Calculator

You can estimate E-tile channel PLL power for Stratix 10 devices, by adding a Transmitter-only row to the **Transceiver** page of the Intel FPGA Power and Thermal Calculator (PTC).

The following three examples illustrate the Intel FPGA PTC configuration for various E-tile channel PLL requirements.

Table 23. E-Tile Channel PLL configured for: Reference clock = 200MHz, pll_clkout1 = 800MHz, pll_clkout2 = 400MHz

Operation Mode	Data Rate	Digital/ Analog Width	Power Mode	FEC	EHIP	Modulation	Digital Freq	# Refclks	Refclk Freq	VOD
Transmitter Only	12800	16	Normal Power	Bypass	Bypass	NRZ	0	1	200	0

Table 24. E-Tile Channel PLL configured for: Reference clock = 125MHz, pll_clkout1 = 500MHz, pll_clkout2 = 250MHz

Operation Mode	Data Rate	Digital/ Analog Width	Power Mode	FEC	EHIP	Modulation	Digital Freq	# Refclks	Refclk Freq	VOD
Transmitter Only	8000	16	Normal Power	Bypass	Bypass	NRZ	0	1	125	0

Table 25. E-Tile Channel PLL configured for: Reference clock = 307MHz, pll_clkout1 = 491MHz, pll_clkout2 = 245MHz

Operation Mode	Data Rate	Digital/ Analog Width	Power Mode	FEC	EHIP	Modulation	Digital Freq	# Refclks	Refclk Freq	VOD
Transmitter Only	19660.8	40	Normal Power	Bypass	Bypass	NRZ	0	1	307	0

Alternatively, you can instantiate an E-Tile Transceiver-native PHY IP in PLL mode in your Quartus Prime project, compile the project, and view the configuration in the Intel FPGA PTC.

Related Information

E-Tile Transceiver PHY User Guide

4.11. Intel FPGA PTC - HPS Page

The **HPS** data entry page of the Intel FPGA Power and Thermal Calculator (PTC) applies to devices with HPS.

To enable parameter entry into the **HPS** page, first select a device that supports HPS in the **Main** page or in **Device Selection**, then turn **ON** the **HPS System Switch** in the **HPS** page. For Stratix 10 devices, select your peripheral modules in the **I/O-IP** page.

Figure 49. HPS Page of the Intel FPGA PTC

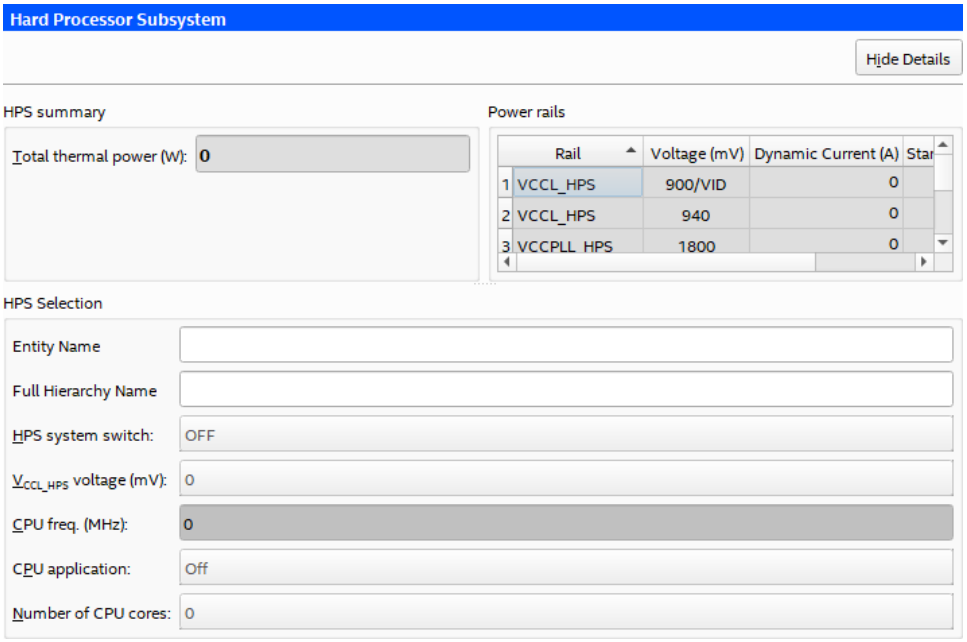


Table 26. HPS Input Parameter Information

Input Parameter	Description
Entity Name	Specifies a name for the entity. This is an optional value.
Full Hierarchy Name	Specify the hierarchical path relevant to this entry. This is an optional entry. When entering levels of hierarchy, the pipe character (|) denotes a level of hierarchy.
HPS System Switch	Turns the HPS system on or off. This selection affects the static power.
VCCL_HPS Voltage (mV)	Specifies the core HPS voltage (in mV).

Table 27. CPU Parameters on the HPS Page

Parameters	Description
CPU Freq. (MHz)	Specifies the operating frequency of all CPUs (in MHz).
CPU Application	Select a benchmark application representative of the application running on the CPUs.
Number of CPU Cores	Specifies the number of cores in the CPU running the selected application.

Related Information

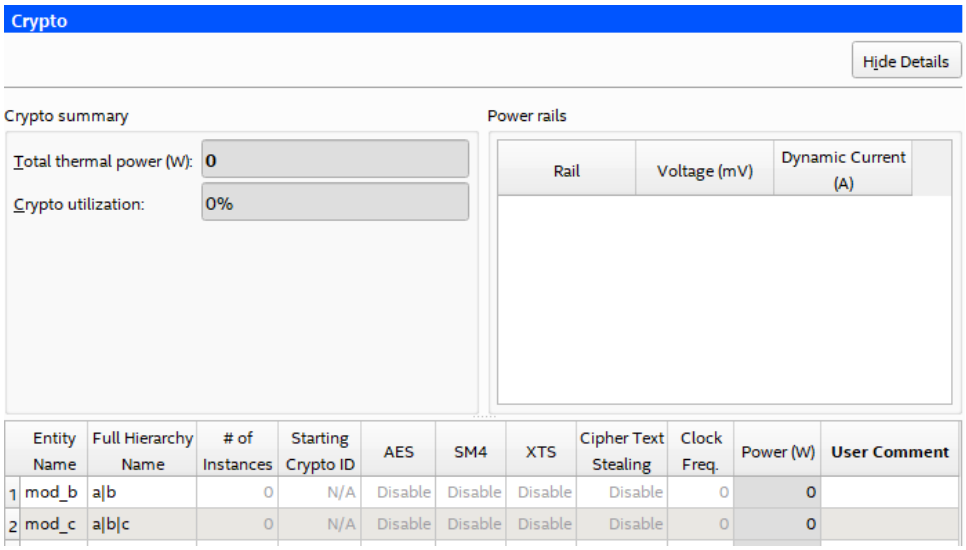
- Agilex 7 General-Purpose I/O User Guide: F-Series and I-Series
- Agilex 7 General-Purpose I/O User Guide: M-Series

4.12. Intel FPGA PTC - Crypto Page

The **Crypto** data entry page is only for Agilex 7 devices with crypto blocks. Only a subset of Agilex 7 devices have crypto blocks, consisting of hardened logic that can perform encryption and decryption functions. The **Crypto** data entry page of the Intel FPGA Power and Thermal Calculator (PTC) allows you to configure crypto blocks for Agilex 7 devices equipped with those blocks, and to obtain power estimates for crypto use.

Note: Not all Agilex 7 devices have crypto blocks. Parameter entry is unavailable if the currently selected device does not have crypto blocks.

Figure 50. Crypto Page of the Intel FPGA PTC



Crypto Summary

Column Heading	Description
Total thermal power (W)	Reports the total thermal power of the crypto blocks in watts (W).
Crypto utilization	Reports the percentage utilization of the crypto block resources.

Crypto Page Information

Column Heading	Description
Entity Name	Specify a name for each entity in the design. This is an optional value.
Full Hierarchy Name	Specify the hierarchical path relevant to this entry. This is an optional entry. When entering levels of hierarchy, the pipe character (|) denotes a level of hierarchy.
# of Instances	Enter the number of crypto block instances with the same parameters.

continued...

Column Heading	Description
Starting Crypto ID	Specify placement information for thermal modeling. This field is available only when **# of Instances** is set to 1.
AES	Specify whether to enable or disable Advanced Encryption Standard (AES) for the crypto block.
SM4	Specify whether to enable or disable SM4 (a block cipher used to encrypt and decrypt data) for the crypto block.
XTS	Specify whether to enable or disable XEX Tweakable Block Ciphertext Stealing (a block cipher mode of operation, abbreviated as XTS) for the crypto block.
Cipher Text Stealing	Specify whether to enable or disable Cipher Text Stealing (CTS) for the crypto block. CTS can be enabled only if XTS is also enabled.
Clock Freq (MHz)	Specify the frequency of the clock, in MHz.
Total Power (W)	Indicates the total estimated power for this row, in watts (W).
User Comment	Enter any comments. This is an optional entry.

Related Information

Agilex 7 FPGAs and SoCs Device Overview

4.13. Intel FPGA PTC - NOC Page

The NOC page of the Intel FPGA Power and Thermal Calculator (PTC) shows the power information relating to the network-on-chip IP.

To enable parameter entry into the NOC page, first select a device that supports NOC on the **Main** page or in **Device Selection**.

Note: Not all Agilex 7 devices have the NOC IP. Parameter entry is unavailable if the currently selected device does not have the NOC IP.

Figure 51. NOC Page of the Intel FPGA PTC

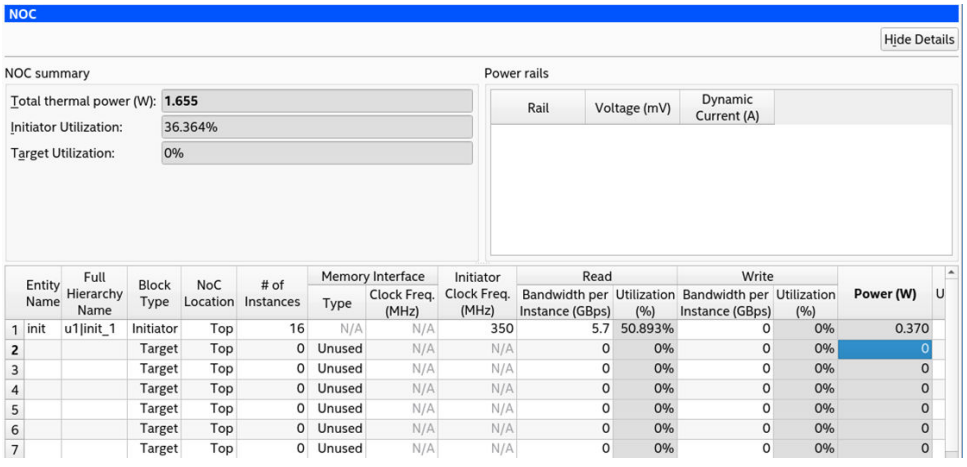


Table 28. NOC Page Information

Column Heading		Description
Entity Name		Specify a name for each entity of the design. This is an optional entry.
Full Hierarchy Name		Specify the hierarchical path relevant to this entry. This is an optional entry. When entering levels of hierarchy, the pipe character (|) denotes a level of hierarchy.
Block Type		Specify whether the block is of type Target or Initiator.
NoC Location		Specify whether the block is located at the Top or Bottom of the device.
# of Instances		Specify the number of instances of this element. A single NoC Initiator Intel FPGA IP may contain multiple initiator interfaces. Similarly, a target memory IP such as the High Bandwidth Memory (HBM2E) Interface FPGA IP may contain multiple target interfaces. This page only reflects the power usage of the NoC targets of IP such as the High Bandwidth Memory (HMB2E) Interface FPGA IP. Estimate the power for the remainder of this IP elsewhere within PTC, for example on the HBM page.
Memory Interface	Type	For target elements only. In the Type column, select between HBM for HBM2e memory or DDR for external memory interfaces implemented in GPIO-B blocks. In the Clock Freq. (MHz) column, enter the clock frequency for these target interfaces
	Clock Freq. (MHz)	
Initiator Clock Freq. (MHz)		For initiator elements only, enter the clock frequency the user interface for these initiators will operate at. If different initiators operate at different frequencies, they will need to be specified on separate rows.
Read	Bandwidth per Instance (GBps)	For both initiator and target elements. Specify read and write bandwidth in the Bandwidth per Instance (GBps). Initiator or target elements with different bandwidth requirements need to be specified on separate rows. The Utilization (%) displays the bandwidth utilization for each initiator or target. A warning is generated if the read bandwidth utilization and write bandwidth utilization add up to more than 100%.
	Utilization (%)	
Write	Bandwidth per Instance (GBps)	
	Utilization (%)	
Power (W)		Reports the power for the total initiators or targets specified on that row.
User Comments		Enter any comments. This is an optional entry.

Related Information

Agilex 7 M-Series FPGA Network-on-Chip (NoC) User Guide

4.14. Intel FPGA PTC - HBM Page

The **HBM** data entry page of the Intel FPGA Power and Thermal Calculator (PTC) shows the power information pertaining to high-bandwidth memory (HBM). This page is available for Agilex 7 M-series and Stratix 10 devices only.

Table 29. HBM Channel Configuration

Column Heading		Description
Entity Name		A user-editable field to name each entity of the design.
Full Hierarchy Name		Specify the hierarchical path relevant to this entry. This is an optional entry. When entering levels of hierarchy, the pipe character (|) denotes a level of hierarchy.
HBM ID		Select the top or bottom HBM stack in devices that include multiple stacks.

continued...

Column Heading		Description
Channel ID		Selects a particular die in the stack.
PC0 Traffic Pattern		Select the traffic pattern that most closely matches your application. (PC0 and PC1 refer to the two pseudo-channels that each physical channel [0-7] is divided into; you can select different traffic patterns for each pseudo-channel.) Intel Stratix 10 devices only.
PC1 Traffic Pattern		Select the traffic pattern that most closely matches your application. (PC0 and PC1 refer to the two pseudo-channels that each physical channel [0-7] is divided into; you can select different traffic patterns for each pseudo-channel.) Intel Stratix 10 devices only.
Pseudo channel 0	Read Rate %	Select to most closely match your application. Agilex 7 M-series devices only.
	Bandwidth %	
	Page Hit Rate %	
Pseudo channel 1	Read Rate %	Select to most closely match your application. Agilex 7 M-series devices only.
	Bandwidth %	
	Page Hit Rate %	
User Comment		User Comment field.

Figure 52. HBM Page of the Intel FPGA PTC (Stratix 10 Devices)

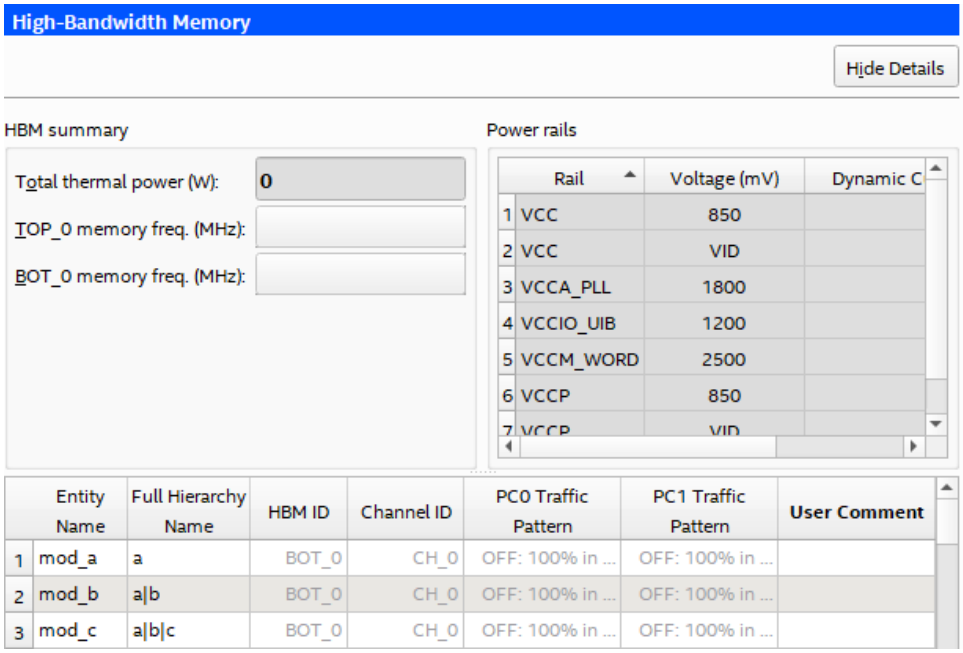
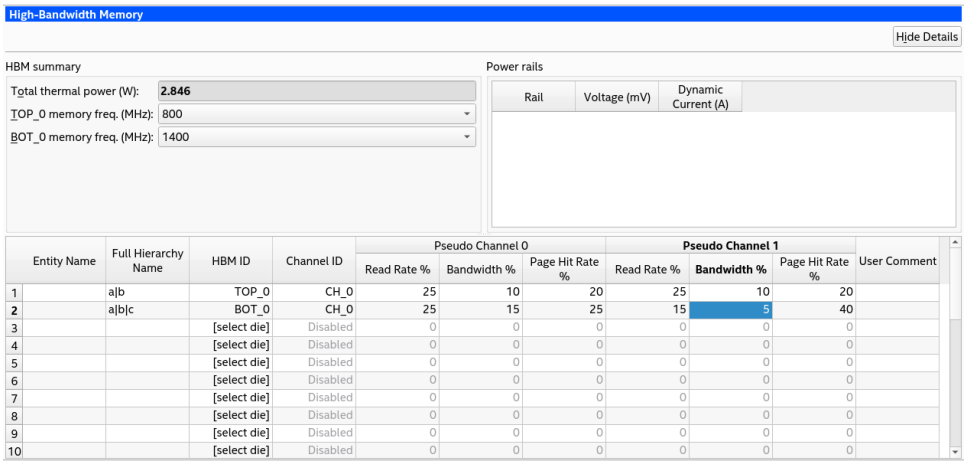


Figure 53. HBM Page of the Intel FPGA PTC (Agilex 7 M-series Devices)



Related Information

High Bandwidth Memory (HBM2E) Interface Agilex 7 M-Series FPGA IP User Guide

4.15. Intel FPGA PTC - Thermal Page

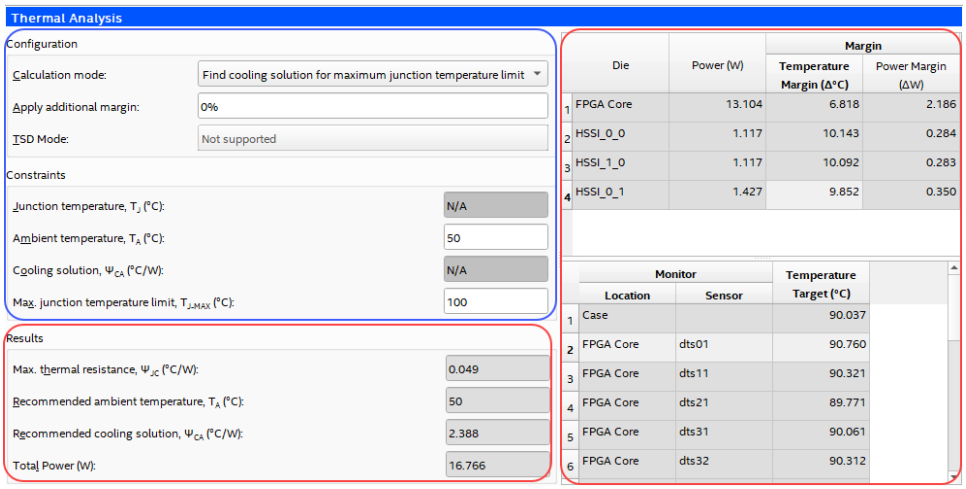
The **Thermal** data entry page of the Intel FPGA Power and Thermal Calculator (PTC) allows you to enter temperature requirements for your design and displays thermal power and thermal analysis information.

Note: To achieve correct power and thermal calculations, ensure that your design and all input values are entered accurately and correctly.

Thermal Page for Agilex FPGA Portfolio Devices

On the **Main** worksheet, verify that **Power Characteristics** is set to **Maximum**, and then select the desired **Calculation mode** from the drop-down menu on the **Main** or **Thermal** page.

Figure 54. Thermal Page of the Intel FPGA Power and Thermal Calculator—Agilex FPGA Portfolio Devices



In the above figure, input parameters are circled in blue and reporting fields are circled in red.

Table 30. Input Parameter Information

Parameter	Description
Calculation Mode	Specifies the calculation mode for the thermal solver to use. The available choices are: • **Use a constant junction temperature**. The Intel FPGA PTC assumes uniform temperature across the dies. If you choose this mode, you can enter the junction temperature on the **Main** page or on the **Thermal** page. *Note:* The power calculated in the **Use a constant junction temperature** mode is not representative of actual power during use. It is unlikely that all components of the die are at uniform temperature during normal operation. For more representative power, use the other calculation modes that utilize the thermal calculator. • **Find cooling solution for maximum junction temperature limit**. The Intel FPGA PTC finds the T_{case}, a cooling solution Ψ_{CA}, and the power of all dies, assuming that no die can exceed the specified maximum T_J. If you choose this mode, enter maximum T_J and ambient temperature values. • **Find available thermal margin for cooling solution**. The Intel FPGA PTC finds the thermal parameters for a known cooling solution and ambient temperature. If you choose this mode, enter values for the ambient temperature and Ψ_{CA}. • **Find ambient temperature for specified cooling solution**. The PTC finds the necessary ambient temperature for a given cooling solution and maximum T_J. If you choose this mode, Enter the Ψ_{CA} and the maximum T_J appropriate for the design. *Note:* To enable selection of non-constant calculation modes, the **Power characteristics** field in the **Device selection** group box of the **Main** page must be set to **Maximum**.
Apply Additional Margin	Specifies, as a percentage, the amount of additional margin to apply to detailed thermal analysis results. The default value is 0%. Valid values are 0-25%. The recommended margin for Agilex 5 and Agilex 7 devices is 10%. Consult your Intel Field Application Engineer (FAE) if you require additional guidance on margin power.

continued...

Parameter	Description
	Note: 1. Setting a non-zero margin causes the total power value on the **Thermal** page to be higher than the power reported elsewhere in the Intel FPGA PTC. 2. If you import a `.ptc` file from an earlier version of the Intel FPGA PTC, which has the **Apply Recommended Margin** parameter set to *Yes*, the current version of the Intel FPGA PTC interprets this as an **Apply Additional Margin** setting of 10%
TSD Mode	Indicates the method by which sensor temperatures are reported. This parameter has no effect on maximum junction temperature or temperature margin.
Junction temperature, T_J (°C)	Allows you to specify the junction temperature for all dies in the package. This field is available only when the selected **Calculation mode** is **Use a constant junction temperature**.
Ambient Temp, T_A (°C)	Allows you to specify the temperature of the air that is cooling the device.
Max. Junction Temp, $T_{J\text{-}MAX}$ (°C)	Allows you to specify the maximum junction temperature that no part of any die in the package should exceed.
Cooling Solution Ψ_{CA}(°C/W)	Allows you to specify the cooling solution when you have selected the **Use a constant junction temperature**, **Find available thermal margin for cooling solution**, or **Find ambient temperature for specified cooling solution** calculation mode.

Table 31. Max. Ψ_{JC} and Recommended Cooling Solution

Column Heading	Description
Max. Ψ_{JC}(°C/W)	Ψ_{JC} is the thermal resistance between each of the dies in the package and the center of the package integrated heat spreader. This field shows the maximum Ψ_{JC} among all dies, assuming the recommended Ψ_{CA} value below.
Recommended ambient Temperature T_A(°C)	T_A is the recommended ambient temperature for the recommended cooling solution.
Recommended cooling solution Ψ_{CA}(°C/W)	Ψ_{CA} is the thermal resistance between the center of the package integrated heat spreader (IHS) and ambient temperature. The recommended Ψ_{CA} is the highest possible thermal resistance of the cooling solution that ensures no part of any die exceeds the specified maximum junction temperature.
Total Power (W)	The total power consumption.

Table 32. Thermal Margin Report Table

Column Heading		Description
Die		The die for which margin is reported: • FPGA Core: The margin for the FPGA core. • HSSI_*x*_*y*: The margin for the specified high-speed serial interface (HSSI) die.
Power (W)		The thermal power dissipated by the specified die. This is the power used in the thermal analysis. *Note:* The power listed on the Thermal page is currently pessimistic; the overall total power reported does not match the total on-chip power dissipation on the Power Summary page.
Margin	Temperature (Δ°C)	The calculated temperature margin in °C for the specified die, relative to the maximum T_J.
	Power (ΔW)	The amount of power in watts that can be added to the specified die, before reaching its maximum T_J.

Temperature margins are calculated relative to a designated maximum junction temperature, T_J. It is possible that one or more dies may have zero temperature margin, because the solution is calculated for that maximum T_J. The calculated power margins indicate the power buffer available before the maximum T_J is exceeded, assuming the same cooling conditions. The calculated power value provides only an approximate estimate of power that can be added to the specific die before reaching its maximum T_J. The actual margin depends on the specific subsystem to which the power is added. Note that any increase or decrease in power changes the required cooling solution.

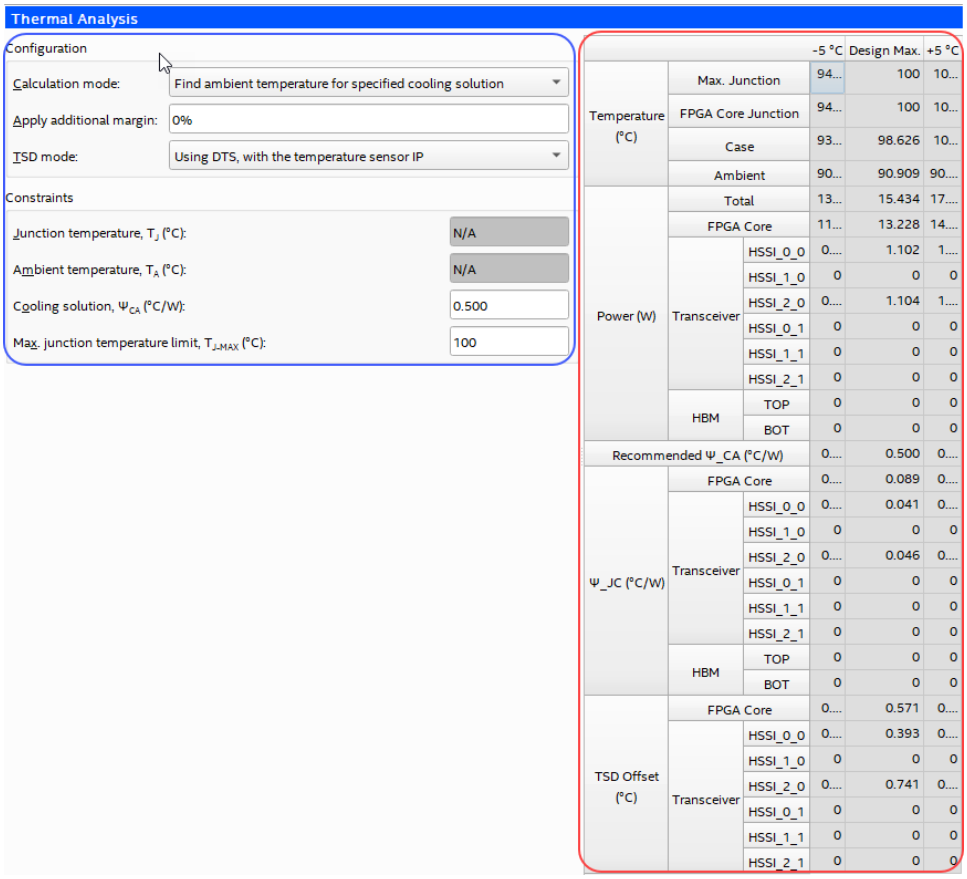
Table 33. Temperature Target Report Table

Column Heading		Description
Monitor	Location	The die for which the temperature is reported: • Case: The temperature at the center of the FPGA lid. • FPGA Core: The temperature at the specified sensor on the FPGA core. • HSSI_*x*_*y*: The temperature of the specified high-speed serial interface (HSSI) die.
	Sensor	The digital thermal sensor (DTS) or thermal diode (TD) sensor reporting the temperature.
Temperature Target (°C)		The calculated temperature for the target location and sensor, when the system is operating.

The monitor sensors report FPGA temperatures at the specified locations when the system is operating. These sensors may not necessarily be at the hottest locations on the die, and therefore can report values that are lower than the actual maximums in the design.

Thermal Page for Stratix 10 Devices

Figure 55. Thermal Page of the Intel FPGA PTC — Stratix 10 Devices



In the above figure, input parameters are circled in blue and reporting fields are circled in red.

Table 34. Input Parameter Information

Parameter Name	Description
Calculation Mode	Specifies the calculation mode for the thermal solver to use. *Note:* To enable selection of non-constant calculation modes, the **Power characteristics** field in the **Device selection** group box of the **Main** page must be set to **Maximum**.
Apply Additional Margin	Specifies as a percentage, the amount of additional margin to apply to detailed thermal analysis results. The default value is 0%. Valid values are 0–25%. The recommended margin for Stratix 10 devices is 25%. Consult your Intel Field Application Engineer (FAE) if you require additional guidance on margin power.

continued...

Parameter Name	Description
	Note: 1. Setting a non-zero margin causes the total power value on the **Thermal** page to be higher than the power reported elsewhere in the Intel FPGA PTC. 2. If you import a `.ptc` file from an earlier version of the Intel FPGA PTC, which has the **Apply Recommended Margin** parameter set to *Yes*, the current version of the PTC interprets this as an **Apply Additional Margin** setting of 25%.
TSD Mode	Specify the method by which offset temperatures are provided—such as from a thermal diode, or a digital temperature sensing mechanism.
Junction temperature, T_J (°C)	Specify the junction temperature for all dies in the package. This field applies only when the selected **Calculation mode** value is **Use a constant junction temperature**.
Ambient Temp, T_A (°C)	Specify the temperature of the air that is cooling the device.
Max. Junction Temp, $T_{J\text{-}MAX}$ (°C)	Specify the maximum junction temperature that no part of any die in the package should exceed.
Cooling Solution Ψ_{CA}(°C/W)	ψ_{CA} is the thermal resistance between the center of the package integrated heat spreader (IHS) and ambient temperature. The recommended Ψ_{CA} is the highest possible thermal resistance of the cooling solution that ensures no part of any die exceeds the specified maximum junction temperature.
Max. Ψ_{JC}(°C/W)	ψ_{JC} is the thermal resistance between each of the dies in the package and the center of the package integrated heat spreader. This field shows the maximum Ψ_{JC} among all dies, assuming the recommended Ψ_{CA} value above.

Table 35. Temperature (°C)

Row Name	Description
Max. Junction	The maximum junction temperature that no part of any die in the package should exceed.
FPGA Core Junction	The maximum junction temperature that no part of any die in the package should exceed.
Case	The case temperature, which is the temperature at the top center of the integrated heat spreader, assuming the recommended Ψ_{CA} value listed above.
Ambient	The temperature of the air that is cooling the device.

Table 36. Power (W)

Row Name		Description
Total		Provides total power consumption of all dies in the package.
FPGA Core		The total thermal power consumption of the main FPGA die containing core logic, assuming the recommended Ψ_{CA} value. This power is reported at the actual temperature of the core die, assuming the recommended Ψ_{CA} value. This temperature may be equal to the maximum junction temperature if the FPGA core die is at the highest temperature among all dies (also known as a hot spot). The FPGA core may also be at a lower temperature, if the hot spot is elsewhere in the package (i.e. on another die).
Transceiver	HSSI_0_0	The total power consumption of HSSI_0_0, assuming the recommended Ψ_{CA} value. This power is reported at the actual temperature of the specific die, assuming the recommended Ψ_{CA} value above. This temperature may be equal to the maximum junction temperature if a specific die is the hot spot, or it may be at a lower temperature if the hot spot is elsewhere in the package.
	HSSI_1_0	
	HSSI_2_0	
	HSSI_0_1	

continued...

Row Name		Description
	HSSI_1_1	*Note:* Each transceiver die in the package reports a small amount of static power even when no channels are used in the corresponding transceiver tile and transceiver rails (V_{CCR_GXB}, V_{CCT_GXB}, and V_{CCH_GXB}) of that tile are grounded. This is an expected result.
	HSSI_2_1	
HBM	Top	The total thermal power consumption of HBM TOP or HBM BOT, assuming the recommended Ψ_{CA} value. This power is reported at the actual temperature of the specific die, assuming the recommended Ψ_{CA} value above. This temperature may be equal to the maximum junction temperature if a specific die is the hot spot, or it may be at a lower temperature if the hot spot is elsewhere in the package.
	Bot	

Table 37. Recommended ψ_{CA} (°C/W)

Row Name	Description
Recommended ψ_{CA} (°C/W)	The thermal resistance between the center of the package integrated heat spreader and the ambient temperature, assuming the specific core temperature in the given table row. For each row, this is the Ψ_{CA} value that would cause the FPGA core junction temperature to be at the specific value for a given row.

Table 38. Ψ_{JC}(°C/W)

Row Name		Description
FPGA Core		The thermal resistance between the main FPGA core die and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
Transceiver	HSSI_0_0	The thermal resistance between HSSI_0_0 and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
	HSSI_1_0	
	HSSI_2_0	
	HSSI_0_1	
	HSSI_1_1	
	HSSI_2_1	
HBM	TOP	The thermal resistance between HBM TOP or HBM BOT and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
	BOT	

Table 39. TSD Offset (°C) (Stratix 10 Devices Only)

Row Name		Description
FPGA Core		The temperature difference between the hot spot on the main FPGA core and location of the thermal sensing diode (TSD) with the highest temperature reported using the Intel Temperature IP Sense software. (When the IP sense method is used to read the TSDs, all the TSD locations are read and the highest of these is reported.)
Transceiver	HSSI_0_0	The temperature difference between the hot spot on the corresponding transceiver die and location of the thermal sensing diode (TSD) with the highest temperature reported using the Intel Temperature IP Sense software. (When the IP sense method is used to read the TSDs, all the TSD locations are read and the highest of these is reported.) `FPGA transceiver temperature = FPGA transceiver TSD temperature measured using the IP sense method + Transceiver TSD offset.`
	HSSI_1_0	
	HSSI_2_0	
	HSSI_0_1	
	HSSI_1_1	
	HSSI_2_1	

continued...

Row Name		Description
		(If you are not using the Intel Temperature IP Sense software to read the TSD offsets, contact your Intel support representative for a workaround to get the correct TSD temperature.)

For more information about HSSI_*x*_*y* locations, refer to the *Physical Package Structure* topic in *AN 787: Stratix 10 Thermal Modeling and Management*.

Tables above show variations of thermal parameters and power consumption with changing junction temperature of the main FPGA core die. Three values are provided for each parameter. The **Design Max** column contains FPGA core temperature and other parameters assuming the recommended Ψ_{CA} value above. The **-5°C** column provides values of all parameters when FPGA core temperature is 5°C lower than in the **Design Max** column. Similarly, the **+5°C** column provides values of all parameters when FPGA core temperature is 5°C higher than in the **Design Max** column. It is important to realize that under the conditions in the **+5°C** column at least one part of one die in the package exceeds the requested maximum junction temperature, and may even exceed the maximum allowed value for the device. Therefore the values in the **+5°C** column should be used only as an estimate of power dependence on temperature for the purpose of computational fluid dynamic (CFD) simulation, and not for any other purpose

In extreme cases, such as thermal runaway, it may not be possible to calculate the values for +/- 5 degrees, in which case the Thermal worksheet displays the error message: *ERROR: Could not calculate parameter variation with core temperature. Try adjusting $T_{J\text{-}MAX}$ to obtain temperature-dependent parameters*. When this error occurs, the recommended Ψ_{CA} value and all other values above are valid, but the table showing variation of thermal parameters and power consumption with changing junction temperature of the main FPGA core die contains some invalid values. As the error text indicates, adjusting the maximum junction temperature may allow the thermal solver to calculate this dependence, albeit at a different range of FPGA core temperatures than the usual range.

Related Information

- AN 787: Stratix 10 Thermal Modeling and Management
- AN 944: Thermal Modeling for Agilex 7 FPGAs with the Intel FPGA Power and Thermal Calculator
- Intel FPGA PTC - Main Page on page 44

4.16. Intel FPGA PTC - Report Page

The **Report** page shows per-rail currents that the Intel FPGA Power and Thermal Calculator (PTC) calculates.

Important: The **Report** page is for determining how much current each rail must be able to handle. Some of the power savings shown on pages, like Static Power Savings and Smart VID Power Savings, could come from different voltage rails for different devices, and because of this reason, the total power each rail must be able to deliver is higher than the total power the device uses.

Figure 56. Report Page of the Intel FPGA PTC

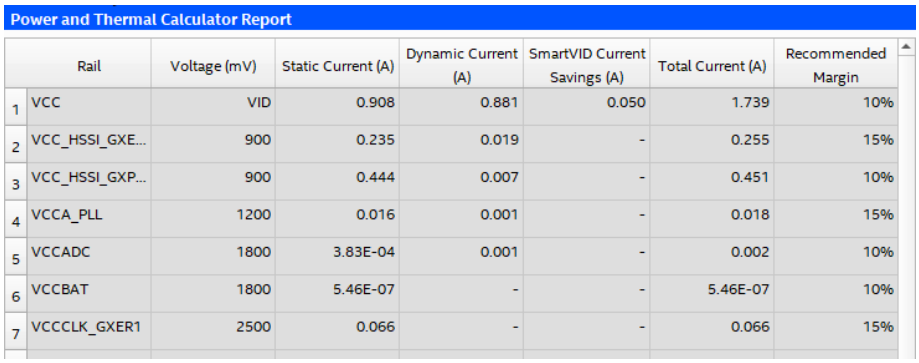
Power and Thermal Calculator Report

	Rail	Voltage (mV)	Static Current (A)	Dynamic Current (A)	SmartVID Current Savings (A)	Total Current (A)	Recommended Margin
1	VCC	VID					
2	VCC	VID					
3	VCC	800					
4	VCC	VID					
5	VCC	850/VID					
6	VCC	VID	1.130	1.008	0.104	2.034	10%
7	VCCADC	1800	3.83E-04	0.001		0.002	10%
8	VCCA_PLL	1200	0.016	0.001		0.018	15%

The **Report** page provides current requirements for each voltage rail, expressed in terms of static current, dynamic current, and total current.

There is a minor difference in the format of the **Report** page between Agilex FPGA portfolio and Stratix 10 device families:

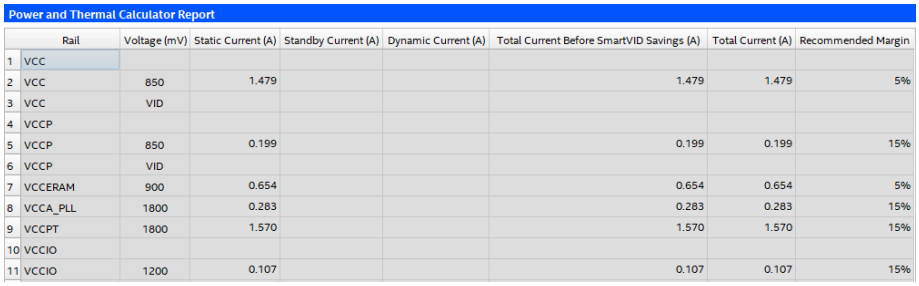
- For Agilex 5 and Agilex 7 device families, every row displayed in the Report table represents a corresponding voltage rail.



Power and Thermal Calculator Report

	Rail	Voltage (mV)	Static Current (A)	Dynamic Current (A)	SmartVID Current Savings (A)	Total Current (A)	Recommended Margin
1	VCC	VID	0.908	0.881	0.050	1.739	10%
2	VCC_HSSI_GXE...	900	0.235	0.019	-	0.255	15%
3	VCC_HSSI_GXP...	900	0.444	0.007	-	0.451	10%
4	VCCA_PLL	1200	0.016	0.001	-	0.018	15%
5	VCCADC	1800	3.83E-04	0.001	-	0.002	10%
6	VCCBAT	1800	5.46E-07	-	-	5.46E-07	10%
7	VCCCLK_GXER1	2500	0.066	-	-	0.066	15%

- For Stratix 10 devices, different sections of the table are preceded by an empty row. For example, an empty VCC row introduces the VCC section of the table, an empty VCCIO row introduces the VCCIO section, and so forth.



Power and Thermal Calculator Report

	Rail	Voltage (mV)	Static Current (A)	Standby Current (A)	Dynamic Current (A)	Total Current Before SmartVID Savings (A)	Total Current (A)	Recommended Margin
1	VCC							
2	VCC	850	1.479			1.479	1.479	5%
3	VCC	VID						
4	VCCP							
5	VCCP	850	0.199			0.199	0.199	15%
6	VCCP	VID						
7	VCCERAM	900	0.654			0.654	0.654	5%
8	VCCA_PLL	1800	0.283			0.283	0.283	15%
9	VCCPT	1800	1.570			1.570	1.570	15%
10	VCCIO							
11	VCCIO	1200	0.107			0.107	0.107	15%

For the **Power and Thermal Calculator Report** table, you can press the **F5** key to resize the rows to be the same height as other rows.

Table 40. Current and Power Regulator Requirements Per Voltage Rail

Column Heading	Description
Rail	Name of the voltage rail.
Voltage (mV)	Rail voltage.
Static Current (A)	Indicates the component of current consumed from the specified power rail whenever the power is applied to the rail, independent of circuit activity (in A). This current is dependent on device size, device grade, power characteristics and junction temperature.
Standby Current (A)	Indicates the component of active current drawn from the specified power rail by all modules on all pages, independent of signal activity (in A). This current is independent of device grade, power characteristics and junction temperature. Standby current includes, but is not limited to, I/O and transceiver DC bias current. Device size has only a small impact on transceiver DC bias current. (This column applies only to Stratix 10 devices.)
Dynamic Current (A)	Indicates the component of active current drawn from the specified power rail due to signal activity of all modules on all pages (in A). This current depends on device size, but is independent of device grade, power characteristics and junction temperature.

continued...

Column Heading	Description
SmartVID Current Savings (A)	Indicates the total current saved from the specified power rail due to SmartVID savings (in A). (This column applies only to Agilex 7 devices.)
Total Current Before SmartVID Savings (A)	Indicates the total current consumed from the specified power rail before SmartVID savings (in A). The sum of static, standby, and dynamic currents. (This column applies only to Stratix 10 devices.)
Total Current (A)	Indicates the total current consumed from the specified power rail (in A). For devices and rails supporting SmartVID, this column shows total current after SmartVID current savings; otherwise, the current reported in this column should equal the sum of static and dynamic currents (for Agilex FPGA portfolio devices) or the sum of static, standby, and dynamic currents (for Stratix 10 devices).
Recommended Margin	Indicates the recommended margin on total current for regulator sizing. The recommended margin on the V_{cc} rail is calculated based on the ratio of dynamic to static power.

5. Factors Affecting the Accuracy of the Intel FPGA PTC

Many factors can affect the estimated values displayed in the Intel FPGA Power and Thermal Calculator (PTC). In particular, the input parameters entered concerning toggle rates and temperature must be accurate to ensure that the system is modeled correctly in the Intel FPGA PTC.

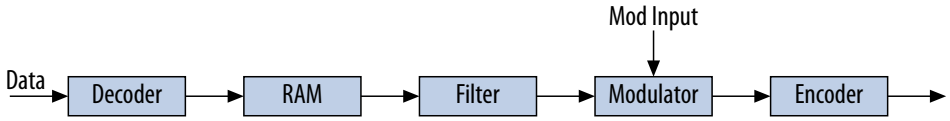
5.1. Toggle Rate

The toggle rates specified in the Intel FPGA Power and Thermal Calculator (PTC) can have a large impact on the dynamic power consumption displayed. To obtain an accurate estimate, you must input toggle rates that are realistic. Determining realistic toggle rates requires knowing what kind of input the FPGA is receiving and how often it toggles.

To get an accurate estimate if the design is not complete, isolate the separate modules in the design by function, and estimate the resource usage along with the toggle rates of the resources. The easiest way to accomplish this is to use previous designs to estimate the toggle rates for modules with similar function.

The input data in the following figure is encoded for data transmission and has a roughly 50% toggle rate.

Figure 57. Decoder and Encoder Block Diagram



In this case, you must estimate the following:

- Data toggle rate
- Mod Input toggle rate
- Resource estimate for the Decoder, RAM, Filter, Modulator, and Encoder module
- Toggle rate for the Decoder, RAM, Filter, Modulator, and Encoder module

You can generate these estimates in many ways. If you used similar modules in the past with data inputs of roughly the same toggle rates, you can use that information. If MATLAB* simulations are available for some blocks, you can obtain the toggle rate information from the simulations. If the HDL is available for some of the modules, you can simulate them to obtain toggle rates.

If the HDL is complete, the best way to determine toggle rates is to simulate the design. The accuracy of toggle rate estimates depends on the accuracy of the input vectors. Therefore, determining whether or not the simulation coverage is high gives you a good estimate of how accurate the toggle rate information is.

The Quartus Prime software can determine toggle rates of each resource used in the design if you provide information from simulation tools. Designs can be simulated in many different tools and the information provided to the Quartus Prime software through a Signal Activity File (`.saf`) or Value Change Dump (`.vcd`) file. The Quartus Prime Power Analyzer provides the most accurate power estimate.

Related Information

Quartus Prime Pro Edition User Guide: Power Analysis and Optimization

5.2. I/O Bank Allocation

The I/O Bank Allocation feature in the Intel FPGA Power and Thermal Calculator (PTC) is available for Agilex 7 devices, and ensures that I/O banks are correctly allocated for proper calculation of thermals.

The Intel FPGA PTC does not allocate power of I/O elements in the FPGA core die uniformly; rather, power contributions of I/O elements are allocated according to their physical locations in the die. The thermal solver uses this power allocation to calculate the temperature map of the die.

If the I/O bank locations are not specified correctly, the power of I/O elements may get allocated incorrectly, to a single bank or to the wrong banks. In such scenarios, the thermal solver still produces a result; however, due to the increased power density, a hot spot may incorrectly occur in the I/O section and erroneously increase the maximum thermals.

The I/O Bank Allocation feature allows you to specify location of I/O elements to banks, thus ensuring that power contributions of I/O banks are allocated correctly, and that there is no miscalculation of thermals.

Related Information

- Agilex 7 General-Purpose I/O User Guide: F-Series and I-Series
- Agilex 7 General-Purpose I/O User Guide: M-Series

6. Intel FPGA Power and Thermal Calculator User Guide Archive

For the latest and previous versions of this user guide, refer to Intel FPGA Power and Thermal Calculator User Guide. If an IP or software version is not listed, the user guide for the previous IP or software version applies.

7. Document Revision History for the Intel FPGA Power and Thermal Calculator User Guide

Document Version	Quartus Prime Version	Changes
2024.04.01	24.1	• Updated several topics to include support for Agilex 5 devices.
2023.12.04	23.4	• Major updates to *Intel FPGA PTC - I/O Page*. — Split the I/O Page Information table for Stratix 10 and Agilex devices. — Added an image for I/O page of the Intel FPGA PTC for Stratix 10 device. — Revised the description in the tables for Stratix 10 and Agilex devices. — Added notes for Application, Write Enable%, and Read Enable% columns. • Minor updates to Agilex-specific table in Intel FPGA PTC - Transceiver Page. • Updated images in the following topics: — *Overview of the Intel FPGA Power and Thermal Calculator* — *Intel FPGA PTC Primary GUI Components* — *Intel FPGA PTC IP Power Summary* — *Intel FPGA PTC IP Power Summary* — *Finding Resources Using the Find Dialog Box* • Made minor updates to the description in *Finding Resources Using the Find Dialog Box*. • Revised the information in *Estimating Power Before Starting the FPGA Design*.
2023.10.02	23.3	• Moved the following topics to *Intel FPGA Power and Thermal Calculator Graphical User Interface* chapter: — *Using Design Hierarchies in the Intel FPGA Power and Thermal Calculator* — *Entering Hierarchy Information Into the Intel FPGA PTC* — *Exporting, Importing, Duplicating, Renaming, and Deleting Hierarchies in the Intel FPGA PTC* — *Bulk Editing Hierarchies in the Intel FPGA PTC* • Revised the "Override Device Selection" image in *Estimating Power While Creating the FPGA Design*. • Revised the "Intel FPGA PTC Hierarchy Manager" image in *Entering Hierarchy Information Into the FPGA PTC* and added a new section for "IP Power Summary" tab. • Made minor revision to the description in *Intel FPGA PTC Hierarchy Manager*. • Added the following new topics: — *Intel FPGA PTC IP Power Summary* — *Finding Resources Using the Find Dialog Box* — *Intel FPGA PTC Searchable Drop-Down Lists* • Added a new section about the "Input Device Utilization of Resources as a Percentage" in *Intel FPGA PTC - Common Page Elements.*

continued...

Document Version	Quartus Prime Version	Changes
		• Updated the description of columns in the following pages: — *Intel FPGA PTC - Logic Page* — *Intel FPGA PTC - RAM Page* — *Intel FPGA PTC - DSP Page* • Added a note to *Intel FPGA PTC - Report Page*. • Updated the images in the following topics: — *Overview of the Intel FPGA Power and Thermal Calculator* — *Intel FPGA PTC Primary GUI Components* — *Entering Hierarchy Information Into the Intel FPGA PTC* — *Exporting, Importing, Duplicating, Renaming, and Deleting Hierarchies in the Intel FPGA PTC* — *Bulk Editing Hierarchies in the Intel FPGA PTC*
2023.06.26	23.2	• Revised the "Intel FPGA PTC Hierarchy Manager" image in *Entering Hierarchy Information Into the FPGA PTC*. • Revised the images and added additional information about device selection in *Intel FPGA PTC Primary GUI Components*. • Made minor updates in *Intel FPGA PTC - Main Page*. • Added *Bulk Editing Hierarchies in the Intel FPGA PTC*. • Added additional information for Intel Agilex 7 devices in *FPGA PTC - Transceiver Page*. • Revised the images in *Exporting, Importing, Duplicating, Renaming, and Deleting Hierarchies in the Intel FPGA PTC* and *Launching the IP Wizard with button*. • Revised *Intel FPGA PTC Hierarchy Manager* to include details about bulk editing. • Revised the Intel FPGA Power and Thermal Calculator image in *Overview of the Intel FPGA Power and Thermal Calculator*. • Revised the I/O Page image and included "Voltage setting for unused HVIO banks" field description in *Intel FPGA PTC - I/O Page*.
2023.03.31	23.1	• Added support for Intel Agilex 7 M-series devices. • Added **NOC** to *Intel FPGA PTC Data Entry Pages* and *PTC - Power Summary* • Added the following parameters to the *RAM Page Information* table — **Vertical Network** — **Vertical Network Port – Read From External Memory Enable %** — **Vertical Network Port – Clock Enable %** • Added *Intel FPGA PTC - NOC Page* • Added **Pseudo channel 0** and **Pseudo channel 1** to *Intel FPGA PTC - HBM Page* • Renamed **Power Summary** window to **Power Summary/Navigation**

continued...

Document Version	Quartus Prime Version	Changes
2022.12.19	22.4	• In the *Overview* chapter: — Removed footnote stating that the PTC does not support importing data from the Quartus Prime Power Analyzer. — In the *Accessing the Intel FPGA Power and Thermal Calculators* topic, added a paragraph to the first row of the table. • In the *Estimating Power Consumption* chapter: — Modified the *Estimating Power While Creating the FPGA Design* topic. — Added the *Importing a .qptc File Generated in the Intel Quartus Prime Power Analyzer* topic. — Modified the steps and figures in the *Entering Hierarchy Information Into the Intel FPGA PTC* topic. — Modified the steps and figure in the *Exporting, Importing, Duplicating, Renaming, and Deleting Hierarchies in the Intel FPGA PTC* topic. • In the *Graphical User Interface* chapter: — Changed *Module Manager* to *Hierarchy Manager* in the *Intel FPGA PTC Primary GUI Components* topic. — Changed *modules* to *entities* in the *Intel FPGA PTC Data Entry Pages* topic. — Added the *Intel FPGA PTC - IP Wizard* topic. • In the *Intel FPGA Power and Thermal Calculator Pages* chapter, updated figures and column description tables in the following topics: — *Intel FPGA PTC - Logic Page* — *Intel FPGA PTC - RAM Page* — *Intel FPGA PTC - DSP Page* — *Intel FPGA PTC - Clocks Page* — *Intel FPGA PTC - PLLs Page* — *Intel FPGA PTC - I/O Page* — *Intel FPGA PTC - Transceivers Page* — *Intel FPGA PTC - HPS Page* — *Intel FPGA PTC - Crypto Page* — *Intel FPGA PTC - HBM Page* • Removed the deprecated *Intel FPGA PTC - I/O-IP Page*. • Updated numerous figures and aligned terminology throughout the document.
2022.09.26	22.3	• Revised *Overview of the Intel FPGA Power and Thermal Calculator* topic for hierarchy support. • Revised *Intel FPGA PTC Power Model Status* topic for clarity. • Consolidated several topics into the *Intel FPGA PTC Versions Available* topic. • Updated the *Estimating Power Consumption Before Starting the Design* topic for hierarchy support. • Added new *Using Design Hierarchies in Intel FPGA PTC* topic. • Added new *Entering Hierarchy Information Into the Intel FPGA PTC* topic. • Added new *Exporting, Importing, Duplicating, Renaming, and Deleting Hierarchies from Intel FPGA PTC* topic. • Added Module Manager explanation and new screenshot to *Intel FPGA PTC Primary GUI Components* topics. • Added new *Intel FPGA PTC Module Manager* topic. • Revised explanation of manual mode in the *Intel FPGA PTC - Common Page Elements* topic.

continued...

Document Version	Quartus Prime Version	Changes
		• Revised *Intel FPGA PTC - I/O Page* for new GPIO voltage setting. • Revised *Intel FPGA PTC - Transceiver Page* for new Treatment of Unused Transceiver Dies setting. • Updated the following topics for hierarchy support: — *Intel FPGA PTC - Logic Page* — *Intel FPGA PTC - RAM Page* — *Intel FPGA PTC - DSP Page* — *Intel FPGA PTC - PLL Page* — *Intel FPGA PTC - I/O Page* — *Intel FPGA PTC - Transceiver Page* — *Intel FPGA PTC - HPS Page* — *Intel FPGA PTC - Crypto Page* — *Intel FPGA PTC - HBM Page*
2022.06.20	22.2	• In the *Intel FPGA PTC Power Model Status* topic, updated the statement of accuracy for the PTC for most Stratix 10 and Intel Agilex designs. • In the *Estimating Power Consumption While Creating the FPGA Design* topic, added a new section: *Appending an Imported .ptc or .qptc File to An Existing Design in the Intel FPGA Power and Thermal Calculator*. • In the *Intel FPGA Power and Thermal Calculator Graphic User Interface* chapter, added the *Deleting Rows from a Table* topic. • In the *Intel FPGA Power and Thermal Calculator Pages* chapter, in the *Intel FPGA PTC Power Summary* topic, added a note to the *Intel Agilex PTC Power Summary* section of the table.
2022.03.28	22.1	• In the *Setting Up the Intel FPGA Power and Thermal Calculator* chapter, in the *Power Analysis for Dual-Core 1SG10M Stratix 10 Devices* topic, made a minor addition to step 7 and added a bullet point in the *Interpreting the Spreadsheet* section. • In the *Intel FPGA Power and Thermal Calculator Pages* chapter: — In the *Intel FPGA PTC - Common Page Elements* topic, added a note to the *Power Rail Current Consumption* section. — Added a note to the *RAM Mode* description in the *Intel FPGA PTC - RAM Page* topic, — Modified the *# PMAs* description in the *Intel FPGA PTC - Transceiver Page* topic, — In the *Intel FPGA PTC - Report Page* topic, added two bullet points explaining a minor format difference between Intel Agilex and Stratix 10 versions of the Report page.
2021.12.13	21.4	• In the *Intel FPGA Power and Thermal Calculator Graphical User Interface* chapter, added an entry for the *Crypto* page to the *Intel FPGA Data Entry Pages* topic. • In the *Intel FPGA Power and Thermal Calculator Pages* chapter: — In the *Power Summary* topic, added *Crypto* to the *Intel Agilex PTC Power Summary* section of the table. — Added the *Crypto Page* topic. — In the *Thermal Page* topic, modified the illustrations and changed the *Apply recommended margin* parameter to *Apply additional margin*, and modified the description accordingly.
2021.10.04	21.3	• Added the *Power Analysis for Dual-Core 1SG10M Stratix 10 Devices* topic. • Added a note and one new section to the *Intel FPGA PTC - Common Page Elements* topic. • Removed a line from the *Power Characteristics* description in the *Device Selection Parameters* table in the *Intel FPGA PTC - Main Page* topic. • Added the *Calculating ALM Utilization* and *Calculating Register Utilization* sections to the *Intel FPGA PTC - Logic Page* topic. • Removed references to *Enpirion* devices, throughout.

continued...

Document Version	Quartus Prime Version	Changes
2021.07.22	21.1	Revised the description of the *FPGA Core* row name for *TSD Offset*, in the *TSD Offset* table in the *Stratix 10* section of the *Thermal Page* topic.
2021.06.10	21.1	In the *Intel FPGA Power and Thermal Calculator Pages* chapter, implemented a minor wording change to the *PLL Reference Clock Frequency (MHz)* description in the *I/O-IP Page* topic.
2021.03.29	21.1	• Implemented minor changes and updates to figures, throughout. • In the *Intel FPGA Power and Thermal Calculator Pages* chapter: — Modified the table in the *Intel FPGA PTC - Power Summary* topic. — Modified the *Junction temperature, T_J* description in the *Main Page* topic. — Added the *eSRAM ID* column to the *RAM Page* topic. — Added the *Domain* column to the *Clock Page* topic. — Added the *IO Bank* and *Bank ID* columns to the *I/O Page* topic. — Modified the description of the *Treatment of Unused HSSI Dies* parameter, and made several changes to the *Transceiver Page Information* table in the *Transceiver Page* topic. — Made extensive changes to the *Thermal Page* topic. — Made changes to the *Current and Power Regulator Requirements Per Voltage Rail* table, in the *Report Page* topic. • In the *Factors Affecting the Accuracy of the Intel FPGA Power and Thermal Calculator* chapter, added the *I/O Bank Allocation* topic.
2021.01.21	20.3	In the *Intel FPGA Power and Thermal Calculator Pages* chapter: • In the *I/O Page* topic, modified the description of the *OE %* column. • Under the *Transceiver Page* topic, added the *Estimating E-Tile Channel PLL Power with the Intel Power and Thermal Calculator* topic.
2020.10.05	20.3	• In the *Setting Up the Intel FPGA Power and Thermal Calculator* chapter, made minor changes to the following topics: — *Obtaining the Standalone Intel FPGA Power and Thermal Calculator* — *Estimating Power Consumption While Creating the FPGA Design* • In the *Intel FPGA Power and Thermal Calculator Graphical User Interface* chapter, made minor changes to the following topics: — *Intel FPGA PTC Select Family Dialog Box* — *Intel FPGA PTC Basic GUI Components* — *Intel FPGA PTC Data Entry Pages* — *Intel FPGA PTC Field Types* — *Intel FPGA PTC Data Entry Error Messages* • Made changes to every topic in the *Power and Thermal Calculator Pages* chapter.
2020.07.24	20.1	In the *Power and Thermal Calculator Tabs* chapter, implemented changes to the *Intel FPGA PTC - ADC/DAC Tab (Stratix 10 Devices Only)* topic.
2020.05.28	20.1	In the *Intel FPGA PTC - Thermal Tab* topic: • Modified the *FPGA Core TSD Offset (°C)* description in the *HBM Die Ψ_{JC}(°C/W)* table. • Modified and consolidated the descriptions for the entries in the *Transceiver Die TSD Offset (°C)* table.

continued...

Document Version	Quartus Prime Version	Changes
2020.04.27	20.1	In the *Power and Thermal Calculator Tabs* chapter, updated the figure and revised the table contents, in the *Intel FPGA PTC - ADC/DAC Tab (Stratix 10 Devices Only)* topic.
2020.04.13	20.1	• Added support for Stratix 10 devices, throughout. • In the *Setting Up the Intel FPGA Power and Thermal Calculator* chapter: — Modified the *Licensing* information in the *Availability* topic. — Modified the *Importing* information in the *Estimating Power Consumption While Creating the FPGA Design* topic. • In the *Power and Thermal Calculator Graphical User Interface* chapter: — Added the *Intel FPGA PTC Select Family Dialog Box* and *Intel FPGA PTC Basic GUI Components* topics. • In the *Power and Thermal Calculator Tabs* chapter: — Added a *Notice* statement to the *Power and Thermal Calculator Tabs* topic. — Added the *Intel FPGA PTC - ADC/DAC Tab* topic. — Added the *Intel FPGA PTC - HBM Tab* topic. — Added the *Intel FPGA PTC - Thermal Tab* topic. — Added the *Intel FPGA PTC - Intel Enpirion® Tab* topic. • Added the *Intel FPGA Power and Thermal Calculator User Guide Archive*.
2020.02.14	19.4	Initial release.

A. Measuring Static Power

Follow these steps to measure static power in your design.

1. Verify that the device is properly configured and in user mode. (CONF_DONE, NSTATUS, NCONFIG, and INIT_DONE values should be high.)
2. Wait until a stable junction temperature (thermal equilibrium) is reached.
   - Use of a thermally controlled chamber is recommended.
   - You can measure the junction temperature of the FPGA using the on-chip temperature sensing diode (TSD). Refer to your device documentation for details on using the TSD. Alternatively, you can measure the junction temperature with the Agilex 7 Temperature Sensor IP Core, but with reduced accuracy.
   - If a thermally controlled chamber is not available, use temperature feedback from the on-chip TSD or Agilex 7 Temperature Sensor IP Core to control a heat sink fan to achieve a desired junction temperature.
   - You can also use a heat gun to achieve a desired temperature; however, this method offers less thermal control.
3. Keep all inputs constant and do not toggle any I/Os or any clock signals (except for the clock to the Agilex 7 Temperature Sensor IP Core, if you are using the Agilex 7 Temperature Sensor IP Core to measure temperature.)
4. Depending on the board design, you can measure static current in one of several ways:
   - Use a regulator with the ability to measure voltage drop across a shunt resistor, and query the power measurement through the power management bus (PMBus)/system management bus (SMBus) interface.
   - If a regulator with PMBus/SMBus support is not available, you can measure the voltage drop across the shunt resistor manually for each power supply and calculate the current from the voltage drop.
   - If you use an external power supply, query the current measurement from the power supply according to the manufacturer's specifications.
5. If you want to isolate and understand the static power component of your design's total power consumption, take several current measurements across a range of temperatures and record the junction temperature of each measurement. Refer to the junction temperatures to correlate static power measurements with their corresponding total power measurements.
6. The silicon static power measurements can be compared with the static power estimate from the Quartus Prime Power Analyzer report or the static values shown on the **Report** tab in the Intel FPGA Power and Thermal Calculator.

Related Information

- Agilex 7 Power Management User Guide

- Quartus Prime Pro Edition User Guide: Power Analysis and Optimization