Welcome to the IDF Research Briefing

Spring 2006

Justin Rattner

Intel Senior Fellow
Intel Chief Technology Officer

Intel Developer FORUM

Agenda

10:00-10:45	Welcome and Research Briefing Justin Rattner, Intel Senior Fellow and Intel Chief Technology Officer
10:45-11:30	Future of the Enterprise Raj Yavatkar, Intel Fellow
11:30-12:30	Lunch with Technologists
12:30-1:30	Building the Mobile Tomorrow Kevin Kahn, Intel Senior Fellow
1:30-2:30	Tech-a-Palooza Hosted by Andrew Chien Director, Intel Research

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Research At Intel

- More than 1100 researchers
- 18 locations worldwide
- 1500+ US patents in 2005
- Innovative research models

Research At Intel

Platform Solutions

IT

Systems

Communications

Microprocessors

Manufacturing

Si Devices & Processes

Research

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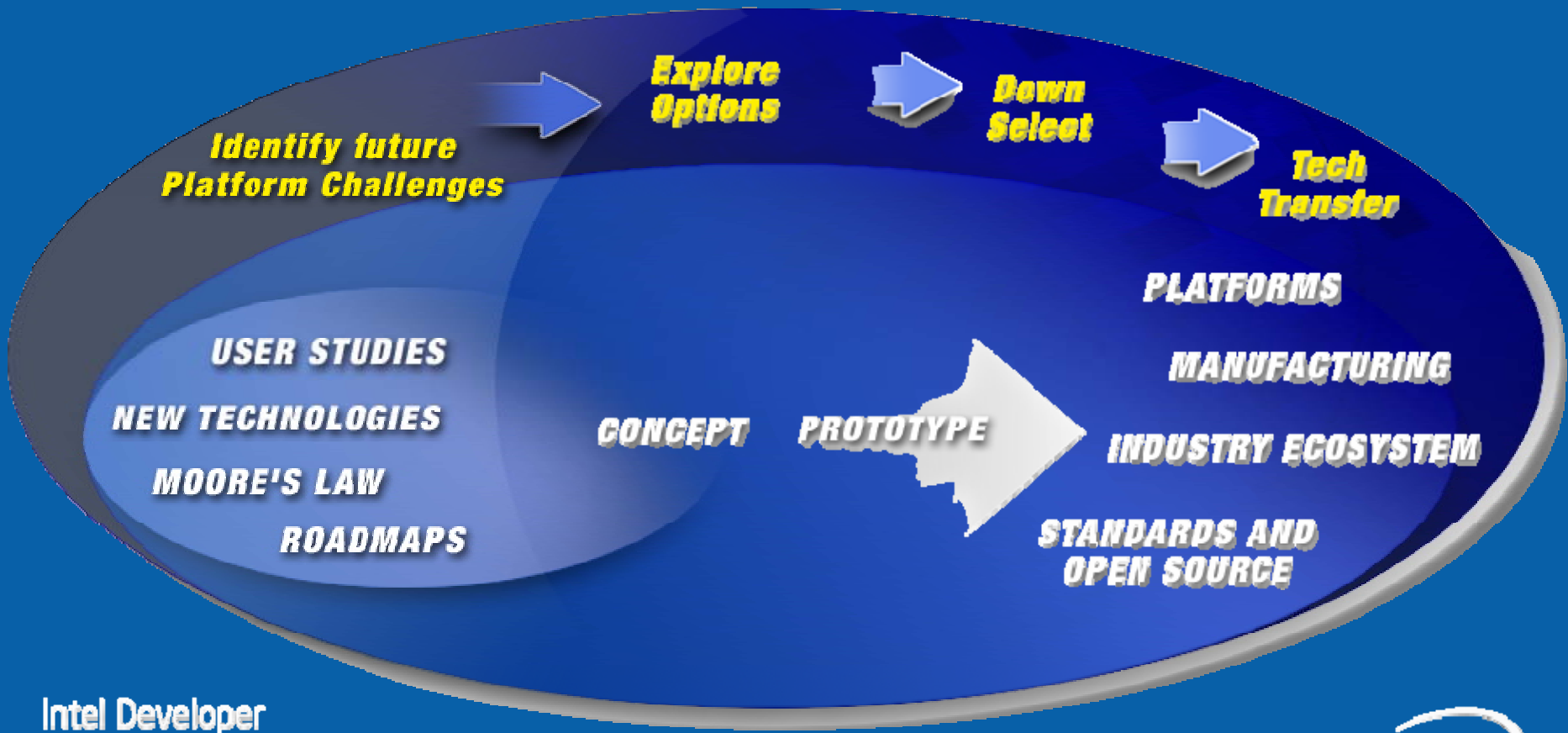
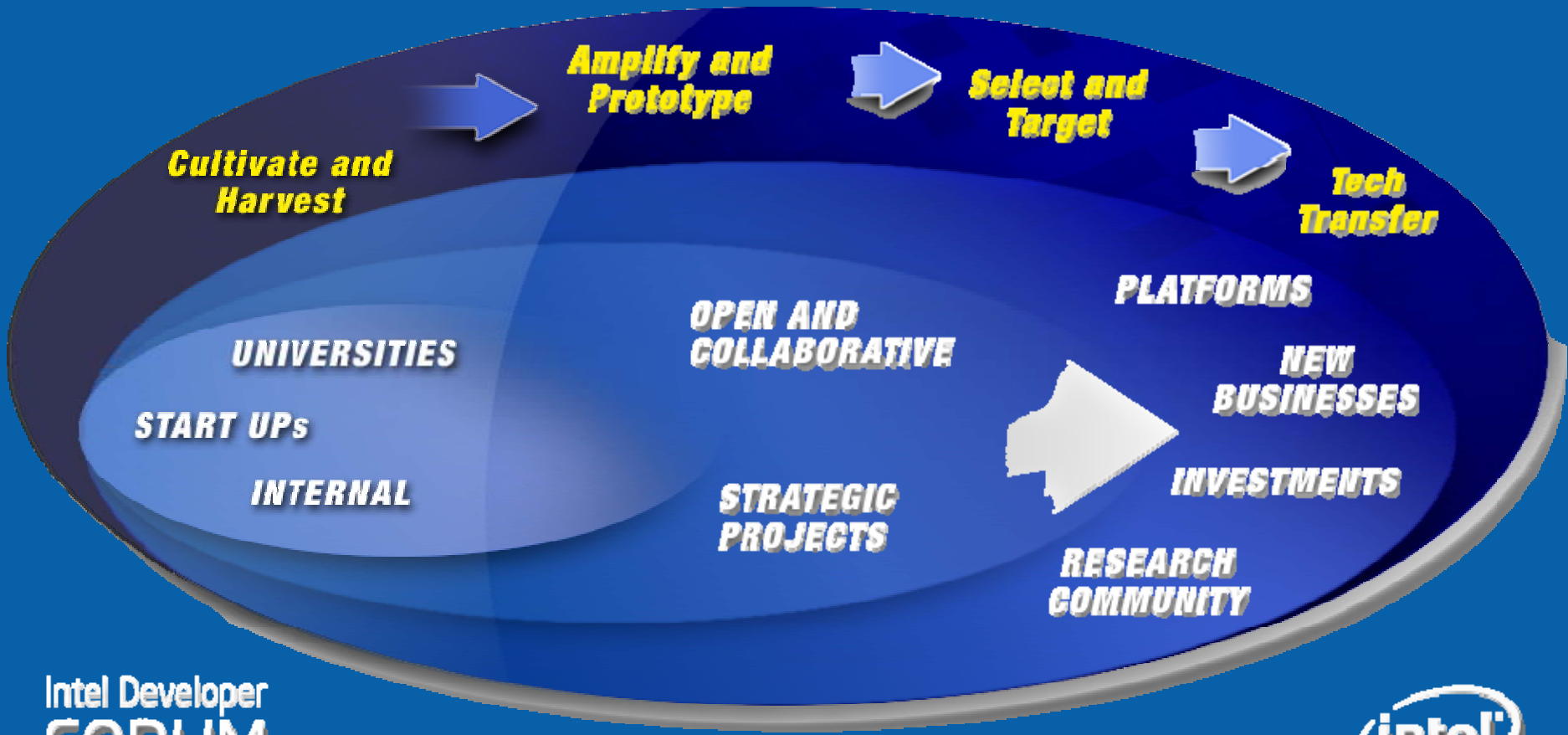
Directed Research

Delivering innovative technologies for identified platform challenges



Exploratory Research

Investigating emerging and disruptive technologies for tomorrow's applications



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Today's Research Tomorrow's Platforms…

- Aware Platforms
  - Introduced Fall IDF 2005
- Tera-Scale Computing Research Program
  - Introduced Today
- Future of the Enterprise
- Building the Mobile Tomorrow

The Era Of Tera

Terabytes of data. Teraflops of power.

Simulated biology

Tele-present doctors

Intuitive interfaces

Machine vision

When personal computing finally becomes ***personal***

Immersive 3D entertainment

Virtual realities

Source: Steven K. Feiner, Columbia University.

Interactive learning

Tele-present meetings

Courtesy of the Electronic Visualization Laboratory, Univ. of Illinois at Chicago.

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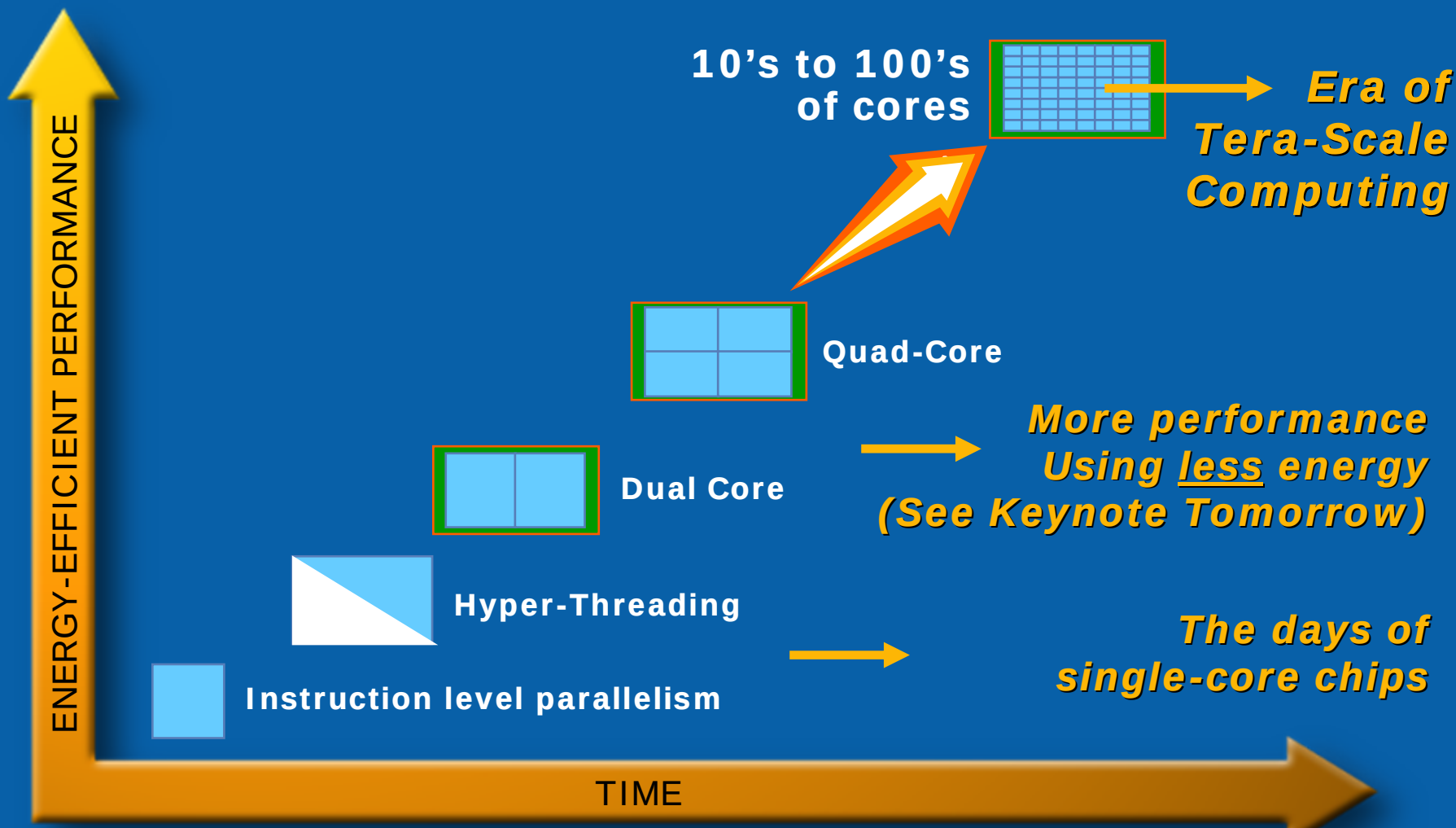
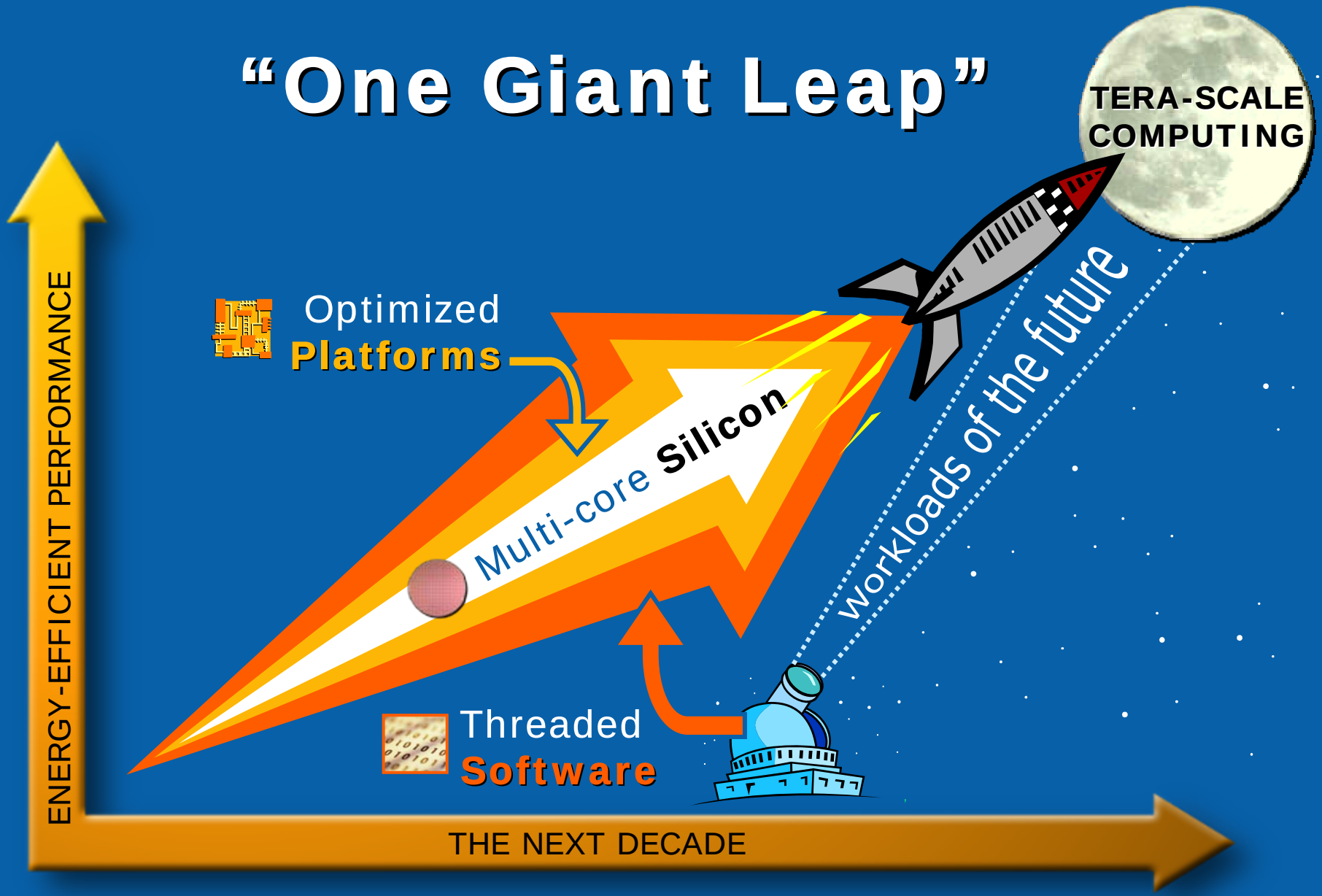
Tera-Leap to Parallelism:



Opportunities and Directions

	Shift to…
Having processors with a multitude of cores that execute many threads in parallel, will enable a host of new and exciting usage models	**Silicon** with 10s or 100s of efficient, highly threaded cores
Highly parallel processors require enhanced, optimized platform architectures to enable scalability and new, extreme computing apps.	**Platforms** with high bandwidth I/O & memory, aggressive power management
To take advantage of parallel computing, we must understand how to design and program for future software workloads	**Software** programming models, tools and apps

“One Giant Leap”



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Intel® Tera-Scale Computing Research Program

80+ Projects Worldwide

Silicon Research

Examples:
High-bandwidth memory
Energy optimization
Configurable caches
Scalable fabrics
CMOS VR
Core I/O

Platform Research

Examples:
3D Stacked Memory
Energy management
High-speed I/O
Virtualization
Multi-radio
Photonics

Software Research

Examples:
Transactional memory
Workload analysis
Parallel run-time
Auto-threading
Compilers
Libraries
Tools

Internal projects plus industry, academic collaborations

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Example Projects

Key Challenge	*Research Direction*	*Example Innovation*
Scalability	Identify and eliminate the remaining bottlenecks	Configurable cache architecture
Balanced Design	Bring more memory closer to the cores	3D stacked memory
Energy Efficiency	Fine control over silicon and platform energy use	EESA: Energy efficient system architecture
Applications	Collaborate with leading application developers	Future disclosure
Programmability	Simplify the writing of parallel programs	Transactional memory to replace locks

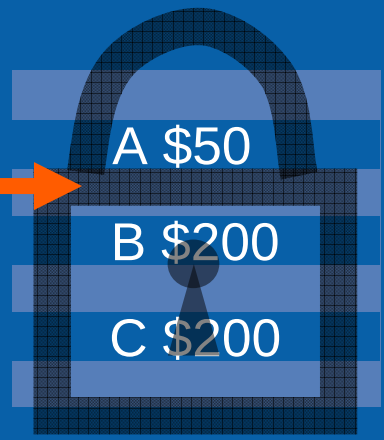
Example: Unlocking Parallelism

Must carefully control how multiple threads access common memory

Today we "lock" memory for one thread at a time.

- Other threads must wait, reducing multi-core benefit
- Locking code scales poorly, must re-do for more threads
- Can cause critical software deadlocks and errors

Account locked during access



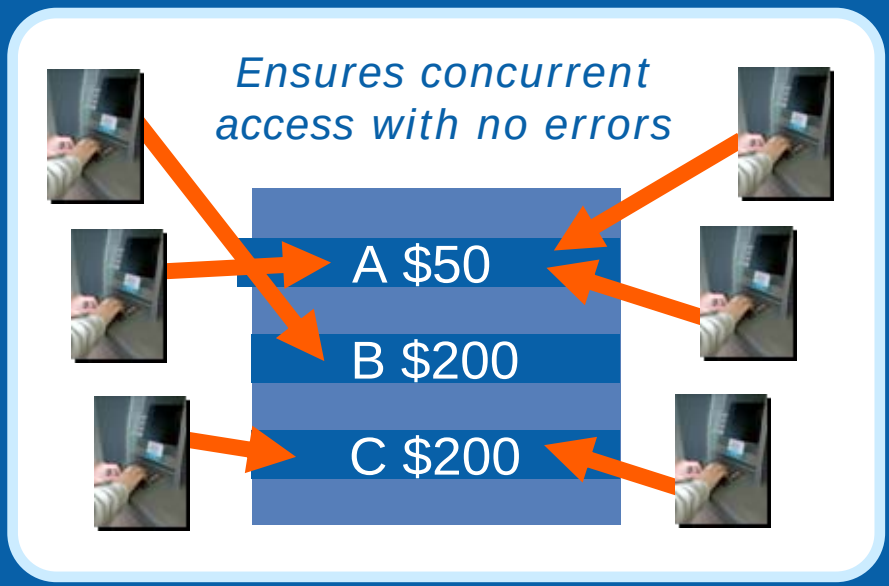
2003 Northeast blackout

Courtesy NASA/JPL-Caltech

Mars rover problem

Solution: Transactional Memory

Transactional memory is a technique for coordinating how multiple threads access the same memory



- Greater performance due to concurrent execution
- Eases the writing of parallel programs that work and scale
- Eliminates deadlocks

Java* based proof-of-concept shows 3-4x performance gain on a 16-way Xeon® Processor-based system.

DEMO

Summary

- Intel researchers are enabling platforms with new capabilities to dramatically improve the way we work and play.
- The Intel® **Tera-Scale Computing Research Program** will enable future platforms to run parallel threads on many cores.
- This broad program includes projects looking ahead to future software workloads, incorporating this data into new designs.
- Transactional Memory research is just one example of how Intel is breaking barriers to “Tera-Scale” personal computing.

Tera-Scale Computing at IDF

Related Sessions:

- Multi-Everywhere: The New Era in Computing
  Wednesday, 2pm in room 2000
- Emerging Applications that Shape the Future Computing Platform
  Tuesday, 11am in room 2000
- Transactional Memory: Unlocking Parallelism
  Tuesday, 10am in room 2000
- Energy Efficient System Architecture
  Thursday, 3:30pm in room 2000
- Silicon Photonics: A Disruptive Technology
  Thursday, 2:30pm in room 2000

Related Demos:

- Booth 1008: Advanced Microprocessor Technology Research
- Booth 1002: Energy Efficient Technology Research