Intel @ VLSI Symposia 2008

Today's Presenters:

Mike Mayberry
VP, Technology & Manufacturing Group
Director, Components Research

Randy Mooney
Intel Fellow, Corporate Technology Group
Director, I/O Research

Rajesh Kumar
Intel Fellow, Digital Enterprise Group
Director, Circuit & Low Power Technologies

Summary

- Intel continues to innovate in research & development
- Five Intel papers will be presented at the 2008 VLSI Symposia
  - Cache memory research
  - Process technology
  - Circuits research
  - Nehalem Micro-architecture
- Intel represented on 3 panels
  - SOI
  - SRAM scaling
  - Photons vs. Electrons

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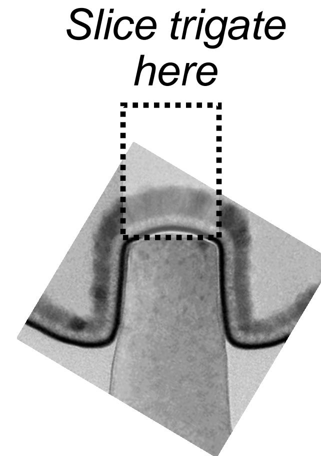
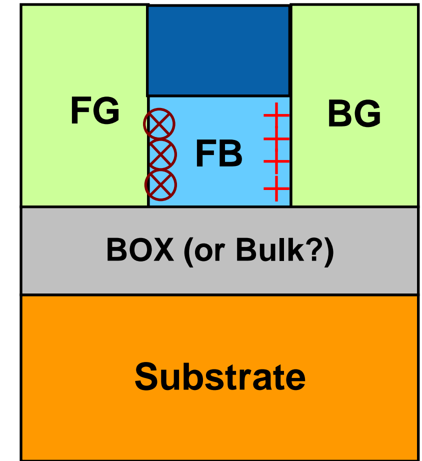
Floating Body Cell

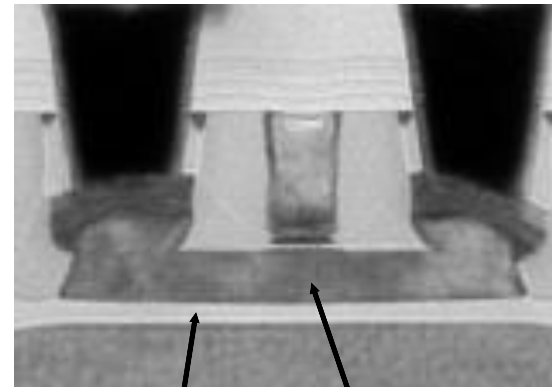
- Floating body cells (FBC) are an alternative to conventional cache memory
  - Potentially 3-4x more bits per area
  - Potentially less costly than embedded DRAM (capacitor is in the body)
- Previous Intel work on non-planar FBC was published at IEDM 2006
  - Charge stored horizontally in narrow fins using technology developed for trigate
- Key elements of this work
  - Planar devices 2 generations smaller than other published results
  - Suitable for 15nm node and beyond, projected bit cell smaller than 0.01 um2
  - Excellent agreement between simulation and experiments that allows scaling prediction
  - This work is at the single cell level; no array data to measure statistics
- Future plans
  - Will need to build large arrays to validate
  - Product intercept not yet determined

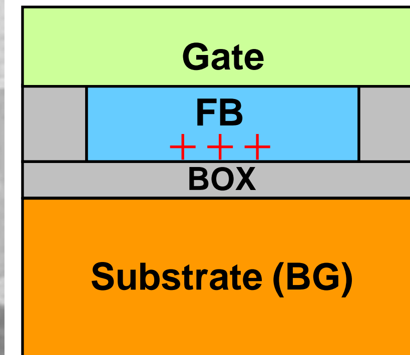
Slice trigate here





Dual gate, Intel IEDM 2006



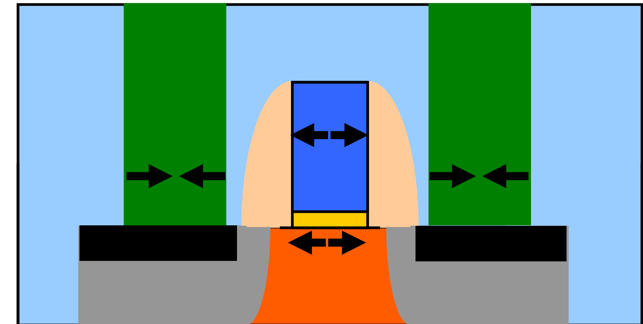


Planar on SOI, Intel VLSI 2008

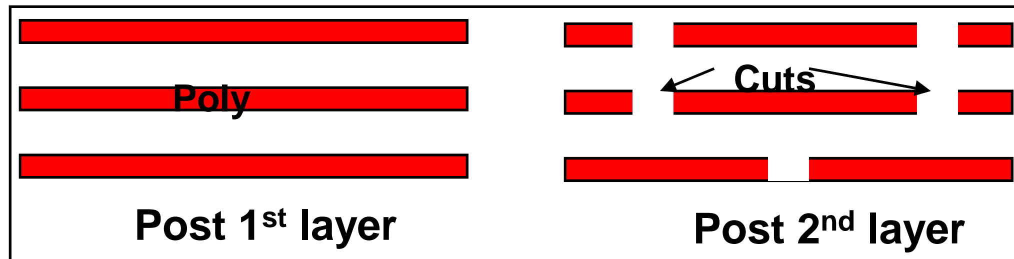
Paper 9.4: A Scaled Floating Body Cell (FBC) Memory with High-k+Metal Gate on Thin-Silicon and Thin-BOX for 16-nm Technology Node and Beyond

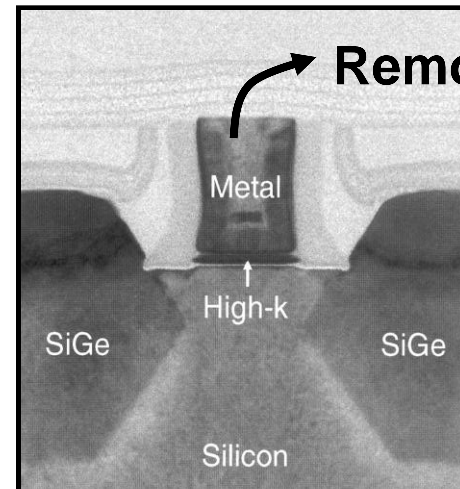
45nm High-k + Metal Gate Strain-Enhanced Transistors

- World's first 45nm high-k + metal gate technology first described at IEDM 2007
- This paper details:
  - Strain integration with high-k + metal gate
  - Performance advantages of Intel's gate last process flow shown
  - Best transistor results for any published 45nm or 32nm technology
  - Unique cost-saving 193nm dry patterning techniques



NMOS:
1) Metal gate Stress
2) Trench Contact Stress

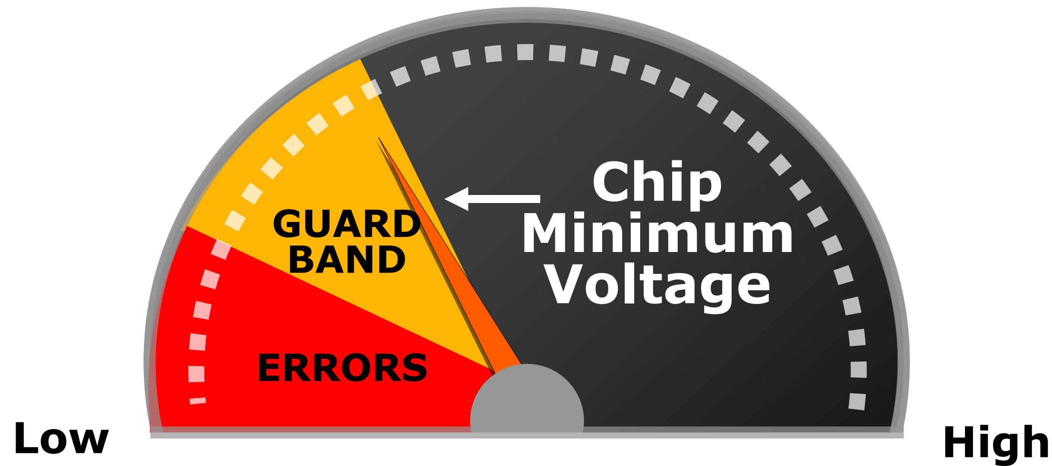




PMOS:
1) Enhanced SiGe stress
2) Dummy gate removal stress

Robust Circuits for Better Energy-Efficiency

- Energy-efficiency is critical to scaling performance
- Minimum voltage & power also subject to guardbands



- Circuits today use this safety margin to protect against any variations in the process, voltages, or temperature.

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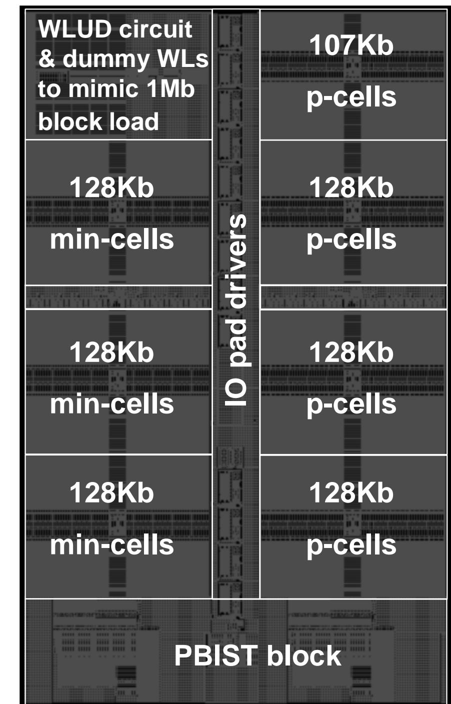
Robust Circuits for Better Energy-Efficiency

- We demonstrate a robust SRAM cell design for building on-chip caches that can **tolerate these variations**
- Uses 45nm minimum feature sizes
- Stabilizes both reads and writes
- Up to 26x better error characteristics

Research will allow Intel to push to better performance and power characteristics without failures on future processes



Testchip image & layout

Paper 5.4: PVT-Variations and Supply-Noise Tolerant 45nm Dense Cache Arrays with Diffusion-Notch-Free (DNF) 6T SRAM Cells and Dynamic Multi-Vcc Circuits

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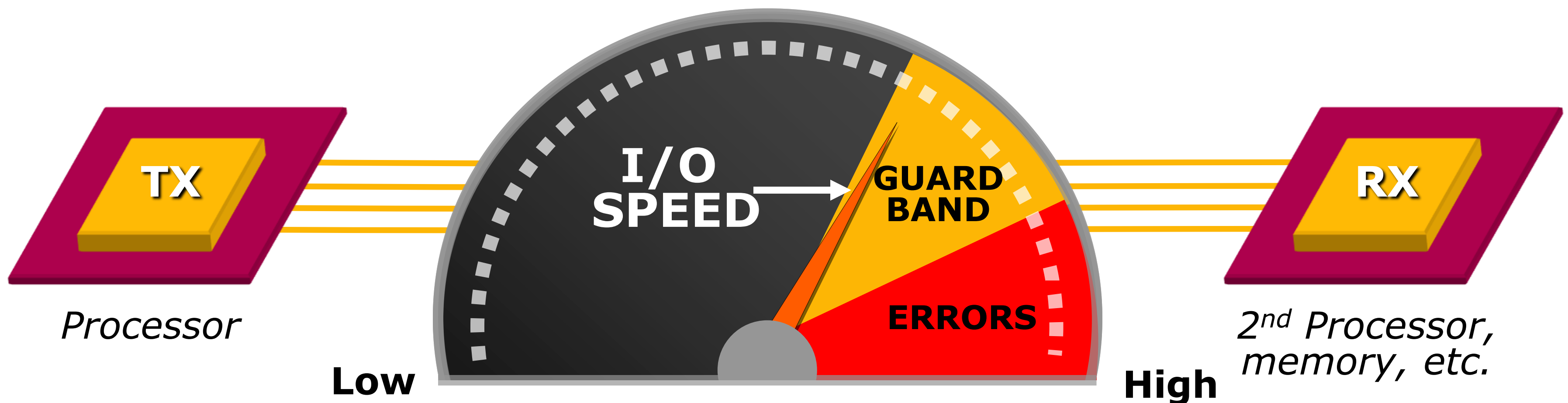
Maximizing I/O Speed w/ On-chip Test Circuits

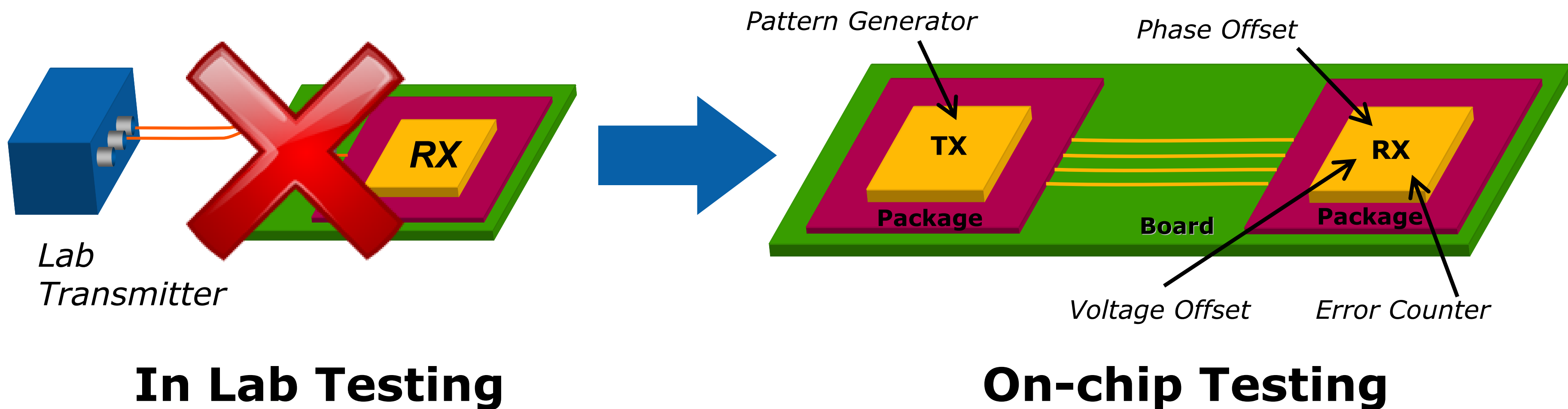
- Shift to many-core increasing demands for chip-chip I/O
  - Bandwidths moving to 10+ Gigabits/sec/pin
- One limitation today is safety margins called “guardbands”



- Conservative margins determined before chips ship to customer

Maximizing I/O Speed w/ On-chip Test Circuits

- Our testchip integrates more I/O test features on-chip
- Tests are more accurate, can be done in **the final system**



Research could reduce guardband size & enable the highest possible performance I/O for tera-scale systems

Nehalem Clocking Highlights

- Extremely high bandwidth Intel® QuickPath interconnect and DDR3 integrated memory controller enabled by advanced clocking
  - 25GB/s, 6.4GTs QPI & 32GB/s memory bandwidth
  - Low Jitter PLL with duty cycle correction & shallow transmit clock distribution
  - Jitter attenuating receiver clocking with PVT tracking
- Modular & scalable
  - Core, memory system, and IO are all decoupled frequency and voltages
- Power efficient clocking architecture
  - Chip frequency adapts to power supply voltage and droops
  - Fast power state transitions with 56% faster PLL lock time
  - Duty cycle adapts to transistor variation and lifetime stress

VLSI Panel Highlights

Tuesday, June 17

- **RJ1: Ten years after – Has SOI finally arrived?**
  Intel Panelist: Mark Bohr
  Other panelists from: Infineon, IBM, SOITEC, AIST, TSMC, Toshiba, Hitachi

- **R1: Who will keep SRAM scaling alive by 2012: Designers or Technologists?**
  Moderators: K. Zhang, Intel, K. Takeuchi, NEC
  Intel panelist: Claire Webb
  Other panelists from: IBM, Texas Instruments, TSMC, Toshiba, Intel, NEC

- **R1: Photons vs. Electrons – Which Will Win and When? (The Ongoing Race for Short-Distance High-Speed Data Connectivity)**
  Intel panelist: Ian Young
  Other panelists from: Stanford University, Force10 Networks, Teranetics, Fujitsu Japan, NTT Japan

Q&A