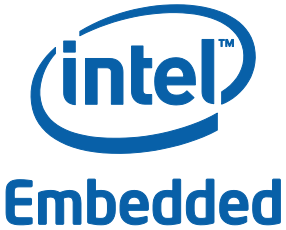

White Paper
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Electrical System-Validation Methodology for Embedded DisplayPort*

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Executive Summary

Embedded DisplayPort* (eDP) is one of the latest digital video standards. This paper describes an innovative idea for eDP System Marginality Validation (SMV). This solution defines an automatic test setup, including both hardware and software.

The advantages of this solution are very low cost, wide validation coverage and good compatibility with customer's environment.

This methodology can be applicable for validating any other video interface, although initially it was used to perform a system-level functional test of the eDP interface.

SMV is a common approach used to indicate a system's health and stability, which, in turn, can be used to determine whether or not a product should be transferred into High Volume Manufacturing (HVM) phase.

The main advantages of the methodology described in this document are:

- No need of logic analyzer (LA) – ~100 K$ cost saving per setup.
- Wide coverage: supports all possible resolutions up to 2560 x 1600.
- Good signal integrity (SI) achieved by using a standard DP Rx and no signal probing.

Contents

Business Challenge

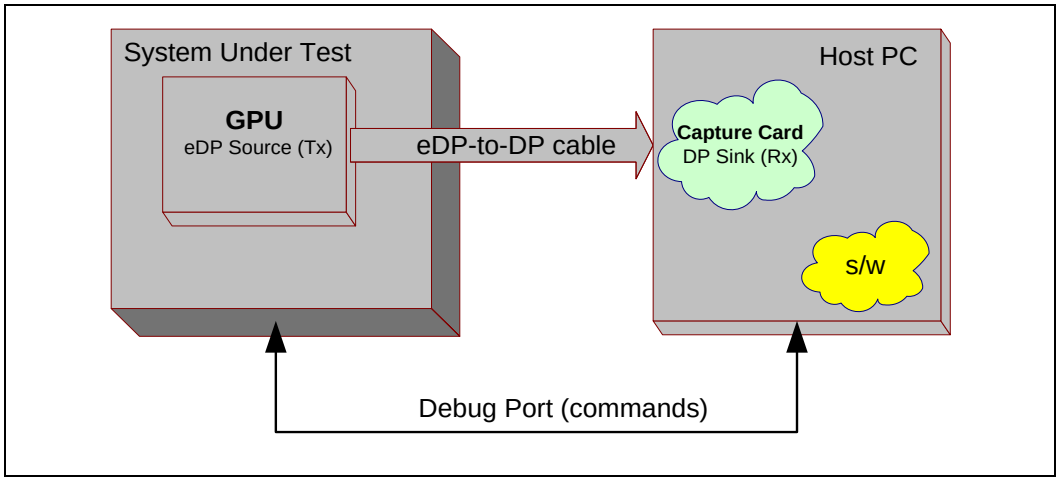
VGA standard is a widely used analog interface, but in the recent years several digital standards emerged (e.g., DVI and HDMI*). Video Electronics Standards Association (VESA) announced the DisplayPort* standard in 2006. The main advantages of DisplayPort are low power consumption, low cost (royalty free), and no clock wire as the clock is embedded into the data. DisplayPort's bit rate per lane is 1.62 or 2.7 Gb/sec (5.4 Gb/sec in the future), multiplied by up to four differential channels named "lanes". DisplayPort has a sub-standard called Embedded DisplayPort* (eDP*) which is intended for an in-box connection, e.g., to feed a flat panel display inside a mobile PC.

DisplayPort and eDP standards are very similar. This paper concentrates on eDP. Its validation is more challenging because of the standard's higher complexity and due to the fact that very few eDP devices have been manufactured so far. The main differences between DP and eDP are the number of electrical wires, different physical connectors, and different usage models. For example, eDP has an option of supplying backlight power to the LCD panel, getting indication from an ambient light sensor and controlling monitor's brightness.

One of the challenge sides for validation engineers is that DisplayPort communication is not symmetrical in terms of physical structure. The traffic is unidirectional from a transmitter (named source, e.g., DVD player) to a receiver (named sink, e.g., video projector). Thus, DisplayPort standard lacks built-in far-end loopback ability. This limitation is one of the major difficulties in validating video interfaces.

In the proposed methodology, the Graphics Processor Unit (GPU) is connected to an eDP capture card, which resides on a PC (Figure 1). The connection is done using eDP-to-DisplayPort cable. A known functional traffic, i.e., a predefined image, is sent over the eDP link, and is captured on the receiver (Rx) side. Then a pixel-to-pixel comparison is performed to find a mismatch. In addition, the transmitter's electrical parameters, e.g., voltage swing, are swept to find the system's margin.

Figure 1. Simplified Setup of eDP* Test



The major advantages of the methodology in this paper are very low cost, wide coverage and good compatibility with the customer's environment. More features are:

- No need of Logic Analyzer – ~100 K$ cost saving (per test setup).
- Wide coverage: supports very high resolutions – up to 2560 x 1600.
- Low test time – a full single run takes ~5 min. The transmission and capture are fast, and part of the test runs on the Intel® architecture (IA) cores of the DUT.
- Good signal integrity (SI) achieved due to a standard DP Rx application. No midbus probing is needed, so the tested signal path is unaffected. This leads to enhanced compatibility with real environment of the customer.
- Low-cost capture card makes massive and parallel validation possible.
- Direct capturing of DP traffic eliminates any data format conversion or level shifting.

The described methodology was first implemented in a CPU validation, but the device under test (DUT) can be any kind of GPU with eDP or DisplayPort output port. Moreover, the main concept of the methodology fits any other video link validation as well.

Solution

Complete Test Setup

The proposed solution requires:

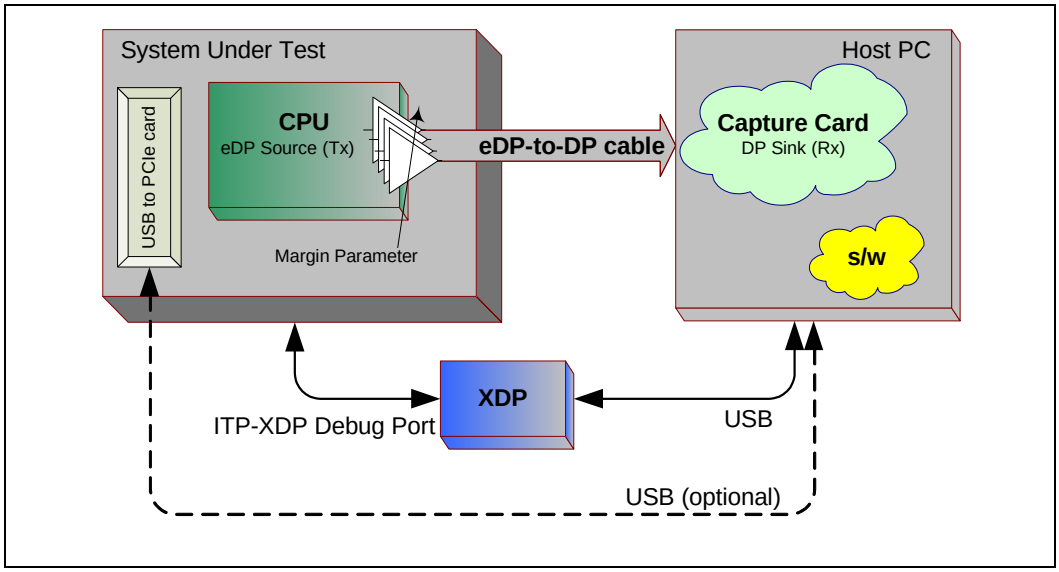
1. The system under test, also known as the target.
2. A UFG-04 DP capture card, connected to a host PC.

3. An eDP-to-DP cable – LA10EM006-2N or similar
4. Automation software.

The whole setup (Figure 2) is controlled automatically by software, which resides on a host PC. The host PC controls the eDP Transmitter (Source Tx) and the capture card (Sink Rx); it also loads a predefined image data into the CPU. The eDP Source transmits the data over the eDP-to-DisplayPort cable, into the DisplayPort capture card. The received image is captured and then compared to the sent image, pixel by pixel. The comparison is done on the host. The software can return not only binary pass/fail information, but also the number of failed pixels and their coordinates. Moreover, it can generate a third image showing location of the differences between sent and received images. The host also sets the SMV margin parameters, like the signal amplitude, to each of the test points.

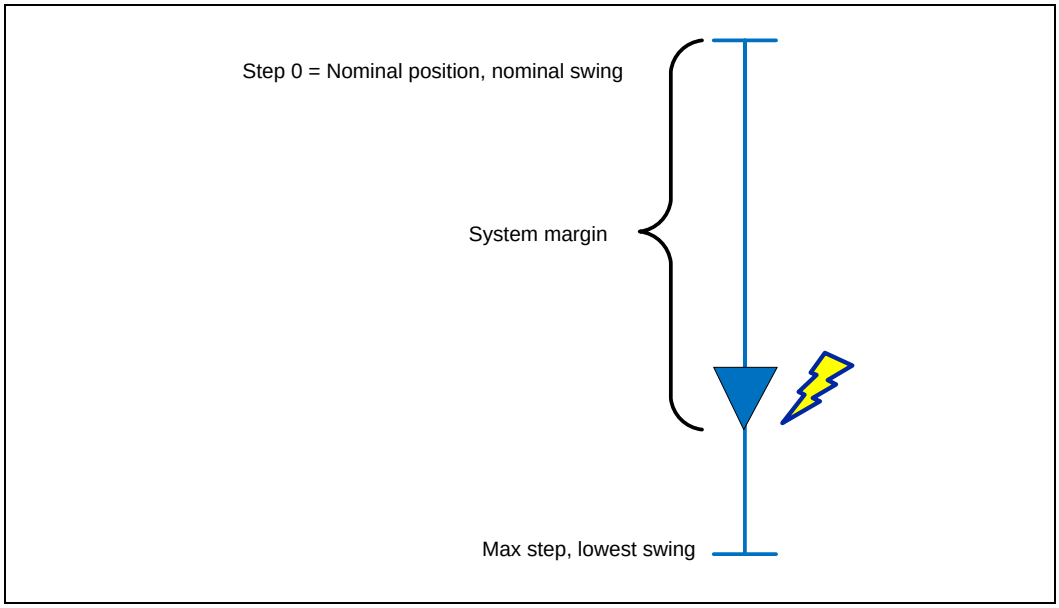
Part of the software code is loaded directly into the CPU's Intel® architecture cores. This requires connections like an extended debug port, e.g., XDP JTAG port, or a USB-to-PCI Express* (PCIe*) bridge add-in card.

Figure 2. Complete eDP* Test Setup



The margin parameter used for the eDP test is Tx amplitude swing. Nominal swing is defined as Step 0, the nominal margin position (see Figure 3). Going down with steps means lowering the swing. When a fail condition is met, the margin we seek is the distance of the current step from the nominal position. Going up with steps, i.e., raising the swing, is also possible though it would produce no fails because the receiver copes better with an amplified signal.

Figure 3. Margin Steps

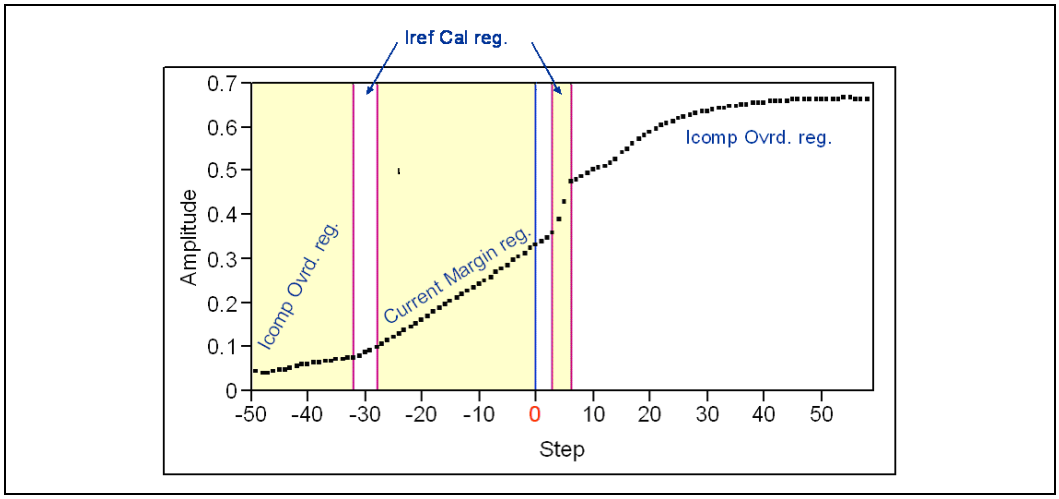


This Tx swing parameter is composed of three different DFT margin hooks, named:

- Current Margin register
- Iref Cal register
- Icomp Override register

All the three hooks affect the output buffer's amplitude. We have characterized each Tx swing step, as seen in Figure 4.

Figure 4. Tx Swing Margin Parameter Characterization



The characterization was done by making the CPU's eDP port to transmit a clock pattern, i.e., "101010…". The signal's swing was measured (Figure 5) on the CPU's pin using an SDA6020 oscilloscope with a D600AT high-impedance differential probe. A clock pattern made the swing measurement to be more accurate, than it would be using a data pattern. Figure 4 illustrates that there is a direct proportion between the signal's amplitude and the step number, but it is not linear in most of the range. An average step size is ~5mV.

Figure 5. Tx Swing Amplitude Sweep, As Seen On An Oscilloscope

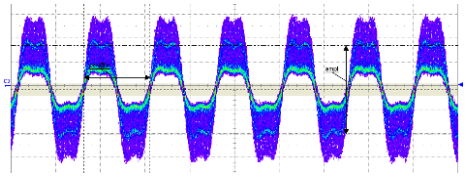
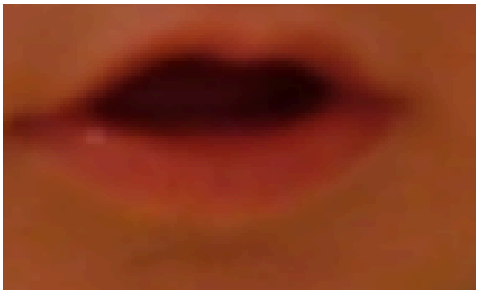
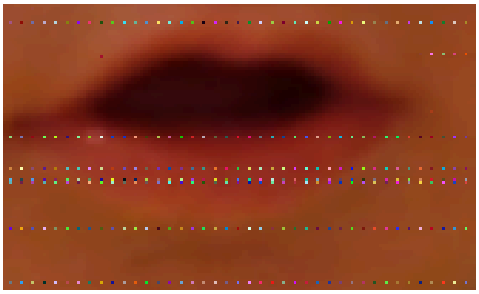
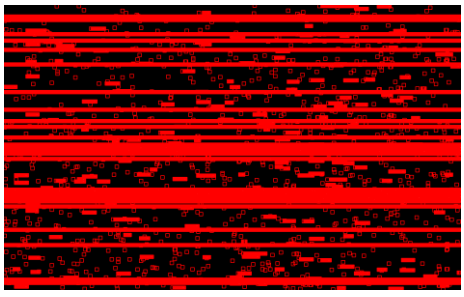


Table 1 illustrates the image comparison principle. It is important to know that not all the shown visualization is implemented in the current test flow, but can be created manually; only images (1) and (2) are available after an automatic test run.

Table 1. The Image Comparison Principle

Original Image Capture	Zoom of Image Capture	Note
		(1)
		(2)
		(3)
		(4)

NOTES:

1. The original image sent over the eDP link.
2. The margin parameter set to step -37 leads to a corrupted received image with lots of mismatched pixels.
3. A difference image, showing the location of the mismatched pixels.

4. The difference image with the mismatched pixels highlighted.

SMV Concept

System Marginality Validation[1] (SMV) is an approach used by engineers to indicate a system's health and stability, which, in turn, can be used to determine whether or not a product should be transferred into High Volume Manufacturing (HVM) phase.

The production yield will eventually reflect the quality and robustness of the design. In case of multiple failures or low SMV margin, an in-depth investigation has to be started to find the root cause. For example, this can be done by means of electrical probing and verifying that the electrical parameters meet their specifications. By testing a small number of DUTs (devices under test), and using statistical techniques of design of experiment (DOE), it is possible to make an estimation of the yield in the mass production phase. By using this methodology, design defects can be corrected before entering HVM.

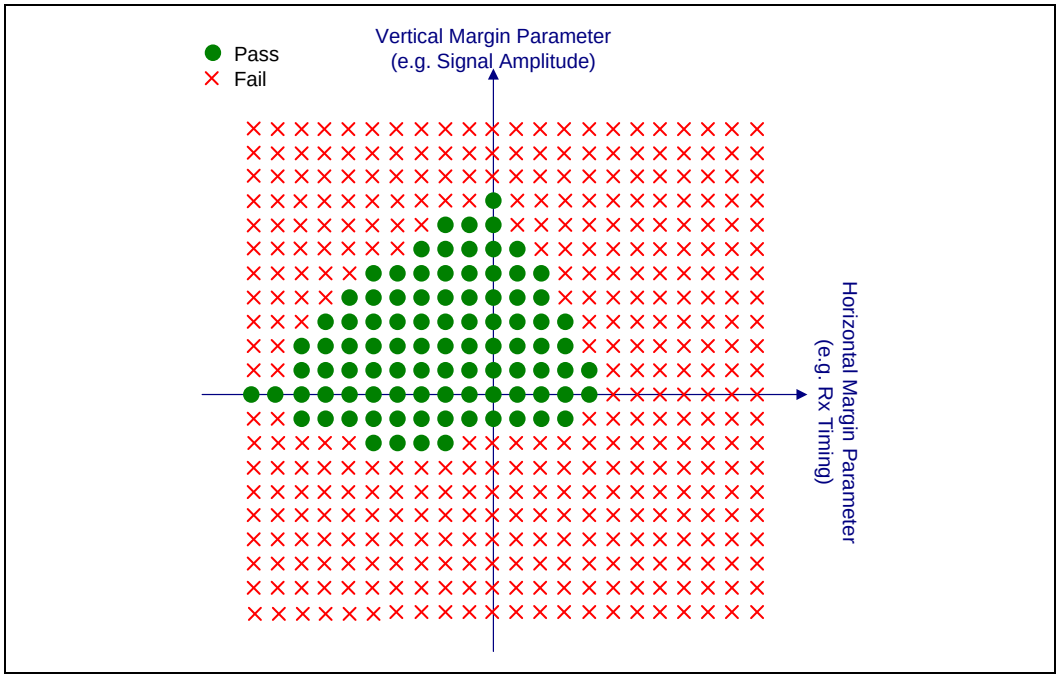
SMV is based on sending data traffic through DUT link, while monitoring reception errors which are predefined beforehand. This step is called "nominal position testing". The next step is to sweep predefined electrical knobs/hooks, in order to check the system's stability. These knobs are called margin parameters, and are usually designed for test (DFT) features. Additional stress tests, e.g., power, can be defined to run simultaneously on the DUT. Some examples of swept margin parameters are:

- Signal amplitude
- Timing parameters of the Rx circuit
- I/O buffer impedance
- I/O buffer voltage references
- Voltage supply level
- Temperature of the chips

Errors are checked at each margin parameter setting. The resulting pass/fail matrix gives an engineer the solution space in which the system can operate without fault. By using the SMV method, worst case patterns can be identified.

A useful representation of the SMV results is a Functional Eye, also known as Data Eye. It is a two-dimensional chart, where each axis represents a different margin parameter. An example of a functional eye can be seen in Figure 6. When a test uses a single margin parameter, it is called one-dimensional test.

Figure 6. Example of SMV Functional Eye



Existing Solutions

We did analysis of available external solutions. Some of the external solutions use a logic analyzer, but they probe the DisplayPort signals in the middle of the bus, called midbus probing, and do not use a standard DP receiver. These methods are not signal-integrity friendly, i.e., the probing affects the measured signal itself, a condition which does not reflect the final product's environment. Moreover, being compatible with the DisplayPort connector, these solutions are physically not compatible with eDP.

The prevalent external DisplayPort tests provide validation of the interface's electrical parameters and conformity with the physical layer (PHY) Compliance Test Specification (CTS) of VESA. This is done by sampling the DisplayPort signal with an oscilloscope and appropriate test adaptor. These tests measure electrical parameters like jitter, pre-emphasis, signal's amplitude, rise/fall times, etc.

Another major part of test solutions available in the market is checking conformity with the Link Layer Compliance Test Specification. The test equipment used here comprises of different DisplayPort protocol analyzers. Some of the tested functions are training sequence, protocol's features check, sending commands over control lines, Cyclic Redundancy Check (CRC), etc. These tests do not include any electrical check of PHY.

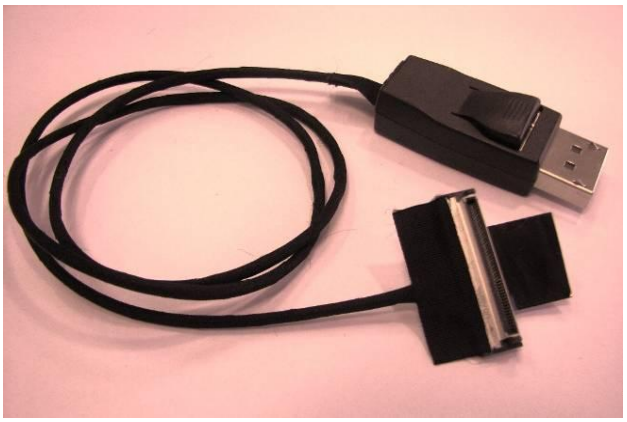
Hardware and Software Uniqueness

eDP*-to-DisplayPort* Cable

A specially designed eDP-to-DisplayPort cable is needed (see Figure 7) because of the physical incompatibility of the eDP Tx and DisplayPort Rx connectors. Since the eDP and DisplayPort standards are very similar, only a passive cable is needed, no level shifting.

The DisplayPort connector has 20 pins, which include four differential lanes of the main link, a differential auxiliary channel (AUX) for slow speed control, Hot-Plug Detect signal (HPD), ground pins, CONFIG control pins, and two power pins. The eDP connector has those and additional optional pins, like brightness control, backlight and ambient light sensing. The eDP standard allows various connectors with 44/40/30/20 pins. However, this paper demonstrates only the 44-pin connector, since the others follow similar principles. Another reason for showing the 44-pin connector is that it used on Intel's Customer Reference Boards (CRB).

Figure 7. eDP*-to-DisplayPort* Cable Assembly



The typical cable's part number is LA10EM006-2N. Its length is 22'' (559 mm). The cable length has to match 4 db insertion loss at 1.35 GHz. The frequency of 1.35 GHz is the first harmonic of the 2.7 Gb/sec DisplayPort data signal. The data lanes' wires are twin-ax coaxial cables.

Several other cables, which customers may put in their systems, can be tested:

- Different cable lengths - 16'' and 28'', not only 22'';
- A cable with coaxial wires (not twin-ax) for the main lanes;

- Cables with the high-speed ground pins connected to the common GND bar, and not passing through separate wires.

An interconnection pin-map between eDP and DisplayPort connectors of the cable is shown in Table 2.

Table 2. Pin-map of the eDP*-to-DisplayPort* Cable

Signal Name	Pin Number	
	44-pin eDP connector	20-pin DP connector
N.A. (not applicable)	1	-
N.A. (not applicable)	2	-
N.A. (not applicable)	3	-
N.A. (not applicable)	4	-
N.A. (not applicable)	5	-
GND (Power Return)	6	GND shield, 13, 14
GND (Power Return)	7	GND shield, 13, 14
GND (Power Return)	8	GND shield, 13, 14
GND (Power Return)	9	GND shield, 13, 14
Hot Plug Detect (HPD)	10	18
N.C. (no connection)	11	-
N.C. (no connection)	12	-
H_GND - High Speed (Main Link) Ground	13	2
Lane 3(n)	14	1
Lane 3(p)	15	3
H_GND - High Speed (Main Link) Ground	16	5
Lane 2(n)	17	4
Lane 2(p)	18	6
H_GND - High Speed (Main Link) Ground	19	8
Lane 1(n)	20	7
Lane 1(p)	21	9

Signal Name	Pin Number	
	44-pin eDP connector	20-pin DP connector
H_GND - High Speed (Main Link) Ground	22	11
Lane 0(n)	23	10
Lane 0(p)	24	12
H_GND - High Speed (Main Link) Ground	25	16
AUX_CH (p)	26	15
AUX_CH (n)	27	17
N.A. (not applicable)	28	-
AUX Power	29	-
N.C. (no connection)	30	-
N.A. (not applicable)	31	-
N.A. (not applicable)	32	-
GND	33	GND shield, 13, 14
N.A. (not applicable)	34	-
N.A. (not applicable)	35	-
N.A. (not applicable)	36	-
N.A. (not applicable)	37	-
N.A. (not applicable)	38	-
N.A. (not applicable)	39	-
GND	40	GND shield, 13, 14
N.A. (not applicable)	41	-
N.A. (not applicable)	42	-
N.A. (not applicable)	43	-
N.A. (not applicable)	44	-

DisplayPort* Capture Card

The UFG-04 DisplayPort capture card, also known as a frame grabber, includes a standard DisplayPort Sink connector. Using a particular DisplayPort receiver in the test setup does not guarantee coverage of all the existing receivers. Nevertheless, using a standard DisplayPort receiver leads to much better fidelity to the case of real customers' system than using signal probing, e.g., midbus probe.

The card's DisplayPort receiver is based on a GM 68020 receiver chip. Up to four lanes are supported, the full DisplayPort link width. This is a PC expansion card with a PCIe* x1 interface. The card has a 2 Gb on-board DDR memory, which serves to store received frames. The maximal supported resolution is WQXGA (2560 x 1600).

Captured frames can be saved to disk in binary .ppm file format. Various link statuses are available for reading, e.g., clock recovery, symbol lock and CRC. You can access the Extended Display Identification Data (EDID) register and the DisplayPort Configuration Data (DPCD) register, which allows emulating various screen types and configurations.

Software and Automation

We chose the Python* programming language to implement our software part. A small part of the code, the eDP functional test (eDPFS), was written on C++ programming language.

The software runs an automatic test performing the following steps:

- Loads an image from a file into the frame buffer of the eDP Source.
- Captures the received image and compares it to the sent image, pixel by pixel.
- Sweeps the SMV margin parameter via all test points, up to a link failure.
- Reports the results into a file.
- The test is launched from Python. Its main input parameters are:
- Image pattern filename
- Test repetitions number
- Number of captured and compared images on each margin step
- Margin parameter, by now only Tx amplitude swing
- Number of mismatched pixels to indicate a fail condition for the test. By default the pass/fail criteria is at least one mismatched pixel in an image.

In the report file we get a table which includes the following output parameters:

- First margin step when an image mismatch has been detected.
- First margin step with broken eDP link - equals or greater than the first failed step.
- Number of mismatched pixels on each margin step.
- In addition, the test reports setup related parameters. The main parameters are:
- Repetition number
- CPU temperature
- CPU Vccp voltage
- CPU serial ID
- Image pattern filename

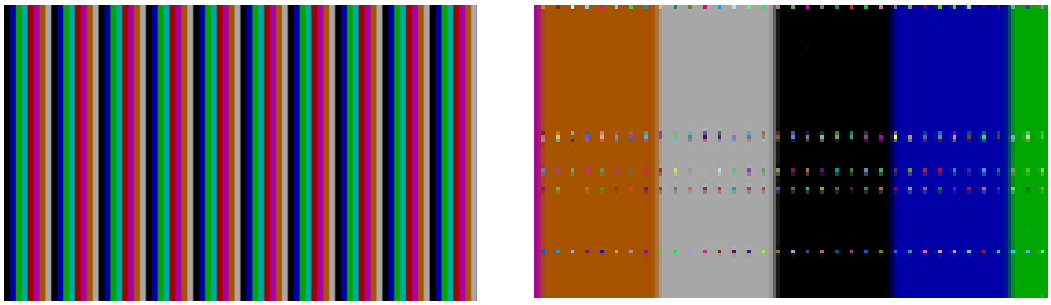
Various input images can be tested and their margin can be compared. This way the test can help to look for worst case images (worst case patterns).

Test software can be designed to be located on the host, or to be partitioned between the host and the system under test. We chose it to be partitioned. The part of the test that runs on IA cores of the DUT runs faster because it is very close to the eDP Source. By now the only part of the test running on the DUT loads an image data image into the CPU display-engine's frame buffer. The program, also known as eDPFS, is loaded into the cache memory of the CPU either using the JTAG Loader or using the PCIe-bridge card.

Results

A sample of the resulting data is presented below; it was obtained from one of the first eDP test runs on a CPU. We used a 22'' cable, part number LA10EM003-3N. This cable is the longest in our set and expected to introduce the least margin. The CPU voltage and case temperature conditions were set to typical, 1.05 Volt and 60°C. The test pattern was a color bars image with resolution of 2560x1600; a sample is shown in Figure 8. Because the error dots are very hard to see, a zoom of the image is shown.

Figure 8. Color Bars Test Image (left) and Zoomed Image With Errors (right)

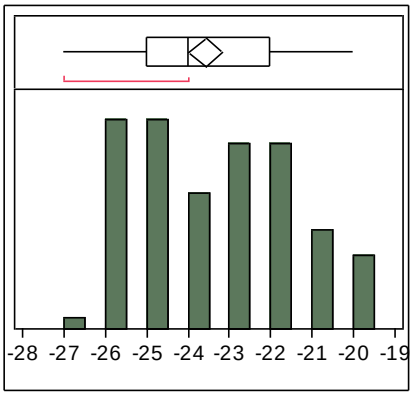


Ten (10) CPU units were tested, while each unit ran 8-10 repetitions. The distribution below shows the detected eDP margin (Figure 9).

The worst case margin seen was 20 steps, which means that first fails occurred when the signal's swing went below about 160mV ptp-differential. If, for example, we normally worked with swing of 400mV, then we had a sufficient margin of 240mV. This margin provided good immunity from noise and manufacturing process variations.

Note: The steps were calibrated using a clock pattern, as described in the section of Complete Test Setup; the actual swing is slightly higher, depending on the pre-emphasis level used.

Figure 9. First Failed Step Distribution

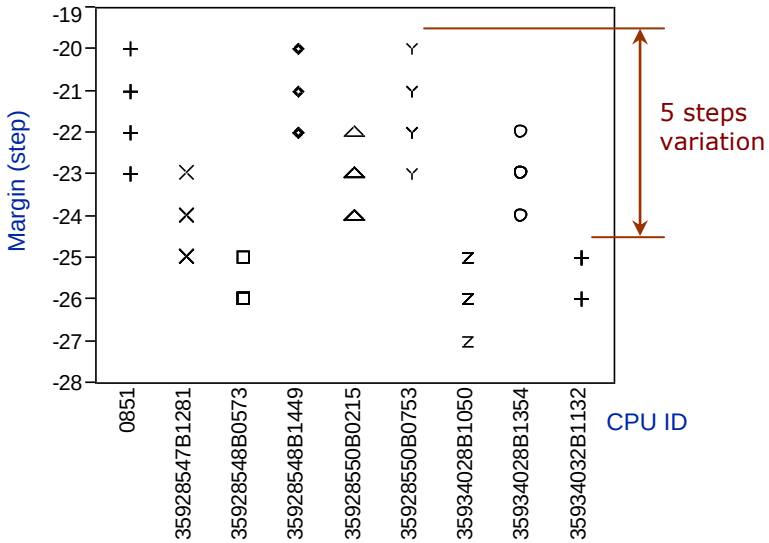


Quantiles		
100.0%	maximum	-20.00
99.5%		-20.00
97.5%		-20.00
90.0%		-21.00
75.0%	quartile	-22.00
50.0%	median	-24.00
25.0%	quartile	-25.00
10.0%		-26.00
2.5%		-26.00
0.5%		-27.00
0.0%	minimum	-27.00

Moments	
Mean	-23.56667
Std Dev	1.8964781
Std Err Mean	0.1999063
upper 95% Mean	-23.16946
lower 95% Mean	-23.96388
N	90

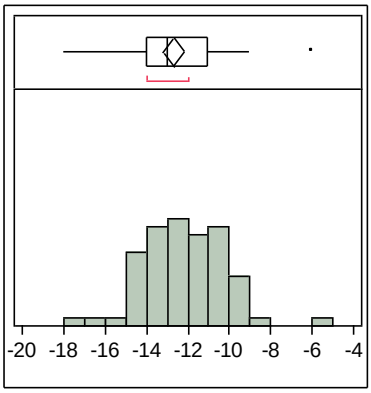
Figure 10 shows unit-to-unit variation. We observed five steps variation between the worst cases.

Figure 10. Unit-to-unit Variation



Based on eight of the CPU units, we have a distribution (see Figure 11) of difference between the last step of the live link, and the first failed step. The link is functioning in the range between those two margin steps, although the received image has errors.

Figure 11. A Difference Between: (Last step of live link) - (First failed step)



Quantiles		
100.0%	maximum	-6.00
99.5%		-6.00
97.5%		-8.18
90.0%		-10.00
75.0%	quartile	-11.00
50.0%	median	-13.00
25.0%	quartile	-14.00
10.0%		-15.00
2.5%		-17.28
0.5%		-18.00
0.0%	minimum	-18.00

Moments	
Mean	-12.67647
Std Dev	2.0032897
Std Err Mean	0.2429346
upper 95% Mean	-12.19157
lower 95% Mean	-13.16137
N	68

Another test, which was manually done with an eDP flat panel, showed a very good margin, without any visual image defects noticed throughout the whole margin parameter's range. The eDP flat panel is actually a notebook's display with an eDP input. This specific panel was a CMO eDP606 with an LED backlight panel, and a 1366x768 resolution. The test was done manually just by changing the Tx swing and looking at the display because the DUT was connected to a real display, not a capture card, so no automatic flow could be implemented. This good result was double-checked; the link is functional with a Tx swing as low as 60mV. This result exhibits the high quality of the cable assembly and/or Rx circuit of this panel.

Conclusion

The presented results proved that the new functional eDP test is not just theoretical but effectively operational. Currently proposed methodology allows many units and repetitions to run while doing this on many systems at an affordable price and time. This test can do a wide coverage and is quite compatible with customer's environment.

This methodology has the potential of expanding validation to other video links like DVI and HDMI. This would allow reducing the cost of not only the eDP and DisplayPort tests, but of other tests too.

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Acronyms

AUX	Auxiliary Channel
CPU	Central Processing Unit
CRB	Customer Reference Boards
CRC	Cyclic Redundancy Check
CTS	Compliance Test Specification
DFT	Designed for Test
DOE	Design of Experiment
DPCD	DisplayPort* Configuration Data
DUT	Device Under Test
EDID	Extended Display Identification Data
eDP	Embedded DisplayPort*
eDPFS	eDP functional test
GPU	Graphics Processing Unit
HPD	Hot-Plug Detect signal
HVM	High Volume Manufacturing
IA	Intel® Architecture
I/O	Input/Output
LA	Logic Analyzer
MPD	Mobile Products Development
PCIe*	PCI Express*
PHY	Physical Layer
SI	Signal Integrity
SMV	System Marginality Validation
VESA	Video Electronics Standards Association
XDP	Extended Debug Port

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