White Paper
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Migration to New Display Technologies on Intel Embedded Platforms

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Executive Summary

With the introduction of Intel's latest embedded platforms comes support for the widest selection of display interfaces. However, going forward into future platforms, the choice of display interfaces will decrease, removing legacy solutions and causing board designers to make choices in the types of interfaces to support. This paper describes the various new and legacy display technologies of Intel's platforms (VGA, TV-OUT, LVDS, SDVO, DVI, HDMI, DisplayPort, Embedded DisplayPort) along with detailing differences in display interfaces between the various scalable/low-power platforms offered during 2009-2012. To aid designers in taking advantage of expanding the scope of displays natively available on a platform, the topics of passive/active dongles, alternative solutions for obtaining legacy display support in future platforms, and ways of obtaining additional displays beyond what platforms natively offer are detailed. The particular platform datasheet of interest should be reviewed for a complete list of supported features.

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Introduction

Background

Each year Intel evolves the display interfaces available for designers on scalable/low-power platforms. Understanding the value, capability, and forward-looking stance of each interface aids system integrators in making the right selection of platform and display interfaces for their design.

Purpose of Document

The purpose of this document is to describe the various display interfaces of Intel's scalable/low-power platforms and discuss methods by which designers may expand the scope of displays natively available on a platform.

Comparison of Display Technologies

Several different display interfaces exist on the latest Intel Low Power and Scalable Embedded platforms. These include VGA, TV-OUT, LVDS, SDVO, DVI, HDMI, DP, and eDP. An overview of each interface follows.

VGA

The legacy analog interface of Video Graphics Array (VGA) was introduced by IBM* in 1987 and is typically used in driving CRTs, flat panels, HD-TVs, and projectors. The standard VGA connector defined is a 15-pin d-sub mini, composed of red, green, blue, horizontal & vertical sync video signals, a VESA Display Data Channel (DDC) for communication of display configuration data, and a clock signal. There are no defined standards related to image quality or maximum resolution supported by the interface, but Intel typically provides a Digital to Analog Converter (DAC) that will increase frequency up till 340MHz depending on the resolution desired. There is no licensing fee associated with utilizing this interface and no content protection or audio signals are provided.

TV-OUT

TV-OUT is another legacy analog video signal developed for television equipment. This interface is realized by providing three 10-bit DAC channels, which when used in various combinations, can form composite video, S-video, and component video signals. These video signals are usually used in the transmission of the standard television video formats: NTSC, PAL, and SECAM. Composite video, originally intended for broadcast media, uses one

DAC and contains all signal information on one pair of wires. S-video introduces a second pair of wires to reduce signal interference and makes use of another DAC to increase video quality. This interface was prevalent with the introduction of the videocassette recorder (VCR). Component video, popular with the introduction of the Digital Video Disc (DVD), uses all three DACs and separates the signaling over multiple signal pairs to produce the highest quality TV-OUT video signal.

LVDS

Introduced in 1994, Low-Voltage Differential Signaling (LVDS) is a low voltage digital method of transferring information at high data rates. The most common application of the LVDS protocol is in driving embedded flat panel displays. There is no standardized connector defined, but signals consist of dedicated data pin pairs, clocking, backlight control, power panel sequencing, and I2C signals for EDID data. Depending on the maximum resolution needed by the display, LVDS supports both single and dual link modes. A variable frequency pixel clock of either 25-112 MHz (single wide) or up to 224 MHz (dual wide) provides support for resolutions of up to 1400x1050 @ 60 Hz or 2048x1536 @ 60 Hz respectively. Since this is considered to be an embedded system display technology, hotplug support, content protection, and audio signals are not included features.

SDVO

Intel created a non-standard extension of the PCI Express interface called Serial Digital Video Output (SDVO) to allow support for display devices not natively supported by Intel chipsets. The SDVO specification was adopted by 3rd party device manufacturers such as Chrontel and Silicon Image to produce devices which would accept SDVO signals and allow for outputs such as VGA/LVDS/HDMI/DVI/TVOUT. Implementation and specific feature support may vary from vendor to vendor, but SDVO is based on a signal set of four lanes – three for pixels and timing data with one for a reference clock. It is based on a variable frequency of between 100-225 MHz. DDC sideband communication, an interrupt pin, and external clock input source pin pairs are included for those interfaces which may require them. However, with the introduction of native support for most digital interfaces within Intel chipsets, the need for SDVO has diminished and plans to phase out support of the interface within the platform have been established.

DVI

The Digital Video Interface (DVI) was designed by the Digital Display Working Group (DDWG) industry consortium in 1999 to replace the legacy VGA connector technology and allow for digital transmission of uncompressed display data. It has established itself as a widely accepted digital interface in the PC and external monitor market, along with support in other consumer devices. The signaling interface is based on Transition-Minimized Differential Signaling (TMDS) and 8b10b encoding to allow for efficient and reliable data

transmission at high speeds. A set of four TMDS lanes exist with three lanes dedicated to pixels and timing information and one lane for clocking information. A single-link DVI interface supports a variable pixel clock frequency of between 25-165 MHz and can support a maximum of 24 bits per pixel. At a pixel clock of 165 Mhz, one can obtain a resolution up to 1920x1200 @ 60 Hz with 24 bpp. If a higher pixel bandwidth is needed, devices can implement dual-link DVI which would double the number of TMDS lanes, allowing for resolutions up to double the bandwidth of single-link mode. Dual-link DVI mode is currently not supported on Intel platforms. In addition to data and clock signals, DVI supports DDC for communication of display data and contains a hot plug detect signal. A variety of DVI connectors exist. DVI-D indicates digital only and allows support for single and dual-link DVI implementations. DVI-A provides pins to support the same analog signals found on VGA connectors. DVI-I allows for support of both digital and analog VGA devices.

HDMI

The High Definition Multimedia Interface (HDMI) was driven by industry consumer electronics vendors in 2002. It was the first interface to combine audio and video, along with adding support for content protection (HDCP). In addition, it is backwards compatible with the DVI interface with regards to video compatibility. Primarily found in digital flat panels and consumer televisions, the HDMI interface is based off TMDS specifications (as with DVI). A set of four TMDS lanes exist, with three lanes dedicated to pixels and timing information and one lane for clocking information. A variable frequency pixel clock rate ranging from 25-340 MHz is provided across a single digital link, allowing for a maximum resolution of 2560x1600 @ 60Hz. Video, audio, and auxiliary data is transmitted through the TMDS data lanes, while separate DDC signals transmit monitor display information. While Intel does not directly support via hardware or software, and optional Consumer Electronics Control (CEC) feature provides flexibility for devices that support CEC to command and control each other. If CEC support is desired, third party vendors create devices which can be included on board designs and can interpret these commands. Hot plug detect is also a feature of the HDMI interface. The latest specification (HDMI 1.4) provides for advanced features such as Deep Color (36 bits per pixel), 3D, Ethernet, audio return channel and 4kx2k resolution support which are not required for compliance but optional depending on the platform. There is a royalty associated with using the HDMI interface that system manufacturers will have to account for. More information can be found on the HDMI.org website.

DisplayPort

The Video Electronics Standards Organization (VESA) defined a new digital display interface standard DisplayPort (DP) in 2006, with the intention of displacing the legacy VGA and DVI interfaces. It provides the ability to support both audio and video content simultaneously or independently. With these characteristics, the interface is primarily targeted to support LCD flat

panels, televisions, and projectors. DisplayPort is the first display interface to not implement differential signaling as do the other display interfaces. Instead, DisplayPort is based on packetized signaling, similar to the way Ethernet or USB operate. This allows for additional features to be supported by the specification as introduced and reduces the number of signals to be routed on board designs. From one to four data lanes of 8B10B encoded data may be supported depending on the resolutions required of the platform. There are no separate clocking signals, as the clock is embedded in the data. Clocking rates of 162, 270, or 540 MHz are supported based on the maximum pixel rate of the supporting specification. DP 1.1 supports resolutions of up to 2560x1600 @ 60 Hz. However, with the most recent revision, DP 1.2, resolutions of up to 3840x2160 @ 60 Hz are supported due to the increase in data bandwidth. Colors of up to 36 bits per pixel are supported by the DisplayPort interface. In addition to the data signals, a hot plug detection and bi-directional auxiliary channel is provided for sideband device management and/or USB communication. Content protection is provided through the High-Bandwidth Digital Content Protection (HDCP) industry standard. DisplayPort is a royalty-free display interface and more information can be found on the VESA.org website.

Embedded DisplayPort

Embedded DisplayPort (eDP) is a companion standard to DisplayPort. The signaling protocol is based off of the DisplayPort standard, but primarily support for features such as backlight control, power panel sequencing, refresh rate switching, and panel self-refresh have been added to the Embedded DisplayPort specification to extend the life of portable devices where Embedded DisplayPort is typically used. The same signal characteristics of DisplayPort apply to Embedded DisplayPort. Expectations are that Embedded DisplayPort will displace LVDS, as Embedded DisplayPort results in fewer signals required, smaller connectors, lower power on Intel-based platforms, and reduced electromagnetic radiation. Additional information can be found on the VESA.org website.

# *Device Capability Evolution of Intel 4/5/6/7 Series Chipset based Platforms*

Intel platforms with integrated graphics have undergone significant advancements and architectural changes over the last four product generations. This section details those differences.

Intel® 4 Series Chipset based Platform

The Intel® 4 Series Chipset based Platforms (first introduced in 2008) are based on a three chip platform composed of the CPU, GMCH, and ICH. All graphical processing capabilities resided within the GMCH, in addition to the memory controller for DRAM system memory as pictured below. There is a dedicated VGA port, two digital ports with configurability to output DP 1.1a / HDMI 1.3a with lipsync and premium audio / DVI / SDVO, and a PCI Express Graphics (PEG) option for using a discrete graphics card. Integrated LVDS is provided on mobile versions of the GMCH or via SDVO on all designs with the SDVO interface. While using integrated displays, two displays may be active simultaneously with unique or replicated content. See Figure 1 for a visual representation.

Figure 1. Intel® 4 Series Chipset Based Platform
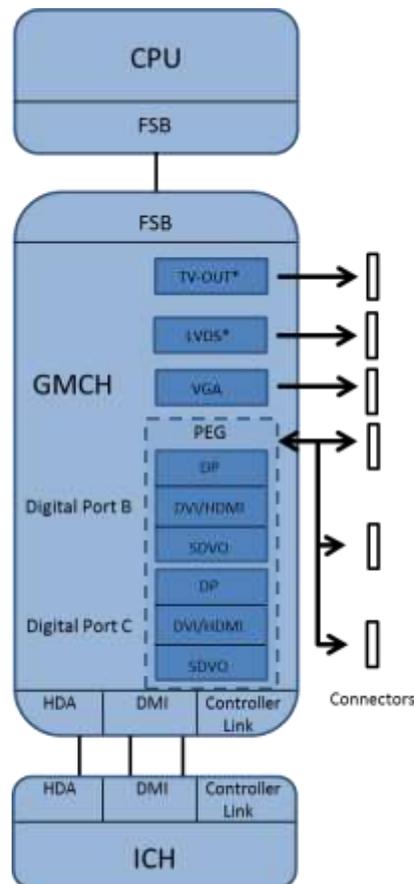
Intel® 5 Series Chipset based Platform

With the introduction of the Intel® 5 Series Chipset based platforms in 2010, the graphics processing unit silicon was combined in the same external package as the CPU. This helped to increase system integration, reduce routing complexity, and improve power management capabilities. Therefore, a platform was composed of a CPU and Platform Controller Hub (PCH). The graphical processing unit in the CPU performed the graphical computations, while the display portion of the graphics engine resided in the PCH. This created the need for a new bus which is called the Intel® Flexible Display Interface (Intel® FDI) to transfer display output from the CPU to the PCH. The PCH provided three digital ports which can be configured to support combinations of DP 1.1a with 2-channel audio support / HDMI 1.3a with Deep Color, xvYCC, and premium audio support / DVI, with SDVO only being supported on Port B. LVDS (mobile only) and VGA resided as outputs from the PCH. eDP was introduced on this platform (mobile only) as an output from the CPU, along with an eDP option from Port D of the PCH. As with the previous generation platform, when using integrated displays, two displays could be active simultaneously with unique or replicated content. However, only a single embedded display type (eDP or LVDS) may be in operation at a time due to the fact that there was only being a single set of backlight control signals provided. When using SDVO-LVDS on the other hand, dual embedded display operation was available as the SDVO chip is able to provide its own set of backlight control signals. A PEG option resided on the CPU. See Figure 2 for a visual representation.

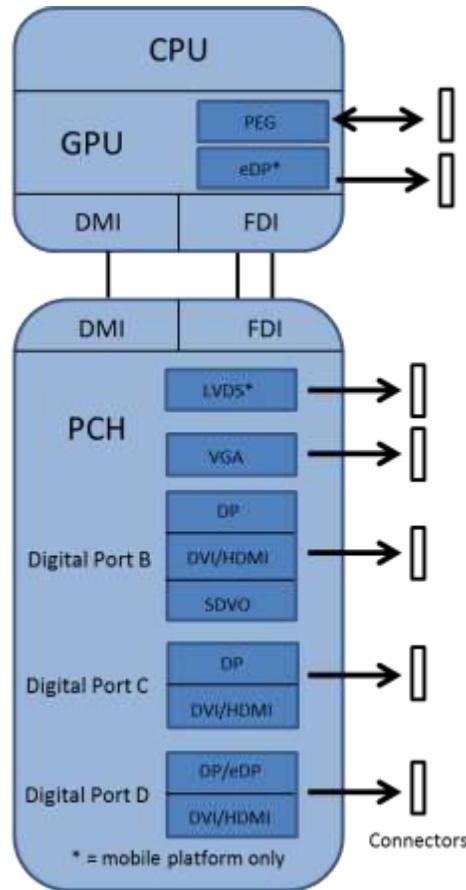**Figure 2. Intel® 5 Series Chipset Based Platform**
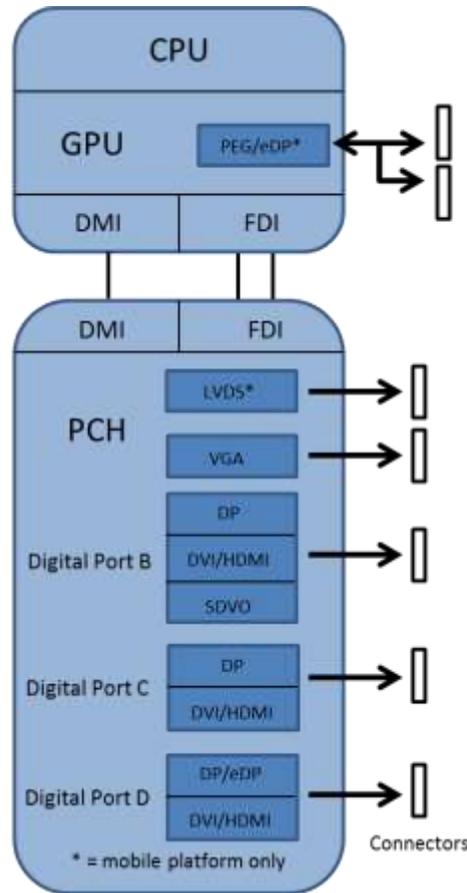
Intel® 6 Series Chipset Based Platform

The Intel® 6 Series Chipset based platforms in 2011 combined silicon from the CPU and the graphics processing unit into one single piece of silicon within the same package. This worked in conjunction with the PCH to allow for the same functional capabilities as that of the Intel® 5 Series Chipset based platforms mentioned above with the exception that on the Intel 6 Series Chipset based platforms, the eDP output from the CPU was not multiplexed off of the PEG, while on Intel 5 Series Chipset based platforms it was multiplexed off of the PEG. The PCH provided three digital ports which can be configured to support combinations of DP 1.1a with 2-channel audio support / HDMI 1.4 with S3D / DVI, with SDVO only being supported on Port B. See Figure 3 for a visual representation.

Figure 3. Intel® 6 Series Chipset Based Platform

Intel® 7 Series Chipset based Platform

The Intel® 7 Series Chipset based platforms launched in 2012 carry forward the same display options of the Intel® 6 Series Chipset based platforms and yet allow for support of up to three simultaneous active displays showing independent or replicated content. Refer to Figure 4 for a platform level diagram. The PCH provided three digital ports which can be configured to support combinations of DP 1.1a with premium audio support / HDMI 1.4 with S3D / DVI, with SDVO only being supported on Port B. See the following section 'Configuration Possibilities for 3 Displays on Intel 7 Series Chipset based Platforms' for limitations which may apply.

Figure 4. Intel® 7 Series Chipset Based Platform
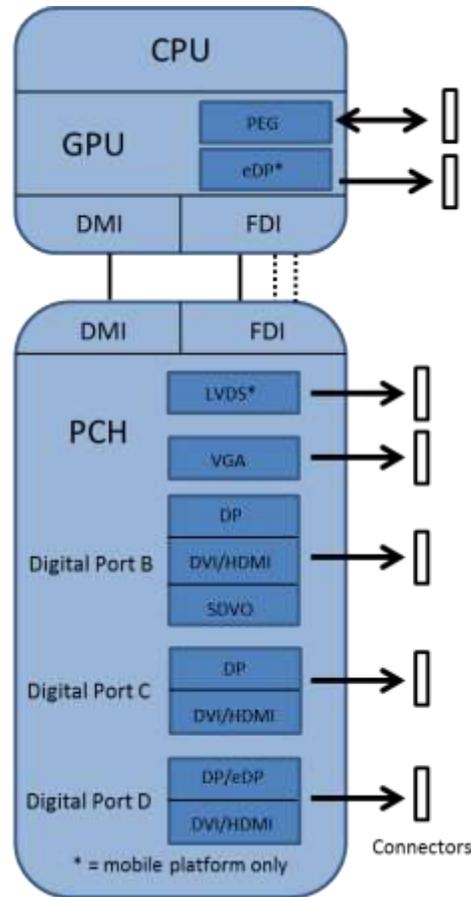
Configuration Possibilities for 3 Displays on Intel 7 Series Chipset based Platforms

The Intel® 7 Series Chipset based platform allows for the support of up to three concurrent displays with independent or replicated content. However, this comes with the requirement that either one of the displays is eDP running off the CPU or two DP interfaces are being used off the PCH. When configuring the 2 DP interfaces from the PCH, one may be an eDP if using Port D. This limitation exists because the 7 Series Intel PCH contains only two display PLLs (the CPU has one display PLL also) which will control the clocking for the respective displays. All display types other than DP have an external variable clock frequency associated with the display resolution that is being used. The DP interface has an embedded clocking scheme that is semi-variable, either at 162 or 270 MHz depending on the bandwidth required. Therefore, Intel only allows sharing of a display PLL with DP related interfaces.

The Intel® Flexible Display Interface (Intel® FDI) is a digital interface which connects the CPU to the PCH. Intel's 5, 6, and 7 Series Chipset based platforms each contain two links (A and B) of up to 4 lanes each that dynamically utilize between one to four lanes depending on the resolution and color type being displayed off the PCH interface. Each link has the bandwidth to support up to a maximum resolution of 2560x1600 @ 60 Hz. However, with the Intel® 7 Series Chipset based platforms, link B has the dynamic capability to split its four lanes into a pair of two lanes, allowing for two displays to be supported off of one link. When split, each pair of lanes is capable of supporting up to a maximum resolution of 1920x1200 @ 60 Hz. Of course, by using the eDP display interface from the CPU, the need to have FDI link splitting disappears, allowing support for full bandwidth on each link of up to a resolution of 2560x1600 @ 60 Hz. The diagrams below help indicate architectural operation of two scenarios of display arrangements – (1) one eDP display driven from the CPU and two displays of any type driven from the PCH (Figure 5), (2) two DP displays and another display of any type (Figure 6). Table 1 shows valid multi display support combinations on Intel 7 Series Chipset based platforms.

Figure 5. Intel® 7 Series Chipset Based Platform Triple Display Scenario #1
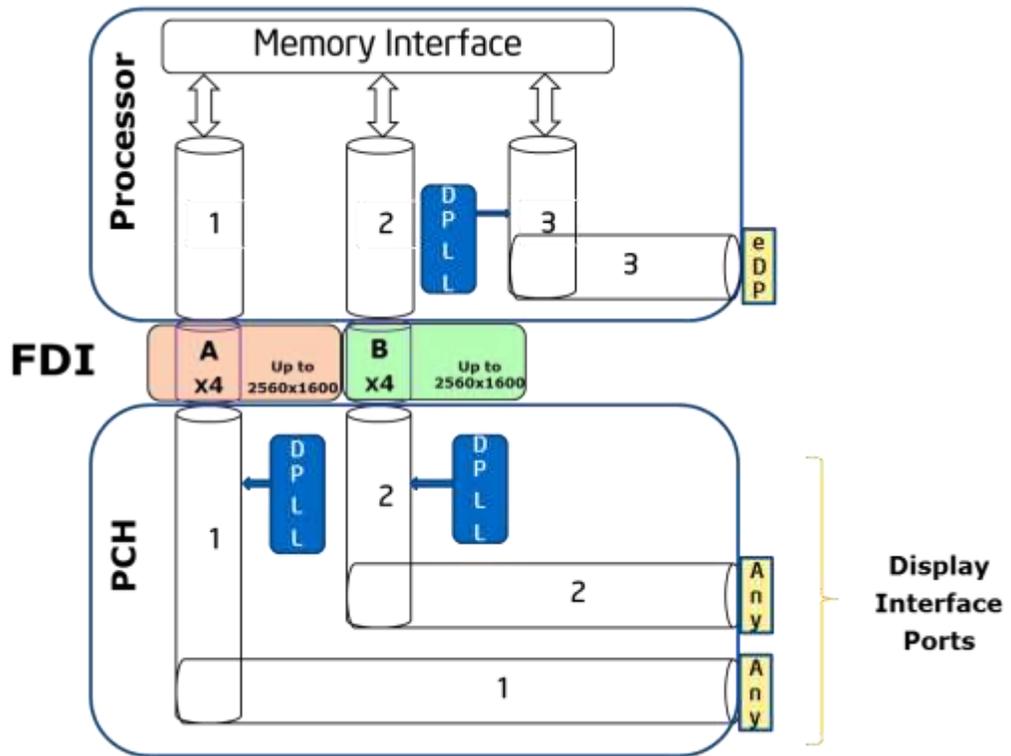
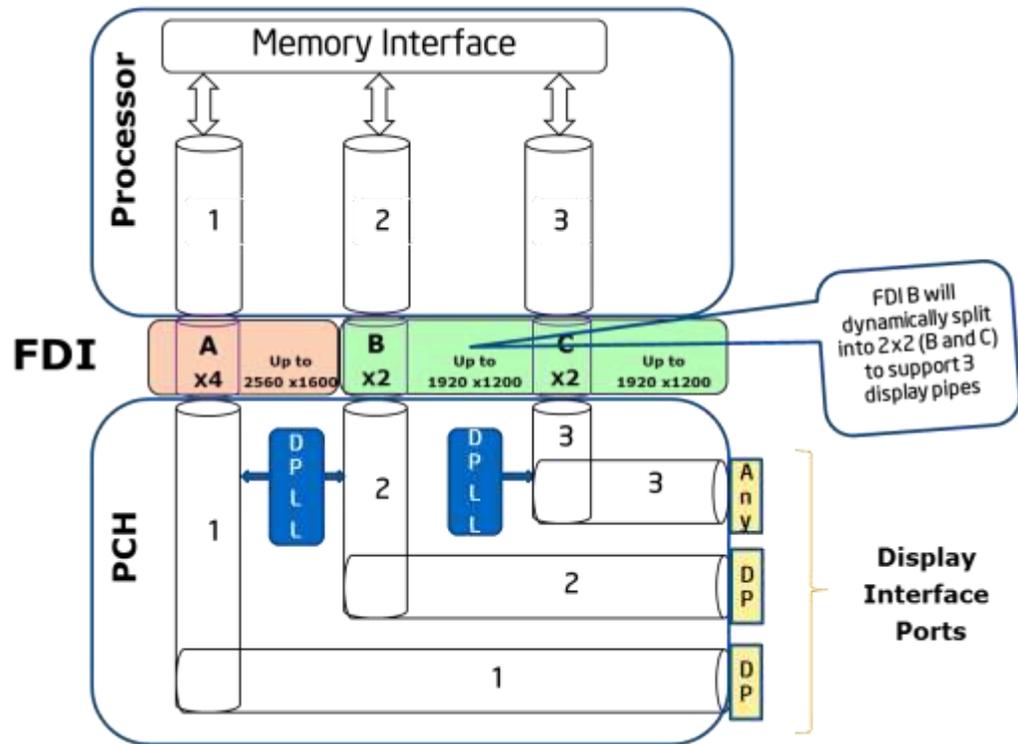**Figure 6. Intel® 7 Series Chipset Based Platform Triple Display Scenario #2**

Table 1. Intel 7 Series Chipset Based Platform Multi Display Support

	Active Display 1	Active Display 2	Active Display 3
Single Display	Any Display (up to 2560x1600 @ 60 Hz, 8 bpc)	-	-
Dual Display	Any Display (up to 2560x1600 @ 60 Hz, 8 bpc)	Any Display (up to 2560x1600 @ 60 Hz, 8 bpc)	-
Triple Display (Mobile Only)	e-DP (CPU) (up to 2560x1600 @ 60 Hz, 8 bpc)	Any Display (up to 2560x1600 @ 60 Hz, 8 bpc)	Any Display (up to 2560x1600 @ 60 Hz, 8 bpc)
Triple Display (Mobile & Desktop)	DP (up to 2560x1600 @ 60 Hz, 8 bpc)	DP (up to 2560x1600 @ 60 Hz, 8 bpc)	Any Display (up to 1920x1080 @ 60 Hz, 8 bpc)

*Any Display = LVDS/CRT/HDMI/DVI/DP/eDP/SDVO

Passive/Active Dongles

With the display interface limitations highlighted previously on the Intel® 7 Series Chipset based platforms, interest has developed in seeking alternatives to obtain display support combinations which are not natively possible on the platform. Solutions exist in the realm of dongles. Display adaptor dongles allow for the conversion from one display interface to another. Solutions exist for nearly every display type, with the most popular being DP -> HDMI/DVI. This paper discusses two classes of adaptor dongle: passive and active.

Since DP and HDMI/DVI are digital interfaces, conversion between the three is relatively straightforward through the use of level shifters and multiplexing of signals over the appropriate interface pins. Passive dongles are those used to convert between display interfaces using this method. No protocol conversion is done in the dongle itself, and the PCH and software graphics driver are aware of the presence of the dongle and will adjust data output characteristics appropriately (those characteristics being display data format and interface pins in use – AUX for DP, DDC for HDMI/DVI). Since different pins are used for sideband communication of display and audio (optional) information, the use of passive dongles requires the implementation of what is referred to as a DisplayPort Interoperability Circuit (detailed in the DisplayPort Interoperability Guideline Version 1.1a from VESA). By implementing this circuitry on board designs, platforms will take advantage of Pin 13 on passive dongles, which indicates the presence of a dongle to be communicated back to the CPU/PCH.

When the need arises to convert between digital and analog display interfaces, active dongles are required. Active dongles provide protocol conversion and contain component circuitry for this process. Because of the need for active components, these dongles are typically larger in size compared to their passive dongle counterparts. Additionally, these dongles do not result in an interrupt or message sent to the CPU/PCH through any standardized interface pin. The graphics engine will see these active dongles as a DisplayPort interface regardless of the type of terminating display interface. Therefore, there is no need for an interoperability circuit on board designs that may utilize these dongles, and the PCH and software graphics driver are not aware of the presence of the dongle. This means that it may be possible for end users or platform integrators to obtain support for display combinations not allowed for natively in the platform by converting DP outputs into other display types. For example, one may obtain support for three HDMI interfaces by using three active DP -> HDMI dongles, or by using one passive DP -> HDMI dongle and two active DP -> HDMI dongles in the same system. Consideration should be taken into account that cost for passive versus active dongles will vary as well, with active dongles typically priced higher.

When using passive or active dongles, it is important for the board or system integrator to carefully complete validation activities related to the use of the

dongles. Intel does not claim compatibility or support for particular dongles provided by third party vendors. Therefore, it is recommended that customers experiencing issues with these devices to contact the dongle/device vendor to address compatibility issues.

Legacy Display Support

In 2010, Intel and other leading PC companies announced that the legacy VGA and LVDS display interfaces would no longer be supported in new product lines in the 2015 timeframe (refer to http://newsroom.intel.com/community/intel_newsroom/blog/2010/12/08/leading-pc-companies-move-to-all-digital-display-technology-phasing-out-analog). Another interface popular with embedded customers, SDVO, will also be phased out of new product lines in 2013. Because of the native implementation of digital interfaces, the need for SDVO has diminished. The focus will be for customers to adopt the more recent digital interfaces. However, shall the need exist for customers to support legacy VGA or LVDS interfaces, this may be accomplished through the use of active dongles as described in the previous section or through on-board third party components.

Support for Additional Displays

With the introduction of the Intel® 7 Series Chipset based platform, Intel has increased the number of supported active displays from two to three. However, for some embedded customers, that number is still not enough to satisfy their platform needs. If additional displays are required some third party options exist. By using a discrete graphics card operating in conjunction with Intel's integrated graphics solution, a mode termed Hybrid Multi-Monitor can exist where both integrated and discrete displays are being driven. Please refer to Document #323214 'Hybrid Multi-Monitor Support' White Paper for more detail on implementation of Hybrid Multi-Monitor on embedded platforms. Another solution is USB-driven displays, which may be attractive for some customers. Third party vendors currently provide solutions for HDMI/DVI/VGA output at up to HD resolutions with audio support.

Conclusions

Intel's latest 7 Series Chipset based platforms offer the widest selection of supported display interfaces and, with support for up to three simultaneous active displays with independent or replicated content, provide compelling display options for embedded platforms. Going forward, customers should

focus on adopting the digital display interfaces into their platforms and, if needed, provide support for legacy interfaces through active dongle adapters. Display capabilities continuously evolve and Intel is committed to seeking the most suitable solutions for our embedded customers.

For additional design assistance or technical resources related to this topic please refer to http://intel.com/embedded/edc.

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Author

David Galus is a Graphics Platform Application Engineer with Intel's Intelligent Systems Group.

Acronyms

AUX – Auxiliary

BPP – Bits Per Pixel

CEC – Consumer Electronic Control

CPU – Central Processing Unit

CRT – Cathode Ray Tube

DAC – Digital-to-Analog Converter

DDC – Display Data Channel

DDWG – Digital Display Working Group

DP – DisplayPort

DRAM – Dynamic Random Access Memory

DVD – Digital Video Disc

DVI – Digital Visual Interface

EDID – Extended Display Identification Data

eDP - Embedded DisplayPort

FDI – Flexible Display Interface

GMCH – Graphics Memory Controller Hub

GPU – Graphics Processing Unit

HD – High Definition

HDCP – High-bandwidth Digital Content Protection

HDMI – High Definition Multimedia Interface

ICH – I/O Controller Hub

LCD – Liquid Crystal Display

LVDS – Low-Voltage Differential Signaling

NTSC – National Television System Committee

PAL – Phase Alternating Line

PCH – Platform Controller Hub

PCI – Peripheral Component Interconnect

PEG – PCI Express Graphics

PLL – Phase-Locked Loop

SECAM –Sequential Color with Memory

SDRAM – Synchronous Dynamic Random Access Memory

SDVO – Serial Digital Video Output

TMDS – Transition-Minimized Differential Signaling

USB – Universal Serial Bus

VCR – Videocassette Recorder

VESA – Video Electronics Standards Association

VGA – Video Graphics Array