Crosstalk Mitigation and Impedance Management Using Tabbed Lines

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Abstract— **As the demand for low-cost electronic systems increases, increasing wiring density/reducing printed circuit board (PCB) layer count becomes inevitable. This reality limits the PCB routing layer options of high-speed input/output (I/O) signals, making it more difficult to meet the next-generation product's performance targets. For example, using densely wired microstrip routing on a PCB helps reduce layer count, but microstrip routing suffers from performance degradation due to increased far-end crosstalk (FEXT). "Tabbed lines" have been proposed to reduce or eliminate FEXT. In this paper we will present an introduction to tabbed lines and their application to crosstalk mitigation and impedance management. Following that, simulation results are presented showing improved memory bus performance on densely routed microstrip channels implemented with tabbed lines.**

Keywords—tabbed line; microstrip; printed circuit board; crosstalk

I.   INTRODUCTION

As the speed of computers continues to increase, one of the bottlenecks that hinders this trend is the data transfer rate of the signal channel between CPU and memory chips. For the widely used double data rate (DDR) memory bus, which is a single-ended, parallel signal bus, far-end crosstalk (FEXT) is often the limiting factor for achieving higher data transfer rate. Therefore, crosstalk mitigation is critical to improve DDR channel performance and hence the speed of computer systems.

The adverse impact of FEXT on high-speed signaling, its expected worsening with higher data rates, as well as a variety of proposed mitigation approaches are described in [1]. The most common approach used to minimize the impact of crosstalk is through avoidance, i.e., at the expense of wiring density, e.g., by increasing the separation between traces or by increasing the separation of vias and/or adding ground vias. Newer approaches that preserve or even increase wiring density, like stub-alternated ("tabbed") lines, have also been proposed [2]. In this work we examine the impact of tabbed lines on DDR channel performance.

As seen in Figure 1, tabbed microstrip wiring consists of short trapezoidal shaped tabs added to the edges of the wire, orthogonal to the direction of propagation. (As shown in this illustration, tabs are placed on both sides of the wires interior to a bus. Bus boundary wires may or may not have tabs on both sides of the wires depending on the adjacent bus or clearance requirements.) These tabs effectively increase the mutual capacitance between the lines without significantly increasing the mutual inductance, and accordingly allow the designer to mitigate FEXT ([2]-[5]). The final difference

between the mode velocities, together with the length of the tabbed line section, determine the magnitude and polarity of the FEXT signal observed at the end of the line.

There are several design variables associated with tabbed lines, e.g., line spacing, tab dimensions, number of tabs per unit length, and the separation of the tabs from each other and the adjacent line. The allowed range for these design variables is limited primarily by PCB manufacturing capability, which typically can provide a usefully large range of final FEXT values and wiring densities. Note that, in most practical cases, the trace width is also reduced from its normal value when tabs are added in order to maintain the target impedance of the line. This latter effect can be applied to advantage in impedance management of breakout wiring.

While tabbed lines can be used to simply compensate for FEXT that would otherwise be generated in a section of simple microstrip wiring, it can also be designed to compensate for crosstalk generated in other sections of the channel [5]. Effective use of the method, particularly for the latter case, requires careful channel analysis starting with a realistic assessment of the relative importance of crosstalk to the particular channel's margins. For example, tabbed line wiring may not be appropriate for channels operating at slower transfer rates or when the wiring lengths are short.
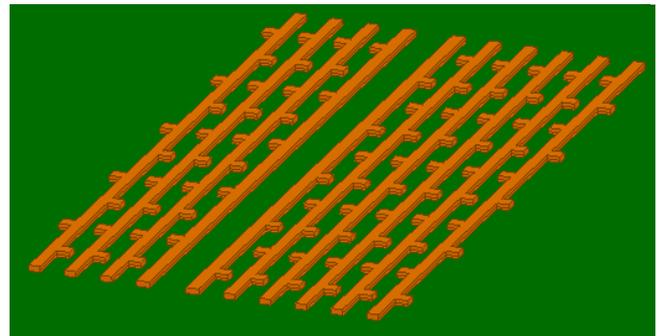

Figure 1: Tabbed lines

For simplicity, the discussion below is based on a differential pair and illustrates why tabbed lines can mitigate FEXT. However, it still provides a good guideline for a general multi-conductor microstrip transmission line system since the major FEXT contribution is from the aggressor lines immediately next to the victim line.

For a differential pair, as a result of the difference between even and odd mode propagation delays, the FEXT

pulse amplitude, $V_f(t)$, on a victim line can be described with the following formula[2]:

$$V_f(t) = \frac{t_f}{2}\left(\frac{C_m}{C_s} - \frac{L_m}{L_s}\right)\frac{dV_i(t-t_f)}{dt} \qquad (1)$$

Here t_f is the time of flight, V_i is the aggressor input voltage, C_m, C_s, L_m and L_s are the mutual capacitance, self-capacitance, mutual inductance, and self-inductance, respectively, per unit length. This equation is valid for times, t, before FEXT saturation occurs. Note that the FEXT amplitude is proportional to the difference between L_m/L_s and C_m/C_s; when the two are equal, FEXT is effectively 0. In such a case even and odd mode propagation delays are equal. The addition of tabs effectively increases C_m / C_s relative to L_m / L_s between circuit traces and thus modulates the crosstalk amplitude.

Microstrip wiring suffers from a disproportion between L_m / L_s and C_m / C_s caused by the inhomogeneous dielectric formed from the boundary between a board's dielectric material and air. This typically results in $C_m / C_s < L_m / L_s$ which, in turn, leads to a crosstalk pulse opposite in sign to that of the rate of change of the aggressor input voltage. Previous work [2-4] demonstrates various wiring methods to equalize the terms, L_m / L_s and C_m / C_s and thus avoid generating FEXT in a microstrip wiring section. One approach [5] focuses on adding enough tabs to increase C_m/C_s sufficiently to allow it to dominate over L_m / L_s, thus *reversing* the polarity of the far-end crosstalk signal. An example of this technique from a test board structure is shown in Figure 2. Here an approximately 0.8inch long segment of strongly coupled tabbed line effectively cancels the far end crosstalk generated along the entire 8 inch long coupled transmission line pair. Figure 3 illustrates the lab measurement results showing the near perfect cancellation of FEXT for this pair of coupled lines.
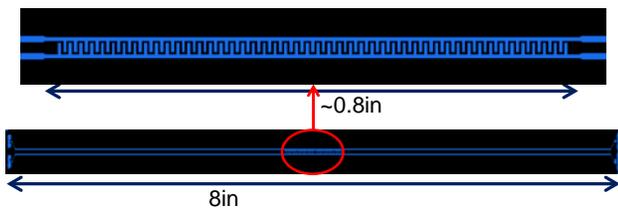

Figure 2: Test board layout for far-end crosstalk amplitude reduction using a short segment of strongly coupled tabbed lines. Note that the crosstalk compensating tabbed section can generally be placed anywhere along the line; here, it is near the center.

II.   TABBED LINE DESIGN METHODOLOGY

As previously mentioned, there are two types of tabbed line design depending on the application. Type (I) is a

segment of tabbed line signal trace that generates zero/minimum FEXT. This type of design is scalable in length, that is, once the design is done, it can be used for any routing length. Its design does not depend on the rest of the channel. Type (II) is a segment of tabbed line trace that minimizes or cancels out some portion of the FEXT of the entire channel by generating FEXT of opposite polarity. The routing length of the tabbed line segment needs to be optimized for the specific channel.
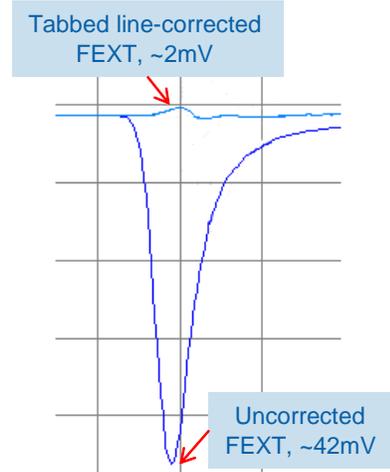

Figure 3: Measurement results showing net FEXT amplitude reduction due to Type (II) tabbed line compensation

The design flow for Type (I) tabbed lines is shown in Figure 4. The entire flow is focused on the segment that will be routed as a tabbed line. It should be noted that equation (1) is based on quasi-static assumption, so the actual performance of the tabbed line over a broad frequency range needs to be validated. Therefore, time-domain simulation is necessary to validate the design and design re-tuning should be done as needed.
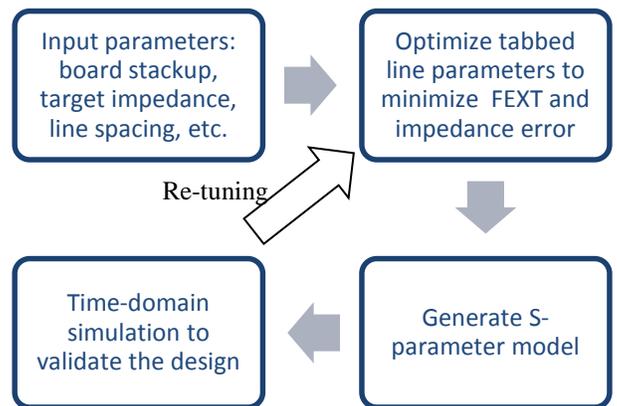

Figure 4: Design flow for minimum FEXT tabbed line

The design flow for Type (II) is described in Figure 5. For this type of design, the FEXT of the entire channel without tabbed lines has to be simulated to provide baseline results. The tabbed lines need to generate the proper amount of FEXT

of opposite polarity to cancel out some or all of the FEXT generated by the entire channel. The FEXT amplitude of opposite polarity also depends on the length of the tabbed line, which can be optimized to match the baseline FEXT. Length optimization is usually preferred over re-tuning the tabbed line design because the former is easier to do. However, sometimes re-tuning the tabbed line design is still necessary for matching impedance to the rest part of the channel.
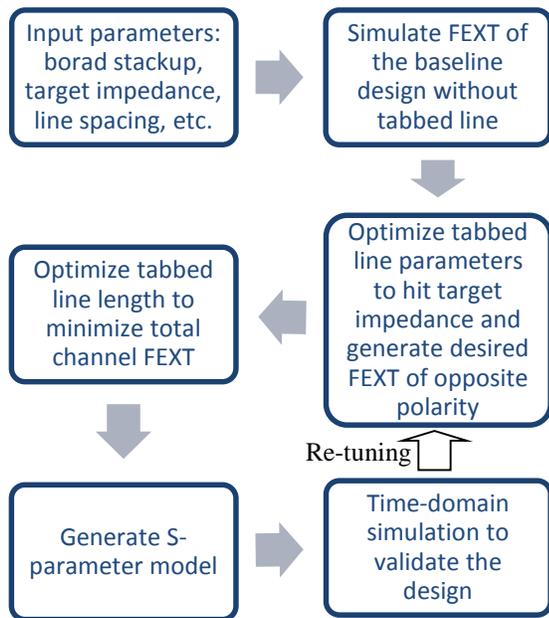
Input parameters: borad stackup, target impedance, line spacing, etc. → Simulate FEXT of the baseline design without tabbed line → Optimize tabbed line parameters to hit target impedance and generate desired FEXT of opposite polarity

Re-tuning

Optimize tabbed line length to minimize total channel FEXT ← Optimize tabbed line parameters to hit target impedance and generate desired FEXT of opposite polarity

Generate S-parameter model → Time-domain simulation to validate the design

Figure 5: Design flow for tabbed line that minimizes channel FEXT.

III. IMPEDANCE MANAGEMENT USING TABBED LINES

Since the addition of tabs to a signal will effectively lower the line's impedance, tabbed lines can be used to lower the impedance of wiring that is already forced to be compressed and therefore has narrow trace width. Narrow lines of this sort can typically be found in the escape and breakout wiring sections of a PCB. Additionally, these narrow wires are not typically called out for impedance control by the PCB vendor due to their narrow width. The impedance of these narrow lines is typically over 50 ohms, and thus such wiring sections present a serious impedance mismatch to the remainder of the channel's impedance, which is typically 40 ohms for DDR. These sections of dense wiring also suffer from high crosstalk.

The addition of tabs to these lines can typically be made without adjusting the wiring pitch, i.e., they are simply

attached to the existing wiring. With the addition of tabs, two benefits are accrued: 1) the impedance of the line can be moved lower, often to 40 ohms and 2) the crosstalk originating in this section can be substantially reduced from its original value.

An example of tabbed routing used in the pinfield to lower the impedance is illustrated below in Figure 6.
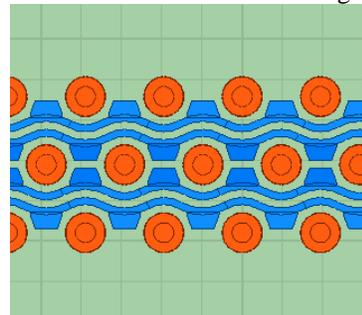

Figure 6: Tabbed line application to 2-track breakout wiring in the pinfield.

From the channel analysis and PCB fabricator's standpoints, it is important to recognize that these wires retain their designation as *uncontrolled* impedances. By adding tabs, the user is moving the impedance of these wires to a generally lower center point and expects and has taken into account normal manufacturing variation around this point.

IV. DDR BUS SIMULATION RESULTS

The signal channel of a typical memory interface is illustrated in Figure 7. The channel starts from the CPU package, followed by several segments of microstrip traces on the mother board including breakout, main routing, and DIMM (dual in-line memory module) field routing, which are modeled as non-ideal multi-conductor transmission lines, followed by the DIMM connectors and the DIMM card. For transmission line segments, 10-line models are used to take into account crosstalk within the byte lane and from the adjacent byte lane as well.

In the results below, two cases are compared: Case I is the regular microstrip routing and Case II is identical to Case I except that the open-field routing uses tabbed lines. To demonstrate the crosstalk reduction effect from tabbed lines, we first look at the time-domain FEXT voltage waveforms as shown in Figure 8. The waveform is measured on the victim line at the receiving end while the excitation, which is a unit step function with finite slew rate, is at transmitting end of the aggressor line next to the victim.[1] Approximately 38 mV reduction in p-p crosstalk voltage for the tabbed line wiring (yellow) is achieved compared to the normal microstrip wiring (blue).

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[1] The excitation and observation locations in the actual simulation are switched by utilizing the reciprocal principle.
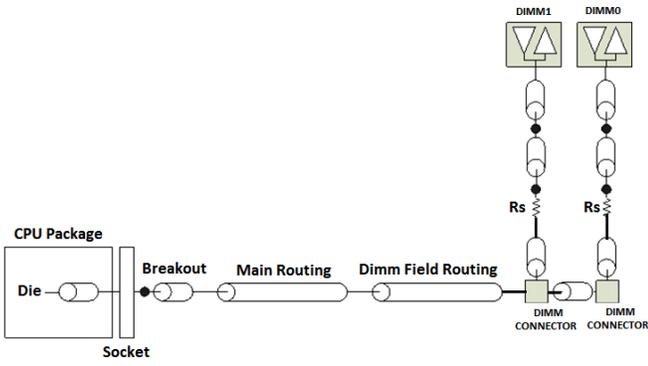
Figure 7: DDR channel model topology used in this study. Channel performance was compared for cases of the "Main Routing" microstrip constructed with and without tabbed lines.
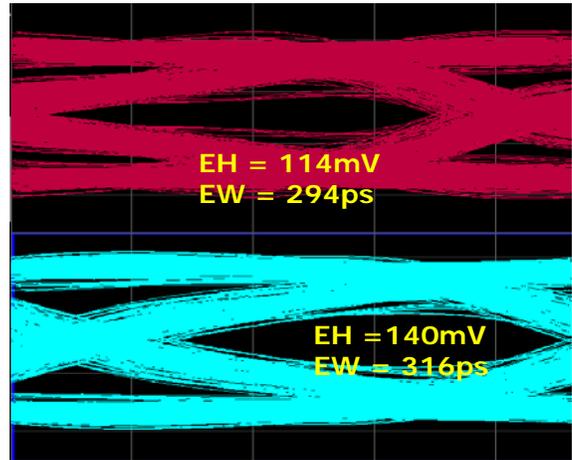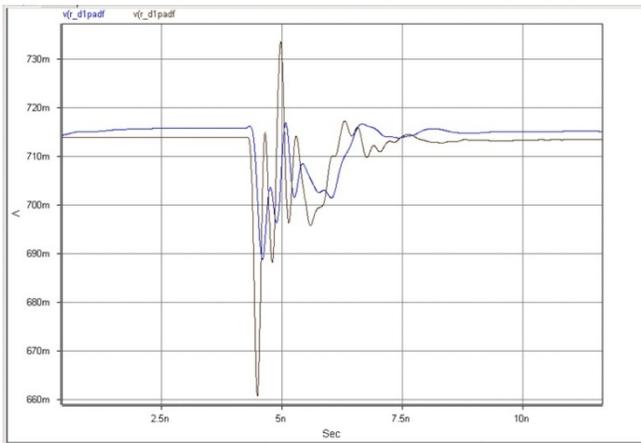

Figure 8: FEXT voltage waveforms at the receiving end. Blue: tabbed line wiring; Yellow: normal microstrip wiring.

Next we compare the eye diagrams of the channel for the two cases. The eye diagrams in Figure 8 are obtained with fixed channel parameters, i.e., assuming all channel parameters, such as trace width, length, dielectric thickness in board stack-up, etc., take fixed values and there is zero manufacture/design variation. By using tabbed line, the eye height (EH) is improved from 114 mV to 140 mV and the eye width (EW) from 294ps to 316ps. This data clearly demonstrates the improvement in overall channel performance just by replacing the open field normal microstrip routing with tabbed line routing.

Finally, we use one-million-case Monte Carlo simulation to take into account the manufacture/design variations for channel parameters and obtain the distribution of channel eye height and width. As shown in Figure 9, again we see obvious improvement by usig tabbed line. For eye height, the mean value is improved from 35 to 66 mV and standard deviation from 8.8 to 6.7 mV. For eye width, the mean value is improved from 63ps to 86ps and standard deviation from 18ps to 11ps.

Figure 9: Eye diagram comparison. Red: normal microstrip wiring. Blue: tabbed line wiring.
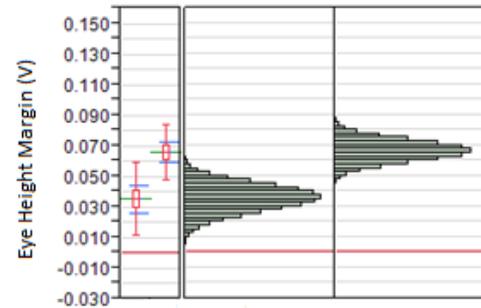
(a)
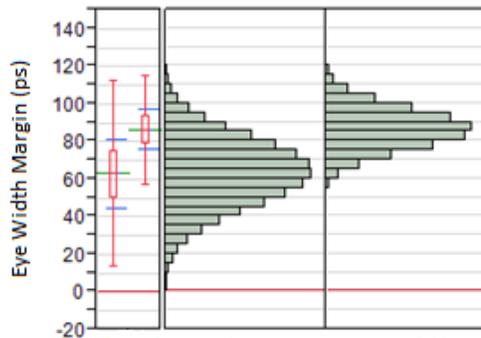
(b)

Figure 10: Eye height (a) and eye width (b) distributions. For both (a) and (b), the left-hand side is for normal microstrip routing and the right-hand side is for tabbed line routing.

V. VALIDATION

To determine if a tabbed routing design meets the impedance and crosstalk objectives, or if some design tuning is required, straightforward experimental methods can be applied to the testing of tabbed line routing sections. Test coupons consisting of a single tabbed wire can be used to assess impedance using a TDR, this can be done by the PCB vendor, but note the vendor should be advised that this does

not imply that the user is attempting a formal change of, for example, narrow breakout wiring to impedance controlled. Test results will be used by the customer to adjust the tabbed line impedance management structures.

Similarly, again by working closely with the PCB vendor, for *controlled* impedance wiring sections, the user may build test coupons consisting of a pair of wires dimensionally identical to those planned for the board. The test coupon architecture will typically have a total of four ports—two ports connected to each of the two ends of the pair of wires. FEXT and impedance can then be determined in the usual way using either a VNA or TDR. Based on the test results and manufacturing fabrication analysis, the user can then make what are typically minimal adjustments to the original design to better meet the design objectives.

VI. SUMMARY

As demonstrated by both simulation and measurement results, tabbed lines can effectively reduce FEXT generated from microstrip routing and the entire signal channel as well. FEXT of closely spaced microstrip wiring can be mitigated by using tabbed lines. Impedance management of otherwise high impedance lines can also be achieved through the use of tabbed lines.

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