

Comprehensive Intel Nehalem Processor

Training

Let MindShare Bring Intel® Nehalem Processors to Life for You

Nehalem processors were recently added to Intel's IA32 CPU family. Building on the previous generation Core 2 architecture, Nehalem brings both major and minor enhancements related to system scalability, hardware integration, main memory access, and power/thermal management.

The primary focus of this course is on Nehalem CPU hardware: processor cores, *Uncore* logic, with an overview of external interfaces and common platform topologies. The course also introduces CPU operational modes, the IA32/64 instruction set, performance monitoring, processor virtualization, etc.--mainly in the context of Nehalem CPU hardware required to support them. Note that other courses in MindShare's IA32/IA64 series offer comprehensive coverage of the software architecture, platform chipsets, QPI, PCI Express, DRAM, virtualization, etc.

The Nehalem Architecture course follows a top-down approach. Key concepts and functional relationships are emphasized, accompanied by specifics of the Nehalem implementation.

You Will Learn:

- Nehalem's place in Intel's IA32/64 CPU family
- Nehalem CPU and platform variants: mobile, desktop, workstation, server
- Architecture of the processor cores (number of cores varies with CPU model)
- Architecture of the new integrated processor uncore logic (shared by all cores)
- Nehalem's extensive power and thermal management features
- CPU reset and initialization
- Error handling
- Performance monitoring
- Processor virtualization support
- External CPU interface basics
- Interrupt handling

Course Length: 3 Days

Course Outline:

- **Part One: Intel IA32 CPU and Platform Background**
 - Nehalem processors and IA32 lineage
 - Intel platform background (pre-Nehalem)
- **Part Two: Nehalem Platform Overview**
 - CPU elements
 - Platform examples
- **Part Three: Processor Core Internal Architecture**
 - Overview of core functional blocks
 - Core fetch/decode/execute engine
 - Implications of HyperThreading
 - Processor operational mode overview
 - Register set
 - Address generation: segmentation and paging
 - IA32e 64-bit extensions
 - Nehalem Caches
- **Part Four: CPU Initialization**
 - Clocks and power supply
 - Reset types
 - Power on configuration (POC)
 - Generic boot up events

- Microcode update
- **Part Five: CPU Management Topics**
 - Power management
 - Thermal management
 - System management mode (SMM)
 - Error handling and machine check architecture (MCA)
- **Part Six: Interrupt Handling**
 - Background
 - Local APICs and IOAPIC
 - Delivery
 - Core interrupt servicing
- **Part Seven: External CPU Interfaces**
 - QuickPath Interconnect (QPI)
 - Integrated memory controller (IMC) and DRAM channels
 - Platform Environmental Control Interface (PECI)
- **Part Eight: Other Processor Features**
 - Processor virtualization support
 - Performance monitoring support
- Appendices:
 - A. Nehalem and Core 2 architectural differences
 - B. Core 2 FSB transaction review

Recommended Prerequisites:

Basic understanding of computer architecture.

Course Material:

MindShare's **x86 Instruction Set Architecture** Book or eBook.

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Publisher: MindShare Press

Students will be provided with an electronic version of the slides used in class.