M.2 – SSIC℠
Electrical Test Specification
Version 1.0, Revision 0.5

August 27, 2013
Revision History

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<th>Revision History</th>
<th>Date</th>
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1. Introduction

This document provides test descriptions for M.2 – SSIC electrical testing. It is relevant for anyone building SSIC modules or systems based on PCI Express M.2 specification.

1.1. Coverage

This document covers items in the Inter-Chip Supplement to the USB Revision 3.0 Specification, Revision 1.01. Tests for HS-GEAR1, HS-GEAR2 and PWM-GEAR1 are included in this specification. Other gears may be covered in future revisions.
2. Test Fixtures

Separate test fixtures needs to be made for system testing and module testing. Each test fixture contains at least one Tx channel and one Rx channel. Since high speed Tx signaling is tested with differential termination and low speed Tx signaling is tested without termination, three test channels are described: High Speed Tx test channel, Low Speed Tx test channel and Rx test channel.

All Tx traces need to be matched lengths and all Rx signal traces need to be matched length but Tx and Rx channel lengths do not need to be matched. Lengths should be as short as possible (approximately 25.4 mm or 1.0 in).

![Figure 1: Proposed System Test Fixture Setup](image1)

![Figure 2: Proposed Module Test Fixture Setup](image2)

The oscilloscope used to capture Tx waveforms must have a sufficiently high sample rate to accurately measure transition times and the minimum expected period of the transmitter output.

2.1. System High Speed Tx Test Channel

The system High Speed Tx test channel includes Tx differential signals with 100Ω differential termination that are broken out to probe pads or probe connectors. Active, high impedance, high bandwidth (minimum 8GHz) differential probes are used to capture data for each high speed Tx test channel.
2.2. **System Low Speed Tx Test Channel**

The Low Speed Tx test channel includes Tx differential signals without termination that are broken out to probe pads or probe connectors. High impedance, medium bandwidth (minimum 100MHz) probes are used to capture data for the low speed Tx test channel.

2.3. **System Rx Test Channel**

The Rx test channel includes differential signals broken out to semi-detent SMP connectors. For compliance testing, an additional ISI channel will be connected between the signal source (test instrument) and the Rx test channel SMP connectors.

2.4. **Module High Speed Tx Test Channel**

The module High Speed Tx test channel includes Tx differential signals with 100Ω differential termination that are broken out to probe pads or probe connectors. Active, high impedance, high bandwidth (minimum 8GHz) differential probes are used to capture data for each high speed Tx test channel.

2.5. **Module Low Speed Tx Test Channel**

The Low Speed Tx test channel includes Tx differential signals without termination that are broken out to probe pads or probe connectors. High impedance, medium bandwidth (minimum 100MHz) probes are used to capture data for the low speed Tx test channel.

2.6. **Module Rx Test Channel**

The Rx test channel includes differential signals broken out to semi-detent SMP connectors. For compliance testing, an additional ISI channel (with insertion loss of approximately 6.0dB at 1.455 GHz) will be connected between the signal source (test instrument) and the Rx test channel SMP connectors.

3. **Test Descriptions**

The tests listed below are required to verify the correct electrical operation of M.2 - SSIC high speed and PWM systems and modules.

3.1. **M.2 - SSIC Transmitter High Speed Electrical Compliance Test**

The high speed electrical tests are performed by causing the M.2 - SSIC transmitter to send a continuous CRPAT compliance test pattern.
The output of the transmitter is captured by a high speed real-time oscilloscope at a sufficiently high sample rate as shown in Table 1: Minimum Waveform Acquisition Rates for High Speed and PWM Gears. Once captured, the acquired waveform is analyzed for eye height and eye width using the SigTest analysis software.

<table>
<thead>
<tr>
<th>Gear</th>
<th>Data Rate</th>
<th>Unit Interval (ps)</th>
<th>Min. Acquisition Rate (GS/s)</th>
<th>Sample Interval (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HS G1 A</td>
<td>1.248 Gb/s</td>
<td>801.28</td>
<td>40.0</td>
<td>25.0</td>
</tr>
<tr>
<td>HS G1 B</td>
<td>1.4576 Gb/s</td>
<td>686.06</td>
<td>40.0</td>
<td>25.0</td>
</tr>
<tr>
<td>HS G2 A</td>
<td>2.496 Gb/s</td>
<td>400.64</td>
<td>40.0</td>
<td>25.0</td>
</tr>
<tr>
<td>HS G2 B</td>
<td>2.9152 Gb/s</td>
<td>343.03</td>
<td>40.0</td>
<td>25.0</td>
</tr>
<tr>
<td>PWM G1</td>
<td>0.003 Mb/s to 0.009 Mb/s</td>
<td>333.333.33 to 111,111.11</td>
<td>40.0</td>
<td>25.0</td>
</tr>
</tbody>
</table>

Table 1: Minimum Waveform Acquisition Rates for High Speed and PWM Gears

### 3.1.1. M-TX High Speed Compliance Test Steps

This test is run on all Tx lanes that support high speed signaling. The DUT is configured to output the high speed Tx compliance pattern (CRPAT) on the lane being tested. A real-time sampling scope is used to capture the Tx output which is then analyzed by the SigTest application to determine eye height and eye width.

#### Starting Configuration

Test parameters such as which gear is to be tested are transmitted to the DUT using a test programmer that performs PWM signaling on the Lane 0 Rx lines. A comprehensive list of configuration parameters is yet to be determined. Configuration parameters set via Lane 0 Rx affect all Tx lanes. Once the test configuration data has been sent to the device under test the test programmer must terminate the LS burst for the configuration parameters to become active.

#### Overview of Test Steps

The test is performed by following these steps:

1. Connect the Tx lane under test to a high speed oscilloscope.
2. Connect Rx lane zero to the test programmer output.
3. Power on the DUT.
4. Configure the lane under test to Transmit Compliance Mode, Test Mode, HS Gear 1, rate series A.
5. Capture 1 million unit intervals of data (see Table 2: Minimum Acquisition Sample Counts and Acquisition Times for High Speed Gears).
6. Using SigTest with the appropriate template file, the eye height and eye width are found and compared to the following values:
   a. **System TX**
      i. **Eye Height** – 95 mV (±47.5 mV)
ii. Eye Width .55 unit interval (UI) (Maximum Tj ≤ 0.45 UI)

b. Module TX
   i. Eye Height – 130 mV (±65.0 mV)
   ii. Eye Width - .61 UI (Maximum Tj <= 0.39 UI)

7. Repeat steps 4 - 6 for each additional Gear and/or rate series supported by the DUT.

<table>
<thead>
<tr>
<th>HS Gear</th>
<th>Unit Interval (ps)</th>
<th>Min. Acquisition Rate (GS/s)</th>
<th>Min. Number of Samples</th>
<th>Min. Acquisition Time (µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>G1 A</td>
<td>801.28</td>
<td>10.0</td>
<td>8,012,800</td>
<td>801.28</td>
</tr>
<tr>
<td>G1 B</td>
<td>686.06</td>
<td>10.0</td>
<td>6,860,600</td>
<td>686.06</td>
</tr>
<tr>
<td>G2 A</td>
<td>400.64</td>
<td>20.0</td>
<td>8,012,800</td>
<td>400.64</td>
</tr>
<tr>
<td>G2 B</td>
<td>343.03</td>
<td>20.0</td>
<td>6,860,600</td>
<td>343.03</td>
</tr>
<tr>
<td>G3 A</td>
<td>200.32</td>
<td>40.0</td>
<td>8,012,800</td>
<td>200.32</td>
</tr>
<tr>
<td>G3 B</td>
<td>171.51</td>
<td>40.0</td>
<td>6,860,400</td>
<td>171.51</td>
</tr>
</tbody>
</table>

Table 2: Minimum Acquisition Sample Counts and Acquisition Times for High Speed Gears

3.2. M-Phy Transmitter Pulse Width Modulation Electrical Compliance Test

The Pulse Width Modulation (PWM) electrical tests are performed by causing the M.2 system or modules transmitter to send a CRPAT in PWM-G1 mode. Three separate CRPAT bursts should be captured including the transition from SLEEP to PREPARE. A detailed description of the method used to force the DUT to transmit a CRPAT in PWM-G1 mode is yet to be determined. The output of the system or module Tx is captured by a real-time oscilloscope.

Overview of Test Steps

The test is performed by following these steps:

1. Connect the Rx lane to the test mode programmer and connect the Tx lane to a high speed oscilloscope via two high impedance single ended probes or one high impedance differential probe. The scope will compute the differential values.
2. Power on the DUT.
3. Configure the lane under test to PWM-G1, small amplitude.
4. Configure the oscilloscope to trigger on the transition out of SLEEP and capture PREPARE and the subsequent burst.
5. Send a message on the Rx channel to cause the Tx channel to respond with a CRPAT burst.
6. Capture the CRPAT burst and measure $V_{\text{DIFF,AC,TX}}$, $V_{\text{DIFF,DC,TX}}$, $T_{\text{PWM,PREPARE}}$, $T_{\text{PWM,TX}}$, $T_{\text{OL,PWM,TX}}$, $k_{\text{PWM,TX}}$, $T_{\text{PWM,TX}}$, and $T_{\text{F,PWM,TX}}$ using the SigTest analysis program with the appropriate template file.
7. Repeat steps 5 and 6 a minimum of three times and assure that each captured burst passes.

**Analysis Details**

$V_{DIF\_DC\_TX}$ finds the mean voltage level within the SLEEP and PREPARE states of the captured waveform to determine DIF-N and DIF-P respectively. $T_{PWM\_PREPARE}$ finds the duration of DIF-P during the PREPARE state. All other PWM test are performed on the first three PWM bursts following the PREPARE state. The zero crossing point of a falling edge is used as the boundary between bits. A simplified algorithmic description of the remaining tests follows:

$V_{DIF\_AC\_TX}$ shall be tested for every bit within the first three bursts. The delta of the absolute minimum voltage and the absolute maximum voltage determines the AC amplitude of a bit.

$T_{PWM\_TX}$ shall be tested for every bit within the first three bursts. $T_{PWM\_TX}$ is the delta between consecutive zero crossings (falling edge only). A linear interpolation will be used to define the zero crossing location.

$TOL_{PWM\_TX}$ shall be tested for every bit within the first three bursts. The average $T_{PWM\_TX}$ is computed for every burst using the first N bits. $TOL_{PWM\_TX}$ is the ratio of a $T_{PWM\_TX}$ and the average bit duration of the same burst.

$k_{PWM\_TX}$ shall be tested for every bit within the first three bursts. The $k_{PWM\_TX}$ is the ratio of $T_{PWM\_MAJOR\_TX}$ and $T_{PWM\_MINOR\_TX}$ within a single bit. A linear interpolation is used on the rising edge to determine the zero crossing boundaries of the $T_{PWM\_MAJOR\_TX}$ and the $T_{PWM\_MINOR\_TX}$.

$T_{R\_PWM\_TX} / T_{F\_PWM\_TX}$ shall be tested for every bit within the first three bursts. The DIFF-P and DIFF-N computed in $V_{DIF\_DC\_TX}$ are used to set the 100% peak-peak value. This peak-peak value is used to determine the 20/80% voltage levels where symmetry is assumed. $T_{R\_PWM\_TX}$ is computed at every rising edge utilizing a linear interpolation to determine the 20/80% locations. Similarly $T_{F\_PWM\_TX}$ is computed at every falling edge.

### 3.3. M-RX High Speed Receiver Jitter Tolerance Test

This test is run on all Rx lanes. The test verifies that the DUT receiver can function normally with jitter and voltage levels near the specification allowed limits and that it does not exceed the allowed receiver error rate in loopback mode. In analog loopback test mode the DUT retransmits the data it receives on the receiver pins. The DUT uses the recovered clock to re-transmit the data. The transmitted and received bit patterns can then be matched in the signal source used for the test to check if any of the bits were received in error. Each receive lane needs to have an associated loopback partner (transmit lane) for this test.
Figure 3: Analog Loopback setup with BERT and the DUT

Starting Configuration

1. The BERT/signal generator is calibrated to provide the worse case signal to the DUT RX. Various components like the Voltage Swing, Random Jitter and Deterministic Jitter are calibrated independently.

Random jitter and voltage swing are calibrated at the output of the BERT. Deterministic Jitter is calibrated at the end of the reference channel. A real time scope and the postprocessing software (Sigtest) are needed to perform calibration for analog loopback test.

The calibration is performed by following these steps:

a. Vswing calibration:

1. Setup BERT to transmit CRPAT pattern.
2. Set all the jitter values to 0 ps in BERT.
3. Make sure that the Pre-cursor and the Post-Cursor values are set to 0.
4. Set differential amplitude in BERT to about 200mV
5. Set up Common Mode voltage in BERT to 140 mV. TBD: May test additional common mode voltages.
6. Capture 1 Million UI with this pattern on the RT scope. Calibration point is shown in Figure 3: Analog Loopback setup with BERT and the DUT above.
7. Post-process the captured waveform using Sigtest. Use appropriate Sigtest template depending on the Gear and the Rate Series configuration for the lane under test. Look at the eye height reported by Sigtest.
8. Repeat steps 4-6 above by adjusting output amplitude in BERT such that the peak to peak eye height reported by SigTest is 160mV ($V_{\text{DIF AC SA RT TX}}$)

b. RJ calibration:
   1. Setup BERT to transmit CRPAT pattern.
   2. Set all SJ amplitude values to 0 ps.
   3. Set RJ amplitude to 13mUI.
   4. Capture 1 Million UI
   5. Post-process the captured waveform using Sigtest. Use appropriate Sigtest template depending on the Gear and the Rate Series configuration for the lane under test. Look at the RJ reported by Sigtest.
   6. Adjust RJ through the BERT such that 1M UI's captured and post-processed through Sigtest using applicable BPF gives RJ of 0.17 UI$_{\text{SS}}$ (@1E-10)
   7. Note this value of RJ

c. Sinusoidal tone 1 (SJ1) calibration:
   1. Setup BERT to transmit CRPAT pattern.
   2. Connect a reference ISI channel to BERT output
   3. Set BERT SJ1 frequency to $f_{\text{SJ1 RX}}$ MHz. (Refer Table below for exact frequency for the Gear and Rate under consideration)
   4. Set all sinusoidal and random jitter amplitude values to 0 ps in BERT.
   5. Set Vswing to that calibrated in the “Vswing calibration” section above.
   6. Capture 1 Million UI
   7. Post-process using appropriate Sigtest template.
   8. Note the Max p-p jitter reading from the Sigtest results.
   9. Set the SJ1 amplitude in BERT to 75 mUI. Make sure that the SJ1 frequency is $f_{\text{SJ2 RX}}$ MHz.
   11. Note the Max p-p jitter reading from the Sigtest results.
12. Adjust source SJ amplitude in BERT till Max p-p jitter reading from the SigTest results is 0.15 UI_{18}\text{HS} (refer table above for gear and rate series specific values) + (reading from step 8 above).

13. Note the SJ1 amplitude adjusted in Step-12

d. Sinusoidal tone 2 (SJ2) calibration:

1. Setup BERT to transmit CRPAT pattern.
2. Set BERT SJ2 frequency to f_{S2,RX}\text{MHz}.
3. Connect a reference ISI channel to BERT output.
4. Set all jitter source amplitudes to 0ps
5. Set Vswing to that calibrated in the “Vswing calibration” section above
6. Capture 1 Million UI
7. Post-process using Sigtest template with BPF lower and upper cutoff frequencies as per table above. Choose appropriate value depending on the HS-Gear and data rate series.
8. Note the Max p-p jitter reading from the Sigtest results.
9. Set SJ2 amplitude to 100 mUI
10. Capture 1 Million UI's
11. Post-process using Sigtest template using BPF with applicable lower and upper cutoff frequencies.
12. Adjust source SJ2 amplitude till Max p-p jitter reading from Sigtest is 0.2 UI_{18}\text{HS} + (reading from step 8) in Sigtest max p-p jitter field.
13. Note the SJ2 amplitude adjusted in Step-12

e. Eye Width calibration:

1. Setup BERT to transmit CRPAT pattern.
2. Setup BERT Vswing to that calibrated in Vswing Calibration section above
3. Setup BERT RJ to that calibrated in RJ Calibration section above
4. Setup BERT SJ1 amplitude to that calibrated in Sinusoidal tone 1 (SJ1) calibration section above. Make sure that SJ1 frequency is f_{S1,RX}\text{MHz}
5. Setup BERT SJ2 amplitude to that calibrated in Sinusoidal tone 2 (SJ2) calibration section above. Make sure that SJ1 frequency is f_{S1,RX}\text{MHz}.
6. Connect a reference ISI channel to BERT output.
7. Connect the other end of the ISI channel to the scope.
8. Capture 1 Million UI
9. Post-process the captured waveform using Sigtest. Use appropriate Sigtest template depending on the Gear and the Rate Series configuration for the lane under test. Look at the Eye Width reported by Sigtest.

10. Adjust RJ amplitude dialed into BERT till Eye Width reported by Sigtest is $E_{RX} = 0.2$ UIHS.

**f. Eye Height calibration:**

If the Eye Height reported by Sigtest in Section e above is not 40mV ($V_{DF\_ACC\_RX}$), then adjust Voltage Swing dialed into the BERT till Sigtest reports 40mV for Eye Height.

**g. Loopback Test:**

1. Using an external configuration device (test programmer) connected to the RX lane-0 and TX lane-0, the DUT is first configured to Gear 1 and Rate Series A.

2. Test programmer configures the DUT into Test Mode by doing the configuration write to the appropriate register.

3. Test programmer configures the lane under test into analog loopback mode by writing the appropriate register.

4. The test programmer reads back the register to know the loopback partner for the lane under test.

5. Test programmer terminates the LS burst.

6. DUT detects end of configuration and enters into analog loopback mode for the lane under test.

7. The test programmer is removed from RX Lane-0 and a programmable signal source such as a Bit Error Rate Tester (BERT) is connected to it via a pair of phase matched cables with appropriate adapters where required. The BERT error detector is connected to the TX lane-0.

8. Adjust the Voltage Swing dialed into the BERT to that calibrated in Eye Height section above.

9. Adjust the RJ to that calibrated in Eye Width section above.

10. Remove the test programmer from the TX and RX lane-0 and connect BERT there.

11. Setup BERT to transmit CRPAT

12. Run the loopback test bit comparisons for $3 \times 10^{10}$ bits (Confidence Level=95%)

13. There should be 0 or 1 bit error during this time.

14. Repeat steps 2 - 13 for each additional Gear and/or rate series supported by the DUT.
### Reference Table for Jitter and Frequency values for various Gears and Data rates

<table>
<thead>
<tr>
<th>HS Gear</th>
<th>Rate Series</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate (DR_{HS}) (Gbps)</td>
<td></td>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>UI_{HS} (=1/DR_{HS}) (ps)</td>
<td>801.28</td>
<td>686.34</td>
<td>400.64</td>
</tr>
<tr>
<td>f_{HS} (=DR/2) (MHz)</td>
<td>624</td>
<td>728.5</td>
<td>1248</td>
</tr>
<tr>
<td>f_{HS,MAX} (=3DR/4) (MHz)</td>
<td>936</td>
<td>1092.75</td>
<td>1872</td>
</tr>
<tr>
<td>f_{HS,MIN} (=DR/10) (MHz)</td>
<td>124.8</td>
<td>145.7</td>
<td>249.6</td>
</tr>
<tr>
<td>f_{C,HS,GX,TX} (MHz)</td>
<td>2</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>f_{STJ,TX} (=1/(30*UI_{HS})) (MHz)</td>
<td>41.60</td>
<td>48.57</td>
<td>83.20</td>
</tr>
<tr>
<td>f_{U,RX} (=1/(2*UI_{HS})) (MHz)</td>
<td>624</td>
<td>728.5</td>
<td>1248</td>
</tr>
<tr>
<td>SJ_{RX} (=0.15UI_{HS}) (ps)</td>
<td>120.19</td>
<td>102.95</td>
<td>60.10</td>
</tr>
<tr>
<td>f_{SJ0,RX} (MHz)</td>
<td>0.2</td>
<td>0.2</td>
<td>0.4</td>
</tr>
<tr>
<td>f_{SJ2,RX} (MHz)</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>f_{SJ3,RX} (=f_{SYSTEM}) (MHz)</td>
<td>Implementation Dependent</td>
<td>Implementation Dependent</td>
<td>Implementation Dependent</td>
</tr>
<tr>
<td>f_{SJ4,RX} (=1/(30*UI_{HS}))</td>
<td>41.60</td>
<td>48.57</td>
<td>83.20</td>
</tr>
<tr>
<td>STD_{J,RX} (=0.2UI_{HS}) (ps)</td>
<td>160.26</td>
<td>137.27</td>
<td>80.13</td>
</tr>
<tr>
<td>TJ_{RX} (=0.52UI_{HS}) (ps)</td>
<td>416.67</td>
<td>356.90</td>
<td>208.33</td>
</tr>
<tr>
<td>STTJ_{RX} (=0.3UI_{HS}) (ps)</td>
<td>240.38</td>
<td>205.90</td>
<td>120.19</td>
</tr>
<tr>
<td>RJ_{RX} (=0.17 UI_{HS}) (ps)</td>
<td>136.22</td>
<td>116.68</td>
<td>68.11</td>
</tr>
</tbody>
</table>

---

**Figure 4**: RX calibration parameters for HS-G1 and HS-G2

#### 3.3.1. **RX_BURST_COUNT Test**

1. Repeat same calibration as analog test.
2. Using an external configuration device (test programmer) connected to the RX lane-0 and TX lane-0, the DUT is first configured to Gear 1, Rate A and minimum T_{ACTIVATE}.
3. Test programmer configures the DUT into HS mode.
4. Test programmer configures the DUT into Test Mode by doing the configuration write to the appropriate register.
5. Test programmer configures the lane under test into M-PHY Burst Count Mode by making write to the appropriate register.
6. BERT sends a pattern comprising of DIF_P, 1 MK0, 64 SKIP symbols (01010101 808080...), followed by DIF-N for 15UI$_{HS}$ + configured T$_{ACTIVATE}$. BERT sends this pattern 1000,000 times.
   a. Repeat with CRPAT instead of the 64 SKIP symbols
   b. Test min time between bursts (9UI$_{HS}$ + configured T$_{ACTIVATE}$)
   c. Alternate CRPAT and Clock pattern
7. RX_BURST_COUNT register is read using the test programmer to check the bursts counted by the DUT.
8. Repeat steps 2 - 7 for each additional Gear and/or rate series supported by the DUT.

### 3.3.2. RX_ERR_COUNT Test
1. Rewrite to just redo Burst count test with probability .01 of MK0 bits getting corrupted and checking valid burst and error counts accordingly.
2. Using an external configuration device (test programmer) connected to the RX lane-0 and TX lane-0, the DUT is first configured to Gear 1, Rate A and minimum T$_{ACTIVATE}$.
3. Test programmer configures the DUT into HS mode.
4. Test programmer configures the DUT into Test Mode by doing the configuration write to the appropriate register.
5. Test programmer configures the lane under test into M-PHY Burst Count Mode by making write to the appropriate register.
6. BERT sends a pattern comprising of DIF_P, Burst Mode CRPAT modified to remove the MK0. BERT sends this pattern 100 times.
7. Repeat steps 2 - 6 for each additional Gear and/or rate series supported by the DUT.

### 3.4. M-Rx Pulse Width Modulation Electrical Compliance Test
This test set verifies the DUT’s receiver can function normally in PWM mode (no received errors) while Rx signal parameters are stressed. The programmable signal source will be used to send the DUT an electrically stressed RRAP request and verify the correct RRAP response is received.

**Overview of Test Steps**

The test is performed by following these steps:
1. Connect Rx Lane0 and Tx Lane0 to the programmable signal.
2. Configure the programmable signal source to stress one of the parameters (listed in Step 7) while sending a RRAP request via the DUTs Rx Lane0.
3. Configure the DUT to receive RRAP requests in PWM-G1 Terminated mode and respond to the requests with a PWM-G1 RRAP response.

4. Connect the programmable signal source to the DUT and transmit a minimum of 1e3 RRAP requests.

5. Record any errors in the received RRAP responses.

6. A lack of errors indicates a passing test for the stressed parameter used.

7. Repeat steps 2-6 while stressing each of the following parameters: \( V_{\text{DIFF}_R} \) (min 60 mV), \( V_{\text{DIFF}_R} \) (max 245 mV), \( T_{\text{PWM}_T} \) (min 1/9 µs), \( T_{\text{PWM}_T} \) (max 1/3 µs), \( T_{\text{OL}_P\text{PWM}_R} \) (min 0.82), \( T_{\text{OL}_P\text{PWM}_R} \) (max 1.18), \( k_{\text{PWM}_R} \) (min 0.6/0.4), and \( k_{\text{PWM}_R} \) (max 0.75/0.25).