Intel® IXP400 Software Version 2.1

Software Product Specification

November 2005

Order Number: 310288, Revision: 001
November 2005

Revision History

Date	Revision	Description
November 2005	001	Initial release.

1.0 Product Context

Intel® IXP400 Software v2.1 enables the underlying capabilities of the Intel® IXP4XX Product Line of Network Processors.

Table 1. Intel® IXP400 Software v2.1 Compatibility Reference

Support Category	Details
Processors supported	• Intel® IXP42X Product Line of Network Processors • Intel® IXP45X and Intel® IXP46X Product Line of Network Processors
Operating system/ development environments	• MontaVista* Linux* Professional Edition 3.1 with Gcc compiler • Wind River* VxWorks* Developer Tool Kit 2.2.1 (Tornado* 2.2.1 / VxWorks 5.5.1) - Gcc compiler with BSP version 1.2/10 [IXDP425 BSP version 1.2/12, IXDP465 BSP version 1.2/1] - Diab* compiler v5.2.1 [IXDP425 BSP version 1.2/12, IXDP465 BSP version 1.2/1]
Hardware platform support	• Intel® IXDP425 Development Platform • Intel® IXDP465 Development Platform

2.0 Product Specifications

This section presents features supported by Intel® IXP400 Software v2.1.

Basic Features

- Processor-specific build mechanism
- Read and/or disable Intel® IXP4XX product line processors capabilities
- Configurable enabling and disabling of software features
- Facility to download Intel® microcode images to NPEs
  - — NPE A image options
    - * Ethernet, HSS, ATM, DMA,
  - — NPE B image options
    - * Ethernet, DMA
  - — NPE C image options
    - * Ethernet, DMA, Crypto

ATM Access

- AAL (AAL5, AAL0, OAM)
- Configure and activate up to 12 ports on the UTOPIA level-2 interface
- Up to 32 VC channels supported
- ATM configuration and management component

ATM Transmit Scheduler (Tx)

- Maximum number of VCs: Up to 32 on device at any time

- Traffic types
  - Number of traffic types: 4
  - Traffic prioritization in normal operation: CBR > rt-VBR = nrt-VBR > UBR
  - Additional QoS support on oversubscription; traffic prioritization changed to: CBR > rt-VBR > nrt-VBR > UBR
  - CDVT not supported
- Applicable conditions
  - PCR for all types
  - SCR and MBS for rt-VBR and nrt-VBR
- Virtual Channel setup
  - Up to 12 ports and 32 VCs across all 12 ports of any supported traffic type (i.e., CBR, rt-VBR, nrt-VBR or UBR)

Security

- Silicon Crypto algorithms enabled for use via software:
  - DES (64-bit block, 64-bit key)
  - 3DES (64-bit block, 192-bit key)
  - AES (128-bit block, 128/192/256-bit key)
  - ARC-4 (8-bit block, 128-bit key)
- Encryption modes of operation:
  - ECB
  - CBC
  - CTR (For AES only)
  - AES-CCM
- Silicon Crypto Authentication algorithms enabled for use via software:
  - SHA1 and MD5 hashing
  - HMAC-SHA1 (512-bit block size, from 20- to 64-byte key sizes)
  - HMAC-MD5 (512-bit block size, from 16- to 64-byte key sizes)
  - WEP ICV (32-bit CRC polynomial)
- Silicon Public Key Exchange (PKE) crypto engine enabled via Intel XScale core software [IXP45X/IXP46X product line only]:
  - Pseudo Random Number generator
  - Exponent/Modulo Arithmetic Unit
  - SHA1 hashing (supports PKE)

DMA

- DMA capabilities to offload data transfers between peripherals and processor memory
- Transfer-mode support
  - Copy only, Copy and Clear Source, Copy and Byte Swap, Copy and Byte Reverse
- Source and Destination Transfer Widths
  - Burst, 8-bit, 16-bit, 32-bit

Ethernet Access

- Enabled additional MII via NPE-A [IXP45X/IXP46X product line only]
  - — Total MIIs enabled: 3; SMII mode is not validated

  Note: NPE-A does not support simultaneous use of Eth and HSS features.
- APIs provisioning for data, control, and management support of Ethernet MAC devices
- Ethernet MIB statistics, tracking and reporting
  - — RFC1213 (SNMP) and RFC1757 (RMON)
- IEEE 802.1d-compliant bridge
- Jumbo frame support — up to 16,320 bytes
- IPv4/IPv6 frame indication
- NPE-assisted Source MAC address-learning
  - — Each NPE can manage up to 511 MAC addresses

  Ethernet Receive Path Services

  - — Filtering Services
    - * Frame size filtering services
    - * Ethernet filtering database services
    - * Destination MAC address filtering
  - — Destination port identification
  - — Spanning tree services
    - – Spanning tree BPDU identification and delivery
    - – Spanning tree port blocking
  - — Learning and Aging Services (NPE-assisted)
    - – Source MAC address learning assistance
    - – MAC address aging assistance
  - — Categorization of IPv4/IPv6 ingress packet (NPE-assisted)
  - — VLAN ingress services (NPE-assisted)
    - – Acceptable frame type filtering
    - – ID copy
    - – VLAN tagging/untagging
    - – VLAN tagging/untagging extended to support 802.11 frames (Wi-Fi)
    - – Filtering
    - – Port ID extraction
  - — Firewall services
    - – Invalid source MAC address filtering
    - – MAC address/mask blocking
    - – MAC address/mask admission
  - — (NPE-assisted) IEEE802.3 to IEEE802.11 header conversion
    - – User-configurable IEEE802.3 to IEEE802.11 conversion
    - – Support for 40 BSSID entries
    - – Support for 40 Access Point MAC entries
    - – Support for inserting Pad byte
    - – Logical destination port ID support

- — Miscellaneous frame inspection/extraction services
  - – Destination and source MAC address copy
  - – Frame header type report
- — Receive QoS services
  - – Receive QoS configuration
  - – Receive QoS classification and delivery

Ethernet Transmit Path Services

- — Transmit QoS service
  - * Priority-based
- — Frame size filtering services
- — IEEE802.11 to IEEE802.3 header conversion
  - * Support for removing Pad byte
- — VLAN egress services
  - * VLAN egress filtering
  - * VLAN egress ID-based tagging/untagging
  - * Support for Wi-Fi header conversion
  - * VLAN tagging/untagging extended to support 802.11 frames (Wi-Fi)

Ethernet PHY

- Provides access to a minimum number of necessary configuration registers on external Ethernet PHYs
- MDIO bus scanning for up to 32 available PHYs
- Configure PHY link speed, half/full duplex, and auto-negotiation settings
- Retrieve PHY status and link state
- Supported PHYs
  - — Intel® LXT971 Fast Ethernet Transceiver
  - — Intel® LXT972 Fast Ethernet Transceiver
  - — Intel® LXT973 Fast Ethernet Transceiver
  - — Micrel Semiconductor* / Kendin* KS8995 5-port 10/100 switch with PHY
  - — Realtek* RTL8305SB 5-port 10/100 switch with PHY

  Note: Other PHYs may be supported (user-upgradeable).

HSS-Access Layer

Note: NPE-A does not support simultaneous use of Eth and HSS features.

- Provides API for T1/E1 and high-speed serial services
- NPE-assisted timeslot switching (HSS Bypass)
  - — Voice-switched within NPE and bypasses Intel XScale core
  - — Bypass mode can be enabled on the fly
  - — “Gain control" lookup table for each bypass channel
  - — Provide a maximum of two pairs of bypassed channels on port 0 at any one time
- Timeslot provisioning
  - — Static timeslot provisioning

  - — Limit of one multi-timeslot packetized channel per T1/E1
- Channel Processing
  - — Bit inversion on a per-channel basis
  - — Packetized N x 64Kbps channels from any TDM stream [where 1 <= N <= 32]; a channel may not span multiple T1/E1s
  - — Packetized (N x 56Kbps with CAS bit) channels from any TDM stream [where 1 <= N <= 32]; a channel may not span multiple T1/E1s
  - — Channelized Service (64 Kbps only)
- Channel Data Processing Services
  - — Transparent (Raw) service for packetized channels without frame alignment
- Basic T1/E1
  - — One packetized N x 64 Kbps or N x 56 Kbps channel per T1/E1, for up to eight T1/E1s; four channels per HSS port
  - — Sixty-four non-packetized 64-Kbps channels, 32 channels per HSS port

Performance Profiling [IXP42X product line only]

- Performance statistics from the Intel XScale core PMU, Internal bus PMU, and XCycle
- Clock Counting
- Event Counting
- Time-based sampling
- Event-based sampling
- Output-to-a-file support

UART Access

- Baud rates between 9,600 and 912.6 Kbps
- 16550 UART support
- Independent UART configuration support

USB 1.1 Device Access

- Sixteen endpoints
- Half-duplex at a 12-Mbps baud rate, slave only

Additional Interfaces Support

- Inter-Integrated Circuit (I^2C) Access support [IXP45X/IXP46X product line only]
- Synchronous Serial Port (SSP) Access support [IXP45X/IXP46X product line only]
- IEEE1588 Time Synchronization (TSYNC) support [IXP46X product line only]

Parity Error Notification Access

- PCI-Parity and parity error detection support [IXP45X/IXP46X product line only]
- ECC [IXP46X product line only]

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