Customer Success

Sensata Technologies: Digital Multimedia

If a picture is worth a thousand words, an executable model is worth a thousand pictures

PROBLEM STATEMENT:

When designing a vision camera system, Sensata knows that decisions made at the architectural level have a great impact on the cost and quality of the final design. Sensata also understands that it is nearly impossible to make architectural changes late in the design cycle. Intel® CoFluent™ Studio enabled the design team to optimize its next-generation image sensing architecture early in the design cycle.

BUSINESS BENEFITS

- Improve productivity with system-level modeling
- Optimize system architecture with performance analysis iterations
- Facilitate team communications via easy to understand graphical notations
- Accurately validate design choices with architectural exploration

Sensata Technologies

Sensata Technologies (www.sensatatechnologies.com), formerly Texas Instruments Sensors & Controls, is the world's leading designer and supplier of sensors and controls. The name Sensata comes from the Latin word sensata, meaning "those gifted with sense."

Sensata's innovative solutions in sensors and controls improve safety, efficiency, and comfort for millions of people every day in automotive, appliance, aircraft, industrial, military, heating, air conditioning, data, telecommunications, and marine applications. Sensata, which currently employs approximately 9,500 people, manufactures over 20,000 different highly engineered and application-specific products. Over one billion units are shipped each year.

Digital Imaging

Sensata Technologies utilized Intel® CoFluent™ Studio system architecture design software to develop a new camera system aimed at automotive and security applications.

The design team created a model of a camera system to simulate the behavior and time properties in Intel® CoFluent™ Studio. Architectural choices were studied and hardware/software partitioning alternatives explored. For each architecture option, local memory requirements, potential traffic bottlenecks, execution times, and complexity of functions were studied and analyzed.

This type of decision was made using spreadsheets in the past. Other ESL tools were also evaluated. Only Intel® CoFluent™ Studio provides the high-level system architecture analysis in the early specification stage Sensata was looking for.

With Intel® CoFluent™ Studio, the Design Team Was Able to Determine the Impact of Various Architectures and Hardware/Software Partitioning Alternatives

Sensata wanted to study how components from a previous design could be merged into a single system-on-chip (SoC). If a single SoC was not optimal, they needed to determine the proper partition between separate components. A total of seven simulation models was created for comparison. Five simulation models were based upon a configuration that utilized a FPGA for image quality control and color processing.

The remaining two simulation models use a DSP for these functions.

Intel® CoFluent™ platform models were created by assembling generic hardware components to provide computing, communication, or storage resources. Hardware (ASIC FPGA, co-processor, accelerator, etc.) or software (DSP, CPU, MCU) computing units are called processors. Communication links, called nodes, can be characterized as bus, routing network, or point-to-point. Storage units are called shared memories. Universal behavioral and performance attributes characterize elements of a platform model.

DESIGN ACCOMPLISHMENTS

Intel®CoFluent™ Studio enabled Sensata to:

- Create, simulate, and analyze seven architectures in four weeks
- Locate potential bottlenecks that required multi-stage pipelines
- Utilized previously recorded performance data to ensure highly accurate simulation results
- Determine utilization for each function with varying pipeline length
- Compare dynamic memory utilization across architectures
- Determine effects of processor speed on dynamic power consumption
- Find the number of processing engines needed to meet timing requirements
- Optimize the tradeoff between memory size, power consumption, and cost

Sensata created and characterized three different platform configurations for representing potential execution structures:

- Platform 1: two hardware processors and a bus
- Platform 2: three hardware processors and a bus
- Platform 3: one hardware processor, one software processor, and a bus

The seven models were created with Intel® CoFluent™ Studio's drag-and-drop mapping feature that allows a single mouse click to allocate functions to processors. Intel® CoFluent™ Studio automatically generated the architecture models in SystemC. Memory sizes, power consumptions, and cost values were defined for processors, functions, operations, and FIFO channels. The design team could evaluate the utilization of each component at any level of the hierarchy as a load ratio (percentage) or in number of cycles per second.

The following table summarizes Sensata's findings for each of the seven simulations that served to identify the optimal architecture by providing guidelines for performance, memory, power, and cost tradeoffs.

Parameters								
	Model 1 (parallel)	Model 2 (pipeline)	Model 4 (pipeline)	Model 5 (DSP)	Model 5A (DSP)	Model 6 (2 chips)		Model 6A (2 chips)
Frame Length (pels)	309500	309500	309500	309500	309500	309500		309500
Clock Period (ns)	20	20	20	20	20	20		20
ProcRelativeSpeed	1	1	1	8	8	1		1
Block Num	14	x	x	x	x	14		14
Stage Num 1/2/3/4	x	6/17/10/6	6/17/10/6	x	x	x		x
Row Image	5	x	5	x	5	5		5
Simulation Results						HWProc2	HWProc3	
Memory Min (KB)	56,02	39,02	39,02	5,02	5,02	29,01	29,01	57,02
Memory Max	76,47	2305,87	67,94	2271,87	37,93	43,12	39,41	78,47
Memory Average	65,50	1099,12	52,53	738,84	17,02	36,89	31,18	66,69
Power Min (mW)	0	0	0	0	0	0	0	0
Power Max	50,66	54	54	48	48	40,832	54	75,66
Power Average	25,73	31,47	31,47	6,19	6,19	15,27	18,74	34,26
Cost	410	2678	391	1712	483	353	36	373

From this table, Sensata deduced that:

- Models 1, 4, 5A, 6, and 6A are preferred candidates compared to Models 2 and 5
- Models 1, 4, 6, and 6A are hardware implementations; Model 5A is a software implementation
- Models 1, 6, and 6A are parallel processing implementations
- Model 1 has lower power, but a small additional cost compared to Models 6 and 6A
- Model 6A has approximately 10% lower cost compared to Model 1

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