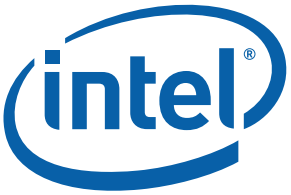

N-series Intel® Pentium® Processors and Intel® Celeron® Processors

Specification Update

December 2018

Revision 016

Document Number: 332095-016

Contents

Revision History

Revision	Description	Date
001	• Initial Release.	April 2015
002	• Errata — Added CHP36-41 • Identification Information — Updated Table 3 — Added Table 4 • Specification Changes — Added CHP1-CHP3 • Specification Clarifications — Added CHP1-CHP3	February 2016
003-009	• Revision Numbers Skipped	N/A
010	• Errata — Added errata CHP42-48	May 2017
011	• Revision Numbers Skipped	N/A
012	• Errata — Added erratum CHP49	July 2017
013	• Errata — Added CHP50-52	August 2017
014	• Errata — Added errata CHP53 — Updated table number in Specification Changes	January 2018
015	• Modified Preface section, Related Documents • Modified Summary Table of Changes section — In Errata, updated table with D1 introduced — In Specification Clarifications, added CHP4 and CHP5 data — In Documentation Changes, updated table • Modified Identification Information section, Component Identification using Programming Interface — Updated Table 1 • Updated section Specification Changes — Added CHP4 — Added CHP5 • Updated section Documentation Changes	May 2018
016	• Errata — Added CHP54	December 2018

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Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents

Document Title	Document Number	Location
N-series Intel® Pentium® Processors and Intel® Celeron® Processors Datasheet – Volume 1 of 3	332092	https://www.intel.com/content/www/us/en/processors/pentium/pentium-celeron-n-series-datasheet-vol-1.html
N-series Intel® Pentium® Processors and Intel® Celeron® Processors Datasheet – Volume 2 of 3	332093	https://www.intel.com/content/www/us/en/processors/pentium/pentium-celeron-n-series-datasheet-vol-2.html
N-series Intel® Pentium® Processors and Intel® Celeron® Processors Datasheet – Volume 3 of 3	332094	https://www.intel.com/content/www/us/en/processors/pentium/pentium-celeron-n-series-datasheet-vol-3.html

Related Documents

Document Title	Document Number/ Location
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference Manual A-M Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference Manual N-Z Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System Programming Guide Intel® 64 and IA-32 Intel Architecture Optimization Reference Manual	https://software.intel.com/en-us/articles/intel-sdm
Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes	https://software.intel.com/en-us/articles/intel-sdm
ACPI Specifications	www.acpi.info

Nomenclature

Errata are design defects or errors. These may cause the processor behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

S-Spec Number is a five-digit code used to identify products. Products are differentiated by their unique characteristics such as, core speed, L2 cache size, package type, etc. as described in the processor identification information table. Read all notes associated with each S-Spec number.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, and so on).

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Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the processor. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations.

Codes Used in Summary Tables

Stepping

X:	Errata exist in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of a table row indicates this erratum is either new or modified from the previous version of the document.

Errata (Sheet 1 of 3)

Number	Steppings		Status	ERRATA
	C0	D1		
CHP1	X	X	No Fix	The SoC May Not Detect a Battery Charger or May Fail to Connect to a USB Host
CHP2	X	X	No Fix	RGB666 Pixel Format Display Panel May Not Operate as Expected
CHP3	X	X	No Fix	LPDDR3 tINIT0 JEDEC* Duration May be Longer Than Specification Requirement
CHP4	X	X	No Fix	HDMI And DVI Displays May Flicker or Blank Out When Using Certain Pixel Frequencies
CHP5	X	X	No Fix	POPCNT Instruction May Take Longer to Execute Than Expected
CHP6	X	X	No Fix	LPSS UART Not Fully Compatible With 16550 UART
CHP7	X	X	No Fix	Accessing Undocumented Unimplemented MMIO Space May Cause a System Hang

Errata (Sheet 2 of 3)

Number	Steppings		Status	ERRATA
	C0	D1		
CHP8	X	X	No Fix	USB xHCI Controller May Not Re-Enter D3 State After a USB Wake Event
CHP9	X	X	No Fix	SoC PCIe* Gen 2 REFCLK Jitter Does Not Meet PCIe* Specification with SSC Enabled
CHP10	X	X	No Fix	SD Card / SDIO Controller PRESET_VALUE Does Not Change Transfer Frequency
CHP11	X	X	No Fix	Leakage Current on MIPI*-CSI Interface May Be Higher Than Specification
CHP12	X	X	No Fix	SATA Signal Voltage Level Violation
CHP13	X	X	No Fix	IA32_DEBUGCTL.FREEZE_PERFMON_ON_PMI is Incorrectly Cleared by SMI
CHP14	X	X	No Fix	Redirection of RSM to Probe Mode May Not Generate an LBR Record
CHP15	X	X	No Fix	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
CHP16	X	X	No Fix	Reported Memory Type May Not Be Used to Access the VMCS and Referenced Data Structures
CHP17	X	X	No Fix	A Page Fault May Not be Generated When the PS bit is set to "1" in a PML4E or PDPTE
CHP18	X	X	No Fix	Some Performance Counter Overflows May Not be Logged in IA32_PERF_GLOBAL_STATUS When FREEZE_PERFMON_ON_PMI is Enabled
CHP19	X	X	No Fix	CS Limit Violations May Not be Detected After VM Entry
CHP20	X	X	No Fix	PEBS Record EventingIP Field May be Incorrect After CS.Base Change
CHP21	X	X	No Fix	MOVNTDQA From WC Memory May Pass Earlier Locked Instructions
CHP22	X	X	No Fix	Performance Monitor Instructions Retired Event May Not Count Consistently
CHP23	X	X	No Fix	LBR Stack And Performance Counter Freeze on PMI May Not Function Correctly
CHP24	X	X	No Fix	VM Exit May Set IA32_EFER.NXE When IA32_MISC_ENABLE Bit 34 is Set to 1
CHP25	X	X	No Fix	Machine Check Status Overflow Bit May Not be Set
CHP26	X	X	No Fix	LPDDR3 tINIT0 Duration May be Longer Than Specification Requirement
CHP27	X	X	No Fix	xHCI USB2.0 Split-Transactions Error Counter Reset Issue
CHP28	X	X	No Fix	SoC May Not Meet PCIe* Clock Jitter Specification
CHP29	X	X	No Fix	SATA Host Controller Does Not Pass Certain Compliance Tests
CHP30	X	X	No Fix	RTIT Trace May Contain FUP.FAR Packet With Incorrect Address
CHP31	X	X	No Fix	RTIT May Delay The PSB by One Packet
CHP32	X	X	No Fix	RTIT TraceStop Condition Detected During Buffer Overflow May Not Clear TraceActive
CHP33	X	X	No Fix	RTIT FUP.BuffOvf Packet May be Incorrectly Followed by a TIP Packet
CHP34	X	X	No Fix	RTIT CYC Packet Payload Values May be Off by 1 Cycle
CHP35	X	X	No Fix	First MTC Packet After RTIT Enable May be Incorrect
CHP36	X	X	No Fix	USB Device Mode May Not be functional when connected to USB1.x
CHP37	X	X	No Fix	Cursor Movements Towards The Edges of Pipe-C Display May Cause Unpredictable Display Behavior
CHP38	X	X	No Fix	Multiple Drivers That Access the GPIO Registers Concurrently May Result in Unpredictable System Behavior
CHP39	X	X	No Fix	Power Rail Leakage at Power On
CHP40	X	X	No Fix	PCIe* REFCLK Drivers Remain Enabled in Sx States
CHP41	X	X	No Fix	SD Card / SDIO Controller PRESET_VALUE Does Not Change Transfer Frequency

Errata (Sheet 3 of 3)

Number	Steppings		Status	ERRATA
	C0	D1		
CHP42	X	X	No Fix	Incorrect Detection of USB LFPS May Lead to USB 3.0 Link Errors
CHP43	X	X	No Fix	USB High Speed Links May Disconnect When Subject to EFT Events
CHP44	X	X	No Fix	XHCI USB Controller May Not Resume After S3 Exit
CHP45	X	X	No Fix	LPC SERR Generation Can Not be Independently Disabled
CHP46	X	X	No Fix	Some RTIT Packets Following PSB May be Sent Out of Order or Dropped
CHP47	X	X	No Fix	System May Hang When DDR Dynamic Self-Refresh is Enabled
CHP48	X	X	No Fix	USB3 PHY May Become Unreliable On Certain SoC Parts
CHP49	X	X	No Fix	System May Experience Inability to Boot or May Cease Operation
CHP50	X	X	No Fix	xHCI Host Controller Reset May Lead to System Hang
CHP51	X	X	No Fix	LPC Clock Control Using the LPC_CLKRUN# May Not Behave As Expected
CHP52	X	X	No Fix	Processor May Not Wake From C6 or Deeper Sleep State
CHP53	X	X	No Fix	LPC_AD3 Signal May Not Behave As Expected During Read or Write Cycle Turnaround Periods
CHP54	X	X	No Fix	eMMC, SD Card, or SDIO CRC Detection

Specification Changes

Number	SPECIFICATION CHANGES
CHP1	VNN Sx Iccmax Specification Update
CHP2	Icc_{max} Definition
CHP3	ICCmax Specification Update for Desktop D1 Stepping SKUs
CHP4	Digital Display Interface Update
CHP5	RTC Register Setting Changes

Specification Clarifications

Number	SPECIFICATION CLARIFICATIONS
CHP1	General Power States for System
CHP2	Enabling SoC USB Debug Port
CHP3	Digital Thermal Sensor (DTS) Accuracy

Documentation Changes

Number	DOCUMENTATION CHANGES
1	HPET feature is not supported
2	Memory Space Address Mapping
3	Note in Section 16.8 of N- Series Intel® Pentium® Processors and Intel® Celeron® Processors Datasheet
4	Information Changes in table 2-17 PCU-LPC Bridge Interface Signals (Sheet 2 of 2)
5	Information Changes in table 2-27 GPIO Multiplexing and Modes (Sheet 4 of 6)
6	V_{IH} Definition incorrect in multiple places in the Datasheet
7	Section 2.5 GPIO Multiplexing, Table 2-27. GPIO Multiplexing and Modes (Sheet 3 or 6)
8	Section 2.1 Platform Power Rails, Table 2-1. Platform Power Well Definitions

Documentation Changes

Number	DOCUMENTATION CHANGES
9	Information changes in section 29.2.182 Device Mode Control Reg 0 (DUAL_ROLE_CFG_REG0)-Offset 80D8H
10	Additional notes to describe the bit range
11	Additional notes to describe the bit range
12	Additional notes to describe the bit range
13	Additional notes to describe the bit range

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Identification Information

Component Identification using Programming Interface

The processor stepping can be identified by the following register contents.

Table 1. Processor Line Component Identification

Reserved	Extended Family[1]	Extended Model[2]	Reserved	SoC Type[3]	Family Code	Model Number[5]	Stepping ID[6]
31:28	27:20	19:16	15:13	12	11:8	7:4	3:0
0000b	0000000b	0100b	000b	0b	0110b	1100b	C0:0011b D1: 0100b

Notes:
1. The Extended Family, Bits [27:20] are used in conjunction with the Family Code, specified in Bits[11:8], to indicate whether the processor belongs to the Intel386™, Intel486™, Pentium®, Pentium® 4, Intel® Core™ SoC family.
2. The Extended Model, bits [19:16] in conjunction with the Model Number, specified in bits [7:4], are used to identify the model of the SoC within the SoC family.
3. The SoC Type, specified in bits [13:12] indicates whether the SoC is an original OEM SoC, an OverDrive SoC, or a dual SoC (capable of being used in a dual SoC system.
4. The Family Code corresponds to bits [11:8] of the EDX register after RESET, bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
5. The Model Number corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
6. The Stepping ID in bits [3:0] indicates the revision number of that model. See Table 2 for the SoC stepping ID number in the CPUID information.

When EAX is initialized to a value of '1', the CPUID instruction returns the Extended Family, Extended Model, Processor Type, Family Code, Model Number and Stepping ID value in the EAX register. Note that the EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX and EDX registers after the CPUID instruction is executed with a 2 in the EAX register.

The processor can be identified by the following register contents.

Table 2. Processor Identification by Register Contents

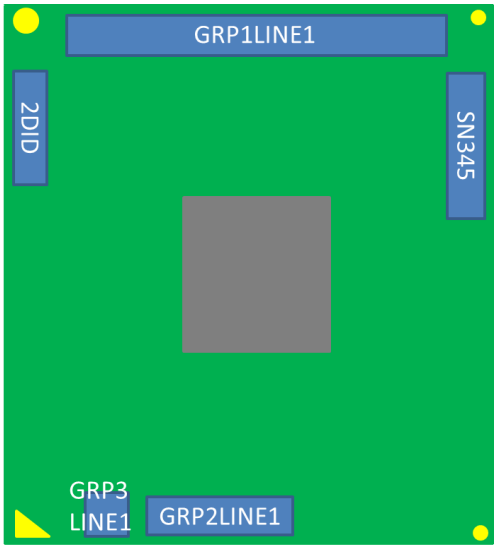
Processor Line	Stepping	Vendor ID[1]	Host Device ID[2]	Processor Graphics Device ID[3]	Revision ID[4]
Intel® Pentium® processor Series and Intel® Celeron® processor Series	C-0	8086h	2280h	22B1h	8'h21
Intel® Pentium® processor Series and Intel® Celeron® processor Series	D-1	8086h	2280h	22B1h	8'h35

Notes:
1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00h–01h in the PCI function 0 configuration space.
2. The Host Device ID corresponds to bits 15:0 of the Device ID Register located at Device 0 offset 02h–03h in the PCI function 0 configuration space.
3. The Processor Graphics Device ID (DID2) corresponds to bits 15:0 of the Device ID Register located at Device 2 offset 02h–03h in the PCI function 0 configuration space.
4. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The processor stepping can be identified by the following component markings.

Figure 1. Processor Family Top-Side Markings



Sample Marking Information:
GRP1LINE1: i{M}{C}YY_FPO12345
GRP2LINE1: SSPEC
GRP3LINE1: {e1}

Table 3. Processor Identification (Sheet 1 of 2)

S-Spec #	MM Number	Processor #	Step-ping	Cache Size (MB)	Func-tional Core	Graphic Freq. (MHz)	Graphic Burst Freq. (MHz)	Graphic Execution Units	Core Freq. (GHz)	Core Burst Freq. (GHz)	Mem. (MHz)	Therm. Design Power (W)
QK0G	94990	Pentium® N3710	D1	2	4	400	700	16	1.6	2.56	1600	6
QK0K	94993	Celeron® N3160	D1	2	4	320	640	12	1.6	2.24	1600	6
QK0J	94992	Celeron® N3060	D1	2	2	320	600	12	1.6	2.48	1600	6
QK0H	94991	Celeron® N3010	D1	2	2	320	600	12	1.04	2.24	1600	4
QK0L	944994 (Desktop SKU)	Pentium® J3710	D1	2	4	400	740	16	1.6	2.64	1600	6.5
QK0N	944996 (Desktop SKU)	Celeron® J3160	D1	2	4	320	700	12	1.6	2.24	1600	6

Table 3. Processor Identification (Sheet 2 of 2)

S-Spec #	MM Number	Processor #	Step-ping	Cache Size (MB)	Func-tional Core	Graphic Freq. (MHz)	Graphic Burst Freq. (MHz)	Graphic Execution Units	Core Freq. (GHz)	Core Burst Freq. (GHz)	Mem. (MHz)	Therm. Design Power (W)
QK0M	944995 (Desktop SKU)	Celeron® J3060	D1	2	2	320	700	12	1.6	2.48	1600	6
S-R29E	942599	Pentium® N3700	C0	2	4	400	700	16	1.6	2.4	1600	6
S-R2A7	943327 (Desktop sku)	Pentium® N3700	C0	2	4	400	700	16	1.6	2.4	1600	6
S-R29F	942600	Celeron® N3150	C0	2	4	320	640	12	1.6	2.08	1600	6
S-R2A8	943328 (Desktop sku)	Celeron® N3150	C0	2	4	320	640	12	1.6	2.08	1600	6
S-R29H	942602	Celeron® N3050	C0	2	2	320	600	12	1.6	2.16	1600	6
S-R2A9	943329 (Desktop sku)	Celeron® N3050	C0	2	2	320	600	12	1.6	2.16	1600	6
S-R29J	942603	Celeron® N3000	C0	2	2	320	600	12	1.04	2.08	1600	4
S-R2KL	94990	Pentium® N3710	D1	2	4	400	700	16	1.6	2.56	1600	6
S-R2KP	94993	Celeron® N3160	D1	2	4	320	640	12	1.6	2.24	1600	6
S-R2KN	94992	Celeron® N3060	D1	2	2	320	600	12	1.6	2.48	1600	6
S-R2KM	94991	Celeron® N3010	D1	2	2	320	600	12	1.04	2.24	1600	4
S-R2KQ	944994 (Desktop SKU)	Pentium® J3710	D1	2	4	400	740	16	1.6	2.64	1600	6.5
S-R2KS	944996 (Desktop SKU)	Celeron® J3160	D1	2	4	320	700	12	1.6	2.24	1600	6
S-R2KR	944995 (Desktop SKU)	Celeron® J3060	D1	2	2	320	700	12	1.6	2.48	1600	6

Table 4. D-1 Step Graphics Identification Table

Segment	Stepping	SKU	Graphics Branding
Mobile	D1	Pentium® N3710	Intel® HD Graphics 405
Mobile	D1	Celeron® N3160, N3060, N3010	Intel® HD Graphics 400
Desktop	D1	Pentium® J3710	Intel® HD Graphics 405
Desktop	D1	Celeron® J3160, J3060	Intel® HD Graphics 400
Note: No specific graphics branding for C-Step			

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Errata

CHP1. The SoC May Not Detect a Battery Charger or May Fail to Connect to a USB Host

Problem: During power-on, when the SoC is used in device mode instead of host mode, the USB D+ line may have a 2 µsec glitch to 3.3 V.

Implication: Due to this erratum, the platform may not detect a battery charger (and hence not charge the battery) or the SoC may not successfully connect to an attached USB host.

Workaround: Power the SoC on before connecting to its USB port. Alternatively, manually disconnecting and re-connecting the USB cable restores operation after the erratum has occurred.

Status: For the steppings affected, see the Summary Table of Changes.

CHP2. RGB666 Pixel Format Display Panel May Not Operate as Expected

Problem: Due to this erratum, the RGB666 format support on the SOC has restrictions on the horizontal resolution. For single link MIPI* DSI (Display Serial Interface), the horizontal resolution must be evenly divisible by 4. For dual link MIPI DSI, one-half the horizontal resolution plus the overlapping pixels must be evenly divisible by 4.

Implication: Due to this erratum, the RGB666 panel may not operate as expected.

Workaround: For dual link panels with overlap, choose the overlap so that one-half the horizontal resolution plus the overlapping pixels is evenly divisible by 4. For single link panels the horizontal resolution must be evenly divisible by 4

Status: For the steppings affected, see the Summary Table of Changes.

CHP3. LPDDR3 tINIT0 JEDEC* Duration May be Longer Than Specification Requirement

Problem: JEDEC Standard JESD209-3 requires a maximum power ramp duration tINIT0 of 20ms. Due to this erratum, the SoC may not comply with the tINIT0 specification.

Implication: Intel has not observed this erratum to impact the functionality or performance of any commercially available LPDDR3 parts. Intel has obtained waivers from vendors who provide commonly used LPDDR3 DRAM parts

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP4. HDMI And DVI Displays May Flicker or Blank Out When Using Certain Pixel Frequencies

Problem: Due to this erratum, HDMI (High-Definition Multimedia Interface) and DVI (Digital Visual Interface) ports may send data out at an incorrect rate, that is different than the one requested when using certain pixel frequencies.

Implication: When this erratum occurs, panels may flicker or blank out. The impacted pixel frequencies are: 218.25MHz, 218.70MHz, 220.50MHz, 221.20MHz, 229.50MHz, 233.793MHz and 234.00MHz.

Workaround: Select a video mode that does not use an affected pixel frequency.

Status: For the steppings affected, see the Summary Table of Changes.

CHP5. POPCNT Instruction May Take Longer to Execute Than Expected

Problem: POPCNT instruction execution with a 32 or 64 bit operand may be delayed until previous non-dependent instructions have executed.

Implication: Software using the POPCNT instruction may experience lower performance than expected.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP6. LPSS UART Not Fully Compatible With 16550 UART

Problem: Stick Parity bit, LCR[5], (Line Control Register, HSUART0_BAR0, Offset 0CH; bit [5] for HSUART0 and HSUART1_BAR0, Offset 0CH; bit [5] for HSUART1) does not follow the 16550 specified behavior, instead the parity bit is always logic 0.

Implication: LPSS (Low Power Sub-system) UARTs are not fully 16550 compatible and may cause an error when connected to a UART device that requires the Stick Parity feature.

Workaround: Do not use Stick Parity mode of UART.

Status: For the steppings affected, see the Summary Table of Changes.

CHP7. Accessing Undocumented Unimplemented MMIO Space May Cause a System Hang

Problem: Access to undocumented unimplemented MMIO space should result in a software error. Due to this erratum, an access to undocumented unimplemented MMIO space may not complete.

Implication: When this erratum occurs, the system may hang.

Workaround: Do not access to undocumented unimplemented MMIO space.

Status: For the steppings affected, see the Summary Table of Changes.

CHP8. USB xHCI Controller May Not Re-Enter D3 State After a USB Wake Event

Problem: After processing a USB wake event, the USB xHCI controller may not reenter D3 state.

Implication: When this erratum occurs, the affected USB xHCI controller may not recognize subsequent USB wake events. When this erratum occurs, PME status bit [15] of register Power Management Control/Status (PM_CS) (Bus 0; Device 20; Function 20; Offset 74H) remains at 1.

Workaround: The software driver should set PMCTRL[28] (Bus 0; Device 14; Function 0; Offset 80A4H) after the xHCI controller enters D0 state following an exit from D3 state.

Status: For the steppings affected, see the Summary Table of Changes.

CHP9. SoC PCIe* Gen 2 REFCLK Jitter Does Not Meet PCIe* Specification with SSC Enabled

Problem: SoC PCIe* REFCLK does not meet PCIe* jitter specification when SSC is enabled.

Implication: This issue only impacts PCIe* interface when it is running at Gen 2 speed when SSC is enabled. No impact to PCIe* Gen 1 operation. Intel has not observed any functional failures due to this erratum.

Workaround: There are no known issues with enabling SSC on PCIe interface that operates at Gen 1 speed. However, if SSC is enabled while PCIe* interface is running at Gen 2 speed, system REFCLK will experience jitter would not meet PCIe specifications.

Status: For the steppings affected, see the Summary Table of Changes.

CHP10. SD Card / SDIO Controller PRESET_VALUE Does Not Change Transfer Frequency

Problem: The PRESET_VALUE (CMD12_ERR_STAT_HOST_CTRL_2 CSR at Bus 0; Device 18; Function 0; Offset 3CH, bit 31) does not change the SD Card/ SDIO bus transfer frequency as required by the SD Host Controller Standard Specification Version 3.0.

Implication: Drivers that attempt to utilize PRESET_VALUE may not obtain the maximum transfer rate of an attached UHS SD card or SDIO bus.

Workaround: Software should set the UHS_MODE field (bits [18:16] of the CMD12_ERR_STAT_HOST_CTRL_2 CSR) before setting the PRESET_VALUE bit to reach the maximum transfer rate.

Status: For the steppings affected, see the Summary Table of Changes.

CHP11. Leakage Current on MIPI*-CSI Interface May Be Higher Than Specification

Problem: The leakage current on the MIPI-CSI interface may exceed the specified limit of ± 10µA.

Implication: Intel has not observed any functional or reliability failures due to this erratum.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP12. SATA Signal Voltage Level Violation

Problem: SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the SATA transmit signaling voltage levels may exceed the maximum motherboard Tx connectors and device RX connector voltage specifications as defined in Section 7.2.2.3 of Serial ATA specification, Rev3.1. This issue applies to Gen1 (1.5Gb/s).

Implication: None known.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP13. IA32_DEBUGCTL.FREEZE_PERFMON_ON_PMI is Incorrectly Cleared by SMI

Problem: FREEZE_PERFMON_ON_PMI (bit 12) in the IA32_DEBUGCTL MSR (1D9H) is erroneously cleared during delivery of an SMI (system-management interrupt).

Implication: As a result of this erratum the performance monitoring counters will continue to count after a PMI occurs in SMM (system-management Mode).

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP14. Redirection of RSM to Probe Mode May Not Generate an LBR Record

Problem: A redirection of the RSM instruction to probe mode may not generate the LBR (Last Branch Record) record that would have been generated by a non-redirected RSM instruction.

Implication: The LBR stack may be missing a record when redirection of RSM to probe mode is used. The LBR stack will still properly describe the code flow of non-SMM code.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP15. Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results

Problem: The act of one processor or system bus master writing data into a currently executing code segment of a second processor with the intent of having the second processor execute that data as code is called cross-modifying code (XMC). XMC that does not force the second processor to execute a synchronizing instruction prior to execution of the new code is called unsynchronized XMC. Software using unsynchronized XMC to modify the instruction byte stream of a processor can see unexpected or unpredictable execution behavior from the processor that is executing the modified code.

Implication: In this case the phrase "unexpected or unpredictable execution behavior" encompasses the generation of most of the exceptions listed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide including a General Protection Fault (GPF) or other unexpected behaviors. In the event that unpredictable execution causes a GPF the application executing the unsynchronized XMC operation would be terminated by the operating system.

Workaround: In order to avoid this erratum programmers should use the XMC synchronization algorithm as detailed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide Section: Handling Self- and Cross-Modifying Code.

Status: For the steppings affected, see the Summary Table of Changes.

CHP16. Reported Memory Type May Not Be Used to Access the VMCS and Referenced Data Structures

Problem: Bits 53:50 of the IA32_VMX_BASIC MSR report the memory type that the processor uses to access the VMCS and data structures referenced by pointers in the VMCS. Due to this erratum, a VMX access to the VMCS or referenced data structures will instead use the memory type that the MTRRs (memory-type range registers) specify for the physical address of the access.

Implication: Bits 53:50 of the IA32_VMX_BASIC MSR report that the WB (write-back) memory type will be used but the processor may use a different memory type.

Workaround: Software should ensure that the VMCS and referenced data structures are located at physical addresses that are mapped to WB memory type by the MTRRs.

Status: For the steppings affected, see the Summary Table of Changes.

CHP17. A Page Fault May Not be Generated When the PS bit is set to "1" in a PML4E or PDPTE

Problem: On processors supporting Intel® 64 architecture the PS bit (Page Size bit 7) is reserved in PML4Es and PDPTEs. If the translation of the linear address of a memory access encounters a PML4E or a PDPTE with PS set to 1 a page fault should occur. Due to this erratum, PS of such an entry is ignored and no page fault will occur due to it is being set.

Implication: Software may not operate properly if it relies on the processor to deliver page faults when reserved bits are set in paging-structure entries.

Workaround: Software should not set bit 7 in any PML4E or PDPTE that has Present Bit (Bit 0) set to "1".

Status: For the steppings affected, see the Summary Table of Changes.

CHP18. Some Performance Counter Overflows May Not be Logged in IA32_PERF_GLOBAL_STATUS When FREEZE_PERFMON_ON_PMI is Enabled

Problem: When enabled, FREEZE_PERFMON_ON_PMI bit 12 in IA32_DEBUGCTL MSR (1D9H) freezes PMCs (performance monitoring counters) on a PMI (Performance Monitoring Interrupt) request by clearing the IA32_PERF_GLOBAL_CTRL MSR (38FH). Due to this erratum, when FREEZE_PERFMON_ON_PMI is enabled and two or more PMCs overflows within a small window of time and PMI is requested, then subsequent PMC overflows may not be logged in IA32_PERF_GLOBAL_STATUS MSR (38EH).

Implication: On a PMI, subsequent PMC overflows may not be logged in IA32_PERF_GLOBAL_STATUS MSR.

Workaround: Re-enabling the PMCs in IA32_PERF_GLOBAL_CTRL will log the overflows that were not previously logged in IA32_PERF_GLOBAL_STATUS.

Status: For the steppings affected, see the Summary Table of Changes.

CHP19. CS Limit Violations May Not be Detected After VM Entry

Problem: The processor may fail to detect a CS limit violation on fetching the first instruction after VM entry if the first byte of that instruction is outside the CS limit but the last byte of the instruction is inside the limit.

Implication: The processor may erroneously execute an instruction that should have caused a general protection exception.

Workaround: When a VMM emulates a branch instruction it should inject a general protection exception if the instruction’s target EIP is beyond the CS limit.

Status: For the steppings affected, see the Summary Table of Changes.

CHP20. PEBS Record EventingIP Field May be Incorrect After CS.Base Change

Problem: Due to this erratum a PEBS (Precise Event Base Sampling) record generated after an operation which changes CS.Base may contain an incorrect address in the EventingIP field.

Implication: Software attempting to identify the instruction which caused the PEBS event may identify the incorrect instruction when non-zero CS.Base is supported and CS.Base is changed. Intel has not observed this erratum to impact the operation of any commercially available system.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP21. MOVNTDQA From WC Memory May Pass Earlier Locked Instructions

Problem: An execution of MOVNTDQA that loads from WC (write combining) memory may appear to pass an earlier locked instruction to a different cache line.

Implication: Software that expects a lock to fence subsequent MOVNTDQA instructions may not operate properly. If the software does not rely on locked instructions to fence the subsequent execution of MOVNTDQA then this erratum does not apply.

Workaround: Software that requires a locked instruction to fence subsequent executions of MOVNTDQA should insert an LFENCE instruction before the first execution of MOVNTDQA following the locked instruction. If there is already a fencing or serializing instruction between the locked instruction and the MOVNTDQA, then an additional LFENCE is not necessary.

Status: For the steppings affected, see the Summary Table of Changes.

CHP22. Performance Monitor Instructions Retired Event May Not Count Consistently

Problem: Performance Monitor Instructions Retired (Event C0H; Umask 00H) and the instruction retired fixed counter (IA32_FIXED_CTR0 MSR (309H)) are used to track the number of instructions retired. Due to this erratum, certain situations may cause the counter(s) to increment when no instruction has retired or to not increment when specific instructions have retired.

Implication: A performance counter counting instructions retired may over or under count. The count may not be consistent between multiple executions of the same code.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP23. LBR Stack And Performance Counter Freeze on PMI May Not Function Correctly

Problem: When FREEZE_LBRS_ON_PMI flag (bit 11) in IA32_DEBUGCTL MSR (1D9H) is set, the LBR (Last Branch Record) stack is frozen on a hardware PMI (Performance Monitoring Interrupt) request. When FREEZE_PERFMON_ON_PMI flag (bit 12) in IA32_DEBUGCTL MSR is set, a PMI request clears each of the ENABLE fields of the IA32_PERF_GLOBAL_CTRL MSR (38FH) to disable counters. Due to this erratum, when FREEZE_LBRS_ON_PMI and/or FREEZE_PERFMON_ON_PMI is set in IA32_DEBUGCTL MSR and the local APIC is disabled or the PMI LVT is masked, the LBR Stack and/or Performance Counters Freeze on PMI may not function correctly.

Implication: Performance monitoring software may not function properly if the LBR Stack and Performance Counters Freeze on PMI do not operate as expected. Intel has not observed this erratum to impact any commercially available system.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP24. VM Exit May Set IA32_EFER.NXE When IA32_MISC_ENABLE Bit 34 is Set to 1

Problem: When "XD Bit Disable" in the IA32_MISC_ENABLE MSR (1A0H) bit 34 is set to 1, it should not be possible to enable the "execute disable" feature by setting IA32_EFER.NXE. Due to this erratum, a VM exit that occurs with the 1-setting of the "load IA32_EFER" VM-exit control may set IA32_EFER.NXE even if IA32_MISC_ENABLE bit 34 is set to 1. This erratum can occur only if IA32_MISC_ENABLE bit 34 was set by guest software in VMX non-root operation.

Implication: Software in VMX root operation may execute with the "execute disable" feature enabled despite the fact that the feature should be disabled by the IA32_MISC_ENABLE MSR. Intel has not observed this erratum with any commercially available software.

Workaround: A virtual-machine monitor should not allow guest software to write to the IA32_MISC_ENABLE MSR.

Status: For the steppings affected, see the Summary Table of Changes.

CHP25. Machine Check Status Overflow Bit May Not be Set

Problem: The OVER (error overflow) indication in bit [62] of the IA32_MC0_STATUS MSR (401H) may not be set if IA32_MC0_STATUS.MCACOD (bits [15:0]) held a value of 0x3 (External Error) when a second machine check occurred in the MC0 bank. Additionally, the OVER indication may not be set if the second machine check has an MCACOD value of 0x810, 0x820 or 0x410, regardless of the first error.

Implication: Software may not be notified that an overflow of MC0 bank occurred.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP26. LPDDR3 tINIT0 Duration May be Longer Than Specification Requirement

Problem: JEDEC Standard JESD209-3 requires a maximum power ramp duration tINIT0 of 20ms. Due to this erratum, the SoC may not comply with the tINIT0 specification.

Implication: Intel has not observed this erratum to impact the functionality or performance of any commercially available LPDDR3 parts. Intel has obtained waivers from vendors who provide commonly used LPDDR3 DRAM parts.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP27. xHCI USB2.0 Split-Transactions Error Counter Reset Issue

Problem: The xHCI controller may not reset its split transaction error counter if a high-speed USB hub propagates a mal-formed bit from a low-speed or full-speed USB device exhibiting non-USB specification compliant signal quality.

Implication: The implication is device dependent.

- Full Speed and Low Speed devices behind the hub may be re-enumerated and may cause a device to not function as expected.

Workaround: Software driver can be modified to workaround this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

CHP28. SoC May Not Meet PCIe* Clock Jitter Specification

Problem: The SoC's PCIe REFCLK signals may not meet PCIe jitter specifications when operating at 5.0 GT/s with SSC (Spread Spectrum Clocking) enabled.

Implication: The platform may not meet REFCLK jitter specification. Intel has not observed any functional failures due to this erratum.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP29. SATA Host Controller Does Not Pass Certain Compliance Tests

Problem: The SoC SATA host controller OOB (Out of Band) Host Responses, OOB Transmit Gap, and OOB Transmit Burst Length do not pass Serial ATA Interoperability Program Revision 1.4.3, Unified Test Document Version 1.01 tests OOB-03[a/b], OOB-05, and OOB-06[a/b].

Implication: Intel has obtained a waiver for these tests. Intel has not observed any functional failures due to this erratum.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP30. RTIT Trace May Contain FUP.FAR Packet With Incorrect Address

Problem: The FUP.FAR (Flow Update Packet for Far Transfer) generated by RTIT (Real Time Instruction Trace) on a far transfer instruction should contain the linear address of the first byte of the next sequential instruction after the far transfer instruction. Due to this erratum, far transfer instructions with more than 3 prefixes may incorrectly include an address between the first byte of the far transfer instruction and the last byte of the far transfer instruction.

Implication: The RTIT Trace decoder may incorrectly decode the trace due to an incorrect address in the FUP packet.

Workaround: The RTIT trace decoder can identify a FUP.FAR in the middle of a far transfer instruction and treat that FUP.FAR as if it was coming from the first byte of the following sequential instruction.

Status: For the steppings affected, see the Summary Table of Changes.

CHP31. RTIT May Delay The PSB by One Packet

Problem: After an RTIT (Real Time Instruction Trace) packet that exceeds the limit specified by Pkt_Mask in RTIT_PACKET_COUNT (MSR 77Ch) bits [17:16], the PSB (Packet Stream Boundary) packet should be sent immediately. Due to this erratum, the PSB packet may be delayed by one packet.

Implication: The PSB packet may be delayed by one packet.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP32. RTIT TraceStop Condition Detected During Buffer Overflow May Not Clear TraceActive

Problem: If an RTIT (Real Time Instruction Trace) TraceStop condition is detected while RTIT_STATUS.Buffer_Overflow MSR (769H) bit 3 is set, the processor may not clear RTIT_CTL.TraceActive MSR (768H) bit 13, and tracing will continue after the overflow resolves. Such a case will be evident if the TraceStop packet is inserted before overflow is resolved, as indicated by the FUP.BuffOvf (Flow Update Packet for Buffer Overflow) packet.

Implication: The RTIT trace will continue tracing beyond the intended stop point.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP33. RTIT FUP.BuffOvf Packet May be Incorrectly Followed by a TIP Packet

Problem: When RTIT (Real Time Instruction Trace) suffers an internal buffer overflow, packet generation stops temporarily, after which a FUP.BuffOvf (Flow Update Packet for Buffer Overflow) is sent to indicate the LIP that follows the instruction upon which tracing resumes. In some cases, however, this packet will be immediately followed by a FUP.TIP (Flow Update Packet for Target IP) which was generated by a branch instruction that executed during the overflow. The IP payload of this FUP.TIP will be the LIP of the instruction upon which tracing resumes.

Implication: The spurious FUP.TIP packet may cause the RTIT trace decoder to fail.

Workaround: The RTIT trace decoder should ignore any FUP.TIP packet that immediately follows a FUP.BuffOvf whose IP matches the IP payload of the FUP.BuffOvf.

Status: For the steppings affected, see the Summary Table of Changes.

CHP34. RTIT CYC Packet Payload Values May be Off by 1 Cycle

Problem: When RTIT (Real Time Instruction Trace) is enabled with RTIT_CTL.Cyc_Acc MSR (768H) bit 1 set to 1, all CYC (Cycle Count) packets have a payload value that is one less than the number of cycles that have actually passed. Note that for CYC packets with a payload value of 0, the correct value may be 0 or 1.

Implication: The trace decoder will produce inaccurate performance data when using CYC packets to track software performance.

Workaround: As a partial workaround, the trace decoder should add 1 to the payload value of any CYC packet with a non-zero payload.

Status: For the steppings affected, see the Summary Table of Changes.

CHP35. First MTC Packet After RTIT Enable May be Incorrect

Problem: When RTIT (Real Time Instruction Trace) is enabled, indicated by TriggerEn in bit 2 of the RTIT_STATUS MSR (769H) transitioning from 0 to 1, the first MTC (Mini Time Counter) packet may be sent at the wrong time.

Implication: The RTIT trace decoder will make incorrect assumptions about the TSC value based on an asynchronous MTC packet.

Workaround: The RTIT trace decoder should ignore the first MTC that follows trace enabling.

Status: For the steppings affected, see the Summary Table of Changes.

CHP36. USB Device Mode May Not be functional when connected to USB1.x

Problem: Device Mode may not be functional when connected to USB 1.x host or hub.

Implication: Due to this erratum, the SoC in Device Mode may be unable to connect to USB 1.x host or hub.

Workaround: None identified..

Status: For the steppings affected, see the Summary Table of Changes.

CHP37. Cursor Movements Towards The Edges of Pipe-C Display May Cause Unpredictable Display Behavior

Problem: Moving the cursor rapidly towards the edges of the display connected to Pipe-C may result in loss of display, display flickering, or other display artifact requiring a display pipe restart.

Implication: When this erratum occurs, cursor movements can affect the display image.

Workaround: It is possible for the display driver to contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

CHP38. Multiple Drivers That Access the GPIO Registers Concurrently May Result in Unpredictable System Behavior

Problem: The PCU (Platform Control Unit) in SoC may not be able to process concurrent accesses to the GPIO registers. Due to this sighting, read instructions may return 0xFFFFFFFF and write instructions may be dropped.

Implication: Multiple drivers concurrently accessing GPIO registers may result in unpredictable system behavior.

Workaround: It is possible for the display driver to contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

CHP39. Power Rail Leakage at Power On

Problem: At power on, leakage from the V1P05A power rail to the V1P8A power rail may result in raising the V1P8A rail to about 400mV prior to that rail being powered.

Implication: Intel has not observed this erratum to impact the operation of any commercially available platform.

Workaround: None identified.

CHP40. PCIe* REFCLK Drivers Remain Enabled in Sx States

Problem: In Sx states, the PCIe REFCLK (CLK_DIFF_N [0:3]) signals stay at 1.05V level instead of shutting off completely.

Implication: Intel has observed a worst case leakage of about 6mW per clock pair during Sx states for each connected PCIe device. Intel has not observed any functional failures as a result of this erratum.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP41. SD Card / SDIO Controller PRESET_VALUE Does Not Change Transfer Frequency

Problem: The PRESET_VALUE (CMD12_ERR_STAT_HOST_CTRL_2 CSR at Bus 0; Device 18; Function 0; MMIO Offset 3CH, bit 31) does not change the SD Card/ SDIO bus transfer frequency as required by the SD Host Controller Standard Specification Version 3.0.

Implication: Drivers that attempt to utilize PRESET_VALUE may not obtain the maximum transfer rate of an attached UHS SD card or SDIO bus.

Workaround: Software should set the UHS_MODE field (bits [18:16] of the CMD12_ERR_STAT_HOST_CTRL_2 CSR) before setting the PRESET_VALUE bit to reach the maximum transfer rate.

Status: For the steppings affected, see the Summary Table of Changes.

CHP42. Incorrect Detection of USB LFPS May Lead to USB 3.0 Link Errors

Problem: The USB 3.0 host controller may incorrectly detect LFPS (Low Frequency Periodic Signal) on certain SoC parts.

Implication: When this erratum occurs, the USB 3.0 host controller may not enumerate the link or may encounter unrecoverable errors during operation.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

CHP43. USB High Speed Links May Disconnect When Subject to EFT Events

Problem: When subjected to EFT (Electric Fast Transient) events, the xHCI host controller USB 2.0 interface may not meet CE Certification requirements according to IEC 61000-4-4 connected to a USB device with an unshielded cable on a USB2 root port.

Implication: When this erratum occurs, the USB high speed device may be falsely disconnected. This will result in failure of the IEC 61000-4-4 EFT test.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP44. XHCI USB Controller May Not Resume After S3 Exit

Problem: The SoC’s XHCI USB controller may hang during an S3 Exit event.

Implication: Subsequent to an S3 exit, the platform’s USB ports may be unavailable.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

CHP45. LPC SERR Generation Can Not be Independently Disabled

Problem: LPC SERR# events are incorrectly propagated to trigger the NMI interrupt when the SEE field of the PCIE_REG_COMMAND register (Bus 0; Device 31; Function 0; Offset 4h) is cleared. This erratum only affects systems with attached LPC devices that signal SERR# events.

Implication: SERR for LPC cannot be disabled using PCIE_REG_COMMAND SEE bit. SERR# is used on the LPC bus to carry the legacy ISA IOCHK# parity error indication.

Workaround: None identified. Software can clear NSC (NMI Status and Control) MSR (Bus 0; Device 31; Function 0; Offset 61h) SNE field to disable SERR for both NMI and LPC.

Status: For the steppings affected, see the Summary Table of Changes.

CHP46. Some RTIT Packets Following PSB May be Sent Out of Order or Dropped

Problem: When a complex micro-architectural condition occurs concurrently with the generation of a RTIT (Real-Time Instruction Trace) PSB (Packet Stream Boundary) packet, the packets that immediately follow the PSB could precede or overwrite some older packets. This erratum applies to no more than 21 packets immediately following the PSB.

Implication: The RTIT packet output immediately following a PSB may not accurately reflect software behavior, and may result in an RTIT decoder error.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP47. System May Hang When DDR Dynamic Self-Refresh is Enabled

Problem: The system may hang when DDR dynamic self-refresh is enabled.

Implication: When this erratum occurs, the system hangs. A cold reset is required to recover the system.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

CHP48. USB3 PHY May Become Unreliable On Certain SoC Parts

Problem: When the system enters S0i3 sleep state, the contents of USB3 PHY configuration registers may change sometimes.

Implication: Due to this erratum, the USB3 device connected to the port may not be detected or the port may downgrade to USB2 speed.

Workaround: It is possible for BIOS to contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

CHP49. System May Experience Inability to Boot or May Cease Operation

Problem: Under certain conditions where activity is high for several years the LPC, RTC and SD Card may stop functioning in the outer years of use.

Implication: LPC and RTC circuitry that stops functioning may cause operation to cease or inability to boot. SD Card that stops functioning may cause SD Cards to be unrecognized. Intel has only observed this behavior in simulation. Designs that implement the LPC interface at the 1.8V signal voltage are not affected by the LPC part of this erratum.

Workaround: Firmware code changes for LPC and RTC circuitry and mitigations for SD Card circuitry have been identified and may be implemented for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

CHP50. xHCI Host Controller Reset May Lead to System Hang

Problem: An access to xHCI configuration space within 1ms of setting the xHCI HCRST (Host Controller Reset) bit of the USB Command Register (xHCIBAR, offset 80h, Bit[1]) or a second setting of the HCRST bit within 120ms may cause the xHCI host controller to fail to respond.

Implication: Due to this erratum, the system may hang.

Workaround: Software must not access xHCI configuration space within 1ms or set HCRST bit within 120ms of setting the HCRST bit.

Status: For the steppings affected, see the Summary Table of Changes.

CHP51. LPC Clock Control Using the LPC_CLKRUN# May Not Behave As Expected

Problem: The LPC_CLKRUN# pin should be an input/open drain output signal as stated for the CLKRUN# signal in Section 2 of the Intel Low Pin Count (LPC) Interface Specification, Revision 1.1. Due to this erratum, if the signal is configured to be an output signal, the buffer may drive an active high level.

Implication: The SoC may prevent a peripheral device from successfully requesting the LPC clock.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.

CHP52. Processor May Not Wake From C6 or Deeper Sleep State

Problem: The processor may not wake after a sleep state entered with MWAIT Target C-State of C6 and Sub C-state of 2 or a target C-state deeper than C6 is requested.

Implication: When this erratum occurs, the system may hang.

Workaround: It is possible for the firmware to contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

CHP53. LPC_AD3 Signal May Not Behave As Expected During Read or Write Cycle Turnaround Periods

Problem: During the turnaround period of a LPC read or write cycle, the processor should first drive LPC_AD[0:3] signals to high (4’b1111) on the first clock cycle and the tristate them on the clock cycle, where their state is maintained by on-processor or on-board pull-up resistors. Due to this erratum, the LPC_AD3 signal may not stay tri-stated during the second clock cycle and may drop to a logical low level instead.

Implication: The LPC device response to this erratum is device-dependent and may lead to a device hang or otherwise exhibit unpredictable behavior.

Workaround: None identified. It is possible for the BIOS to contain a mitigation for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

CHP54. eMMC, SD Card, or SDIO CRC Detection

Problem: The eMMC, SD Card, or SDIO controllers may fail to detect a CRC error if a bit error occurs on the DATA3 signal during read operations when in eMMC High Speed DDR or SD Card/SDIO DDR50 mode. CRC detection on other DATA signals is not impacted.

Implication: The controller will not flag the CRC error to the driver or application, which could result in data integrity issues. Bit errors on eMMC, SD Card, or SDIO DATA signals are not expected on platforms that follow Intel recommended design guidelines and tuning processes.

Workaround: None identified. To mitigate the issue, eMMC High Speed SDR or SD Card/SDIO SDR50 modes can be used instead of High Speed DDR or DDR50.

Status: For the steppings affected, refer the Summary Table of Changes.

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Specification Changes

CHP1. VNN Sx Iccmax Specification Update

Table 5 will be updated with the following data.

Table 5. SoC Power Rail DC Specifications and Maximum Current

Power Rail (SoC)	N3000 (TDP-4W) (SDP-3W) (DC) (S0-Imax)(mA)	N3050 (TDP-6W) (SDP-4W) (DC) (S0-Imax)(mA)	N3700 (TDP-6W) (SDP-4W) (QC) (S0-Imax)(mA)	N3150 (TDP-6W) (SDP-4W) (QC) (S0-Imax)(mA)	S3 Imax (mA)	S4 Imax (mA)	S5 Imax (mA)
VCC0+VCC1 (merged)	3600	3600	7700	7700	0	0	0
VGG	11000	11000	11000	11000	0	0	0
VNN	3500	3500	3500	3500	175	175	175
V1P05A	1900	2000	2000	2000	15	15	15
V1P15S	500	500	500	500	0	0	0
V1P24A	500	500	500	500	5	5	5
V1P5S or V1P8S	20	20	20	20	1	0	0
V1P8A	550	550	550	550	5	5	5
V3P3A_PRIME	200	200	200	200	1	1	1
LPC IO (3.3V)	148	148	148	148	1	1	1
VSDIO (3.3V)	141	141	141	141	1	0	0
VSDIO (1.8V)	93	93	93	93	1	0	0
VDDQ (1.35V)	2400	2400	2400	2400	15	0	0
VCC_RTC	1	1	1	1	1	1	1

Note: VCC_RTC I_{ccmax} in G3 state is 6uA. This current specification is valid at an ambient temperature of 25°C with 3V coin cell battery.

CHP2. Icc_{max} Definition

The following Notes will be added to Table 5.

1. The data in this table only represent peak or worst case conditions and does NOT represent sustained or average current requirements.
2. The data in this table should ONLY be used for power delivery or voltage regulator (VR) design. These numbers should only be used as guidance to enable appropriate power delivery or voltage regulator part selection and should not be used for Battery Life analysis or Power Performance estimation.

CHP3. ICCmax Specification Update for Desktop D1 Stepping SKUs

Below are the updated specifications on TDP, core and gen ICCmax value for Desktop SKUs in D-stepping.

Desktop SKUs	Pentium® J3710	Celeron® J3160	Celeron® J3060
Core / CPU ICCMax	10A[1]	10A[1]	10A[1]
Gen / GFX ICCMax	12A[1]	12A[1]	12A[1]
Thermal Design Power (TDP)	6.5W (+/-10%)	6W (+/-10%)	6W (+/-10%)

Note: New Iccmax value will be backward compatible and support both C and D stepping SoC

DTS accuracy is ±8°C under 60°C and ±5°C above 60°C.

CHP4. Digital Display Interface Update

Doc# 540602 - Braswell Platform Design Guide - Table24-2, Digital Display Interface has been updated to reflect that DDI0, DDI1 and DDI2 of SoC that can be used to connect to DisplayPort (DP)

CHP5. RTC Register Setting Changes

The following register is added to section 33.18 of Datasheet Volume 3. It contains the registers used in the RTC workaround in erratum CHP49.

Access Method

Type: Message Mapped I/O Register **Offset:** [ILB_BASE_ADDRESS] + 74h (Size: 32 bits)

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000003Dh

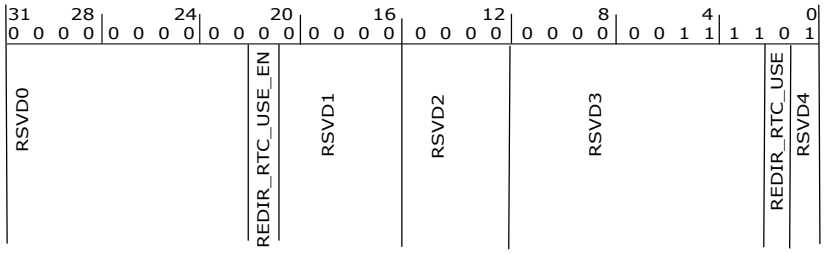


Table 22: Bit Range and Field Name Description

Bit range	Default and Access	Field Name (ID): Description
31:22	0x0 RO	**RSVD0**
21	0x0 RW	**REDIR_RTC_USE_EN:** Redirect RTC Usage Enable: When this bit is set to 0, RTCC[1] can be used to redirect RTC usage to RTC circuits not affected by erratum CHP49
20:16	0x0 RW	**RSVD1**
15:12	0x0 RO	**RSVD2**

11:2	0xF RW	**RSVD3**
1	0x0 RW	**REDIR_RTC_USE:** Redirect RTC Usage: When this bit is set to 1, RTC usage is redirected to RTC circuits not affected by erratum CHP49
0	0x1 RW	**RSVD4**

Specification Clarifications

CHP1. General Power State of the System Update

Table 6 will be updated as follows:

Table 6. General Power States for System

States/Sub-States	Legacy Name/Description	CPU State	Graphics Adapter State
G0/S0/C0	**FULL ON:** Processor operating. Individual devices may be shut down to save power. The different processor operating levels are defined by Cx States.	Full-on	D0
G0/S0/Cx	**Cx State:** Processor manages C-State itself.	C1/C1E: Auto Halt	D0
		C6: Deep Power Down	D3/Display Off
		C7: Deep Power Down	D3/Display Off
G1/S3	**Suspend-To-RAM(STR):** The system context is maintained in system DRAM, but power is shut to non-critical circuits. Memory is retained and refreshes continue. All external clocks are shut off, RTC clock and internal rind oscillator clocks are still toggling.	Off	Display Off
G1/S4	**Suspend-To-Disk (STD):** The context of the system s maintained on the disk. All of the power is shut down except power for the logic to resume. The S4 and S5 states are treated the same.	Off	Display Off
G2/S5	**Sort-Off:** System context is not maintained. All of the power is shut down except power for the logic to restart. A full boot is required when waking. The S4 and S5 states are treated the same.	Off	Display Off
G3	**Mechanical-OFF:** System content is not maintained. All power shutdown except for the RTC. No "wake" events are possible, because the system does not have any power. This state occurs if the user removes the batteries, turns off a mechanical switch, or if the system power supply is at a level that is insufficient to power the "waking" logic. When system power returns, transition will depend on the state just prior to the entry to G3.	Off	Display Off

CHP2. Enabling SoC USB Debug Port

Note: Unlike the previous generation of SoCs, a different process must be followed in order to enable USB debug ports on the SoC. To enable debug port in BSW, please follow these steps:

1. Enable Windbg by "bcdedit/debug"
2. Restart target system
3. Shutdown target system
4. Open Winbg in the host system
5. Connect USB 3.0 debug cable to port between target system and host system
6. Power on target system

7. Host can recognize target as “USB 2.0 Debug Connection Device” in device manager
8. xHCI controller can work in target system
9. Winbg can work between host and target system

Any deviation from this process may not be able to enable the debug ports on the SoC successfully.

CHP3. Digital Thermal Sensor (DTS) Accuracy

DTS accuracy is ±8°C under 60°C and ±5°C above 60°C

§ §

Documentation Changes

Below section provides an update for N-series Intel® Pentium® Processors and Intel® Celeron® Processors Datasheet Volume 1 of 3.

HPET feature is not supported

The HPET feature is not supported and should be removed from the *N-series Intel® Pentium® Processors and Intel® Celeron® Processors Datasheet Volume 1 of 3*, Doc #547869

Memory Space Address Mapping

All addresses in Table 16-30 are offsets from the CFIO memory space base address, also known as, IOBASE. Base addresses for CFIO memory space registers (IOBASE) are located in `D31:F0:0x4C`. Each GPIO Community has 16-bit addressing with a possible address space of 64kb.

Note in Section 16.8 of N- Series Intel® Pentium® Processors and Intel® Celeron® Processors Datasheet

When running the LPC interface at 1.8V (1.8V supplied to ball G1), the interface will not be active until the v1p8Mode register bit is set for the GPIO family, as follows:

```
hshvfamily_3x3_rcomp_9_0_family_config_reg (IOBASE + 0x18000 + 0x1214)
bit 21=1b
```

This expected behavior is due to the way internal buffers are designed.

Information Changes in table 2-17 PCU-LPC Bridge Interface Signals (Sheet 2 of 2)

The Pwrgood Assert State for `LPC_CLK [0]` should be revised as `0 (20K PD)` as shown in the below table.

Signal Name	Dir.	Platform Power	Type	Default Buffer State	
				Pwrgood Assert State	Resetput Deassert State
LPC_CLKRUN_N	I/O	V3P3A/V1P8A	GPIOHV, HS	Input (20K PU)	Input (20K PU)
LPC_CLK [0]	I/O	V3P3A/V1P8A	GPIOHV, HS	0 (20K PD)	Clock
LPC_CLK [1]	I/O	V3P3A/V1P8A	GPIOHV, HS	Input (20K PU)	Input
LPC_RCOMP	I/O	V3P3A/V1P8A	GPIOHV, HS	Z	Z

Information Changes in table 2-27 GPIO Multiplexing and Modes (Sheet 4 of 6)

The Resetout deassert State for `MF_LPC_CLKOUT0` should be revised as Clock, as shown in the table below.

Count	SoC Pin No	CFIO	Default Mode	Default Function	GPIO SoC Power Rail	Pwrgood Assert State	Reset out De-assert State	Optional Mode/ Direction
117	P2	MF_LPC_CLKOUT0	1	LPC_CLKOUT0	V3P3A/V1P8A	0 (20k PD)	Clock	

V_{IH} Definition incorrect in multiple places in the Datasheet

Table 21-34. RTC Well DC Specification

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input High Voltage	2.3	-	-	V	1
V_{IL}	Input Low Voltage	-	-	0.78	V	2

Notes:
1. V_{IH} is defined as the voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the voltage level at a receiving agent that will be interpreted as a logical low value

Section 2.5 GPIO Multiplexing, Table 2-27. GPIO Multiplexing and Modes (Sheet 3 or 6)

Table 2-27. GPIO Multiplexing and Modes (Sheet 3 of 6)
The Optional Modes/ Direction for SoC Pin No. AD52, AH50, AH48 and AH51 need to be revised as follows:

Count	SoC Pin No.	CFIO Name	Default Mode	Default Function	GPIO SoC Power Rail	Pwrgood Assert State	Reset out De-assert State	Optional Modes/ Direction
55	AD52	GPIO_SUS1	1	GPIO_SUS1	V1P8A	Input (20k PD)	Input (20k PD)	Mode6/PCI_WAKE1_N **(PCIE_TX/RX[0])**/1
56	AH50	GPIO_SUS2	1	GPIO_SUS2	V1P8A	Input (20k PU)	Input (20k PU)	Mode6/PCI_WAKE2_N **(PCIE_TX/RX[1])**/1
57	AH48	GPIO_SUS3	1	GPIO_SUS3	V1P8A	Input (20k PD)	Input (20k PD)	Mode6/PCI_WAKE3_N **(PCIE_TX/RX[2])**/1
58	AH51	GPIO_SUS4	1	GPIO_SUS4	V1P8A	Input (20k PU)	Input (20k PU)	Mode6/PCI_WAKE4_N **(PCIE_TX/RX[3])**/1

Note: The PCI_WAKEx_N optional mode signal should be paired with the PCIe lane shown in brackets (PCIE_TX/RX[x])

Section 2.1 Platform Power Rails, Table 2-1. Platform Power Well Definitions

A note to describe LPC Voltage Supply is to be added into Note 1 below, Table 2-1. Platform Power Well Definitions.

Note: The voltage supply for SDIO can be 1.8V or 3.3V. Ball G1 is incorrectly named as SDIO_V3P3A_V1P8A_G3 and actually supplies the LPC power well but also can be 1.8V or 3.3V.

Below section provides an update for N-Series Intel® Pentium® Processors and Intel® Celeron® Processors Datasheet Volume 2 of 3.

Information changes in section 29.2.182 Device Mode Control Reg 0 (DUAL_ROLE_CFG_REG0)-Offset 80D8H

The Field Name (ID): Description for Bit Range 23, EN_PIPE_4_1_SYNC_PHY_STATUS is documented as Reserved. It should be revised as shown in the table below.

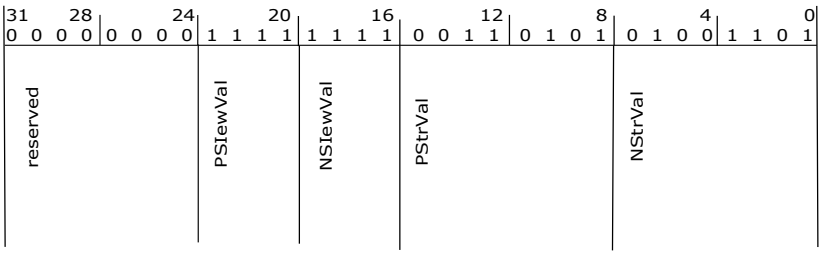
Bit Range	Default & Access	Field Name (ID): Description
23	0x0 RW	EN_PIPE_4_1_SYNC_PHY_STATUS: Reserved. System software/firmware must always set this field to 0x1 before USB x HCI Host Controller Reset is done. Power Well: SUS

Below section provides an update for N-Series Intel® Pentium® Processors and Intel® Celeron® Processors Datasheet Volume 3 of 3.

Additional notes to describe the bit range

This section provides additional notes to describe the bit range of `PSlewVal` and `NSlewVal` in Section 33.7.66 RCOMP Value Register `(hshvfamily_3x3_rcomp_9_0_family_rcomp_value_reg)` - **Offset 120Ch**

RCOMP Value Register
Access Method
Type: Message Bus Register (Size: 32 bits)
Offset: [Port: 0x48] + 120Ch
Op Codes: 06h - Read, 07h - Write
Default: 00FF354Dh



Bit range	Default and Access	Field Name (ID): Description
23:20[1]	0xf RO	P Slew Value (PSlewVal): P Slew values. Valid only after calibration is done.
19:16[2]	0xf RO	N Slew Value (NSlewVal): N Slew Value. Valid only after calibration is done.

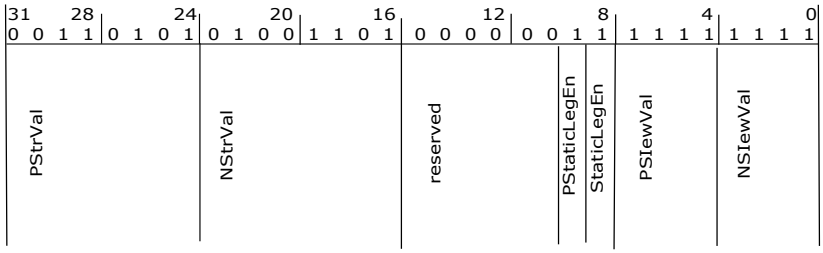
Note: 1. For LPC IO family, bits [23:22] contain the PSIewVal, and bits [21:20] are reserved.

2. For LPC IO family, bits [19:18] contain the NSIewVal and bits [17:16] are reserved.

Additional notes to describe the bit range

This section provides additional notes to describe the bit range of `PSlewVal` and `NSlewVal` in section 33.7.66 Family_config_rcomp_reg `(hshvfamily_3x3_rcomp_9_0_family_rcomp_value_reg)` - **Offset 1210h**

GPIO Family RCOMP Register
Access Method
Type: Message Bus Register (Size: 32 bits)
Offset: [Port: 0x48] + 1210h
Op Codes: 06h - Read, 07h - Write
Default: 354D03FFh



Bit range	Default and Access	Field Name (ID): Description
7:4[1]	0xf RW	P Slew Value (PSlewVal): P Slew values for Pull-up settings.
3:0[2]	0xf RW	N Slew Value (NSlewVal): N Slew Values for Pull-down settings.

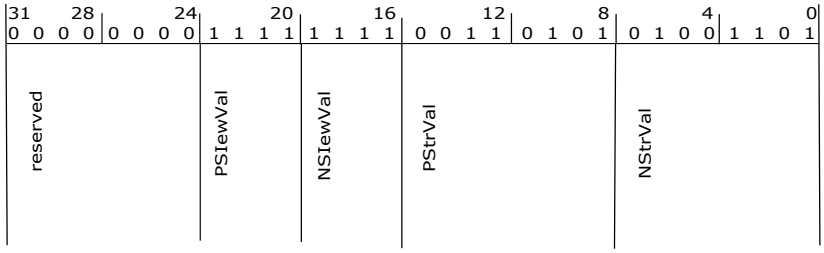
Note: 1. For LPC IO family, bits [5:4] are used to configure the PSIewVal, and bits [7:6] are reserved.

2. For LPC IO family, bits [1:0] are used to configure the NSIewVal and bits [3:2] are reserved.

Additional notes to describe the bit range

This section provides additional notes to describe the bit range of `PSlewVal` and `NSlewVal` in section 33.7.60 RCOMP Value Register `(hshvfamily_3x3_rcomp_7_0_family_rcomp_value_reg)` - **Offset 118Ch**

RCOMP Value Register
Access Method
Type: Message Bus Register (Size: 32 bits)
Offset: [Port: 0x48] + 118Ch
Op Codes: 06h - Read, 07h - Write
Default: 00FF354Dhs



Bit range	Default and Access	Field Name (ID): Description
23:20[1]	0xf RO	P Slew Value (`PSlewVal`): P Slew values. Valid only after calibration is done.
19:16[2]	0xf RO	N Slew Value (`NSlewVal`): N Slew Value. Valid only after calibration is done.

Note: 1. For SD card IO family, bits [23:22] contain the `PSIewVal`, and bits [21:20] are reserved.

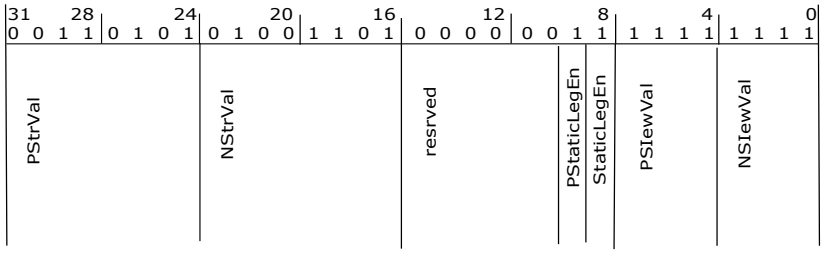
2. For SD card IO family, bits [19:18] contain the `NSIewVal` and bits [17:16] are reserved.

Additional notes to describe the bit range

This section provides additional notes to describe the bit range of `PSlewVal` and `NSlewVal` in section 33.7.61 Family_config_rcomp_reg `(hshvfamily_2x3_rcomp_7_0_family_rcomp_reg)` - **Offset 1190Ch**

GPIO Family RCOMP Register
Access Method
Type: Message Bus Register (Size: 32 bits)
Offset: [Port: 0x48] + 1190Ch
Op Codes: 06h - Read, 07h - Write

Default: 354D03FFh



Bit range	Default and Access	Field Name (ID): Description
7:4[1]	0xf RW	P Slew Value (PSlewVal): Slew values for Pull-up settings.
3:0[2]	0xf RW	N Slew Value (NSlewVal): Slew Values for Pull-down settings.

1. For SD card IO family, bits [5:4] contain the `PSIewVal`, and bits [7:6] are reserved.
2. For SD card IO family, bits [1:0] contain the `NSIewVal` and bits [3:2] are reserved.