Intel® High Definition Audio Specification
Document Change Notification

Date:	March 2, 2012		
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Change Identification:	**DCN No: HDA046-A**
Change Revision:	1.0
Document Revision:	Intel® High Definition Audio 1.0a

Title: Implementation-Specific Settings of the HD Audio Controller Output/Input Payload Capability

Brief description of the functional changes:

The reset values used for the HD Audio Controller Output/Input Payload Capability registers are currently set to fixed values based on the maximum capacity of an HD Audio link. Additional capacity may be specified only in increments of whole HD Audio Links.

There is a need to allow for the optimization of integrated HD Audio solutions where the Controller bandwidth is not limited by the bandwidth of physical HD Audio Links. Integration of the HD Audio Controller and HD Audio Codec in the same ASIC reduces the platform cost related to the adoption of HD Audio and facilitates the upgrade of the hardware for the support of new versions of digital display connection standards like HDMI and DisplayPort.

This DCN proposes to standardize the solution to the stated problems while requiring no change to Controllers or drivers supporting the reset values currently indicated in the HD Audio Specification.

Definition Text Formatting:

xxx	Original text in existing specification or DCN released earlier.
yyy	New text inserted by this new DCN.
~~zzz~~	Deleted text introduced by this new DCN.

New Definitions:

3.3.5 Offset 04h: OUTPAY – Output Payload Capability

Length: 2 bytes

Table 1. Output Payload Capability

Bit	Type	Reset	Description
15:0	RO	~~3Ch~~ Imp.Dep	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit Word quantities per 48-kHz frame. The default link clock speed of 24.000 MHz (the data is double pumped) provides 1000 bits per frame, or 62.5 Words in total. Forty bits (2.5 Words) are used for command and control, leaving 60 Words available for data payload. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. In some non-standard link implementations, the data payload may be other than 60 Words, due to differences in the implementation. Such non-standard link implementations are outside the scope of this specification; however they must maintain compatibility with the concept of 48 kHz periods and the 24 MHz Wall Clock Counter. 00h: 0 Words 01h: 1 Word payload … FFh: 255h Word payload

3.3.6 Offset 06h: INPAY – Input Payload Capability

Length: 2 bytes

Table 2. Input Payload Capability

Bit	Type	Reset	Description
15:0	RO	~~1Dh~~ Imp.Dep	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit Word quantities per 48-kHz frame. The default link clock speed of 24.000 MHz provides 500 bits per frame, or 31.25 Words. 36 bits (2.25 Words) are used for command and control, leaving 29 Words for payload. This measurement is on a per-codec basis. In some non-standard link implementations, the payload may be other than 29 Words, due to differences in the implementation. Such non-standard link implementations are outside the scope of this specification; however they must maintain compatibility with the concept of 48 kHz periods and the 24 MHz Wall Clock Counter. 00h: 0 Words 01h: 1 Word payload … FFh: 255h Word payload