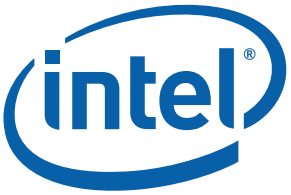
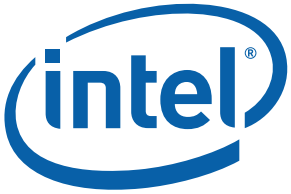


Intel® C600 Series Chipset and Intel® X79 Express Chipset

Specification Update

March 2013

Reference Number: 326515-002



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Contents

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Revision History

Revision	Description	Date
001	• Initial Release.	March 2012
002	• Added Intel® X79 Express chipset. • Updated markings table. • Updated device and revision ID table. • Added errata: — Intel® AMT and Intel® Standard Manageability KT/SOL interrupt status cleared prematurely. — Incorrect IRQ(x) vector returned for 8259 interrupts with RAEOI enabled. — USB RMH false disconnect issue. — Packet loss on Intel® 82579 Gigabit Ethernet controller. — PCI Express* root ports unsupported request completion issue.	March 2013

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Preface

This document is an update to the specifications contained in the Affected Documents/ Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document Number
Intel® C600 Series Chipset and Intel® X79 Express Chipset Datasheet	326514-002

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes that apply to the Intel® C600 Series Chipset and Intel® X79 Express Chipset product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

▌	A change bar to left of a table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Erratum Number	Stepping	Status	Errata
	C1		
1	X	No Fix	USB Isoch In Transfer Error Issue
2	X	No Fix	USB Full-speed/low-speed Device Removal Issue
3	X	No Fix	USB Babble Detected with SW Overscheduling
4	X	No Fix	USB Full-speed/low-speed EOP Issue
5	X	No Fix	USB PLL Control FSM Not Getting Reset on Global Reset
6	X	No Fix	Asynchronous Retries Prioritized Over Periodic Transfers
7	X	No Fix	USB FS/LS Incorrect Number of Retries
8	X	No Fix	Incorrect Data for FS/LS USB Periodic IN Transaction
9	X	No Fix	SATA Signal Voltage Level Violation
10	X	No Fix	SATA Differential Return Loss Violations
11	X	No Fix	High-speed USB 2.0 Transmit Signal Amplitude
12	X	No Fix	Delayed Periodic Traffic Timeout Issue
13	X	No Fix	USB Full-speed/low-speed Port Reset or Clear TT Buffer Request
14	X	No Fix	Intel® 82579 Gigabit Ethernet Controller Transmission Issue
15	X	No Fix	USB RMH Think Time Issue
16	X	No Fix	EVA SMBus controller fails to log completer abort error
17	X	No Fix	Intel® AMT and Intel® Standard Manageability KT/SOL Interrupt Status Cleared Prematurely
18	X	No Fix	Incorrect IRQ(x) Vector Returned for 8259 Interrupts With RAEOI Enabled
19	X	No Fix	USB RMH False Disconnect Issue
20	X	No Fix	Packet Loss on Intel® 82579 Gigabit Ethernet Controller
21	X	No Fix	PCI Express* Root Ports Unsupported Request Completion Issue

Specification Changes

Spec Change Number	Stepping	SPECIFICATION CHANGES
	C1	
		There are no specification changes in this revision of the specification update.

Specification Clarification

No.	Document Revision	SPECIFICATION CLARIFICATIONS
		There are no specification clarifications in this revision of the specification update.

Documentation Changes

No.	Document Revision	DOCUMENTATION CHANGES
		There are no documentation changes in this revision of the specification update.

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Identification Information

Markings

PCH Stepping	S-Spec	Top Marking	MM#	Notes
C1	SLJKG	BD82C602	919598	Intel® C602 Chipset
C1	SLJNG	BD82C602J	920240	Intel® C602J Chipset
C1	SLJKJ	BD82C604	919601	Intel® C604 Chipset
C1	SLJKH	BD82C606	919599	Intel® C606 Chipset
C1	SLJKF	BD82C608	919597	Intel® C608 Chipset
C1	SKJN7	BD82X79	920099	Intel® X79 Chipset

PCH Device and Revision Identification

Device Function	Description	Dev ID	C1 Rev ID	Comments
D31:F0	LPC	0x1D41	06h	All SKUs
D31:F2	SATA[1,2]	0x1D00	06h	Non-AHCI and Non-RAID Mode
		0x1D02	06h	AHCI (Ports 0-5)
		0x1D04	06h	RAID: 0/1/5/10
		0x1D06	06h	Premium RAID: 0/1/5/10 (Server / Workstation Only)
D31:F5	SATA[1,2,3]	0x1D08	06h	Non-AHCI and Non-RAID Mode (Ports 4 and 5)
D31:F3	SMBus	0x1D22	06h	
D31:F6	Thermal	0x1D24	06h	
D22:F0	MEI #1	0x1D3A	06h	
D30:F0	DMI to PCI Bridge	0x1D25h	06h	When D30:F0:4Ch:bit 29 = 1
		0x244Eh	A6h	When D30:F0:4Ch:bit 29 = 0
D29:F0 or D29:F7	USB EHCI #1	0x1D26	06h	
D26:F0 or D26:F7	USB EHCI #2	0x1D2D	06h	
D27:F0	Intel HD Audio	0x1D20	06h	
D28:F0	PCI Express Port 1	0x1D10 or 0x1D11	B6h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 0
		0x244Eh[10]	B6h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 1
D28:F1	PCI Express Port 2	0X1D12 or 0x1D13	B6h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 0
		0x244Eh[10]	B6h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 1
D28:F2	PCI Express Port 3	0X1D14 or 0x1D15	B6h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 0
		0x244Eh[10]	B6h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 1
D28:F3	PCI Express Port 4	0X1D16 or 0x1D17	B6h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 0
		0x244Eh[10]	B6h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 1
D28:F4	PCI Express Port 5	0X1D18 or 0x1D19	B6h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 0
		0x244Eh[10]	B6h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 1
D28:F5	PCI Express Port 6	0X1D1A or 0x1D1B	B6h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 0
		0x244Eh[10]	B6h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 1
D28:F6	PCI Express Port 7	0X1D1C or 0x1D1D	B6h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 0
		0x244Eh[10]	B6h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 1
D28:F7	PCI Express Port 8	0X1D1E or 0x1D1F	B6h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 0
		0x244Eh[10]	B6h	When D28:F0/F1/F2/F3/F4/F5/F6/F7:ECh:bit 1 = 1
D25:F0	LAN[4]	0X1D33	06h	
D22:F0	MEI #1	0x1D3A	06h	

Device Function	Description	Dev ID	C1 Rev ID	Comments
D22:F1	MEI #2	0x1D3B	06h	
D22:F2	IDE-R	0x1D3C	06h	
D22:F3	KT	0x1D3D	06h	
D17:F0	Virtual Root Port[9]	0x1D3E	06h	
Bn[5]:D0:F0	PCIe Upstream Port	0x1D74	06h	C606/C608 SKUs only
Bn+1:D8:F0	Virtual Switch Port	0x1D3F	06h	C606/C608 SKUs only
Bx[5]:D0:F0	SCU0	varies[6]	06h	
Bx:D0:F3	SMB 0	0x1D70	06h	
Bx:D0:F2	SCU1	0x1D61[6]	N/A8	C606/C608 SKUs only
Bx:D0:F4	SMB 1	0x1D71	06h	C606/C608 SKUs only
Bx:D0:F5	SMB 2	0x1D72	06h	C608 SKU only

Port Configuration	Intel® Rapid Storage Technology enterprise (Intel® RSTe) SAS RAID 5	Third Party Device Driver	SCU Device ID (Physical Functions)	SCU Device ID (Virtual Functions)	Hard SKU or Equivalent
4 ports SATA only	SATA RAID 5	No	1D6Bh	1D5Bh	C602
4 ports SATA/SAS	No	No	1D69h	1D59h	C604/C602J
4 ports SATA/SAS	Yes	No	1D65h	1D55h	
8 ports SATA only	SATA RAID 5	No	1D6Ah	1D5Ah	
8 ports SATA/SAS	No	No	1D68h	1D58h	C606
8 ports SATA/SAS	Yes	No	1D64h	1D54h	
8 ports SATA/SAS	Yes	No	1D60h	1D50h	C608
4 ports SATA Only	N/A	Yes	1D6Fh	1D5Fh	
4 ports SATA/SAS	N/A	Yes	1D6Dh	1D5Dh	
8 ports SATA Only	N/A	Yes	1D6Eh	1D5Eh	
8 ports SATA/SAS	N/A	Yes	1D6Ch	1D5Ch	

PCH CRID Table

CRID Select Keys	PCH Stepping	Rev ID	CRID Value	Notes
1Dh	B0	04h	04h	Enable CRID by writing 1Dh to D31:F0:Offset 08h
	C0	05h	05h	
	C1	06h	05h	

The RID register will not retain its value during suspend states. To prevent undesirable enumeration events, the system BIOS must reselect the CRID during resume events from ACPI S3 or S4 states.

Errata

1. USB Isoch In Transfer Error Issue

Problem: If a USB full-speed inbound isochronous transaction with a packet length 190 bytes or greater is started near the end of a microframe the PCH may see more than 189 bytes in the next microframe.

Implication: If the PCH sees more than 189 bytes for a microframe, an error will be sent to software and the isochronous transfer will be lost. If a single data packet is lost, no perceptible impact for the end-user is expected.

Note: Intel has only observed the issue in a synthetic test environment where precise control of packet scheduling is available, and has not observed this failure in its compatibility validation testing.

- Isochronous traffic is periodic and cannot be retried, thus it is considered good practice for software to schedule isochronous transactions to start at the beginning of a microframe. Known software solutions follow this practice.
- To sensitize the system to the issue, additional traffic such as other isochronous transactions or retries of asynchronous transactions would be required to push the inbound isochronous transaction to the end of the microframe.

Workaround: None.

Status: No Plan to Fix.

2. USB Full-speed/low-speed Device Removal Issue

Problem: If two or more USB full-speed/low-speed devices are connected to the same USB controller, the devices are not suspended, and one device is removed, one or more of the devices remaining in the system may be affected by the disconnect.

Implication: The implication is device dependent. A device may experience a delayed transaction, stall, and be recovered via software; or stall and require a reset such as a hot-plug to resume normal functionality.

Workaround: None.

Status: No Plan to Fix.

3. USB Babble Detected with SW Overscheduling

Problem: If software violates USB periodic scheduling rules for full-speed isochronous traffic by overscheduling, the RMH may not handle the error condition properly and return a completion split with more data than the length expected.

Implication: If the RMH returns more data than expected, the endpoint will detect packet babble for that transaction and the packet will be dropped. Since overscheduling occurred to create the error condition, the packet would be dropped regardless of RMH behavior. If a single isochronous data packet is lost, no perceptible impact to the end user is expected.

Note: USB software overscheduling occurs when the amount of data scheduled for a microframe exceeds the maximum budget. This is an error condition that violates the USB periodic scheduling rule.

Note: This failure has only been recreated synthetically with USB software intentionally overscheduling traffic to hit the error condition.

Workaround: None.

Status: No Plan to Fix.

4. USB Full-speed/low-speed EOP Issue

Problem: If the EOP of the last packet in a USB Isochronous split transaction (Transaction >189 bytes) is dropped or delayed 3 ms or longer the following may occur:

- If there are no other pending low-speed or full-speed transactions, the RMH will not send SOF or Keep-Alive. Devices connected to the RMH will interpret this condition as idle and will enter suspend.
- If there is other pending low-speed or full-speed transactions, the RMH will drop the isochronous transaction and resume normal operation.

Problem: If there are no other transactions pending, the RMH is unaware a device entered suspend and may starting sending a transaction without waking the device. The implication is device dependent, but a device may stall and require a reset to resume functionality.

If there are other transactions present, only the initial isochronous transaction may be lost. The loss of a single isochronous transaction may not result in end-user-perceptible impact.

Note: Intel has only observed this failure when using software that does not comply with the USB specification and violates the hardware isochronous scheduling threshold by terminating transactions that are already in progress.

Workaround: None.

Status: No Plan to Fix.

5. USB PLL Control FSM not Getting Reset on Global Reset

Problem: Intel® C600 Series Chipsets USB PLL may not lock if a Global Reset occurs early during a cold boot sequence.

Implication: USB interface would not be functional an additional cold boot would be necessary to recover.

Workaround: None.

Status: No Plan to Fix.

6. Asynchronous Retries Prioritized Over Periodic Transfers

Problem: The integrated USB RMH incorrectly prioritizes full-speed and low-speed asynchronous retries over dispatchable periodic transfers.

Implication: Periodic transfers may be delayed or aborted. If the asynchronous retry latency causes the periodic transfer to be aborted, the impact varies depending on the nature of periodic transfer:

- If a periodic interrupt transfer is aborted, the data may be recovered by the next instance of the interrupt or the data could be dropped.
- If a periodic isochronous transfer is aborted, the data will be dropped. A single dropped periodic transaction should not be noticeable by end-user.

Note: This issue has only been seen in a synthetic environment. The USB spec does not consider the occasional loss of periodic traffic a violation.

Workaround: None.

Status: No Plan to Fix.

7. USB FS/LS Incorrect Number of Retries

Problem: A USB low-speed transaction may be retried more than three times, and a USB full-speed transaction may be retried less than three times if all of the following conditions are met:

- A USB low-speed transaction with errors, or the first retry of the transaction occurs near the end of a microframe, and there is not enough time to complete another retry of the low-speed transaction in the same microframe.
- There is pending USB full-speed traffic and there is enough time left in the microframe to complete one or more attempts of the full-speed transaction.
- Both the low-speed and full-speed transactions must be asynchronous (Bulk/Control) and must have the same direction, either in or out.

Note: Per the USB EHCI Specification a transaction with errors should be attempted a maximum of 3 times if it continues to fail.

Implication: For low-speed transactions the extra retries allow a transaction additional chances to recover regardless of wheter the full-speed transaction has errors or not.

If the full-speed transactions also have errors, the PCH may retry the transaction fewer times than required, stalling the device prematurely. Once stalled, the implication is software dependent, but the device may be reset by software.

Workaround: None.

Status: No Plan to Fix.

8. Incorrect Data for FS/LS USB Periodic IN Transaction

Problem: The Periodic Frame list entry in DRAM for a USB FS or LS Periodic IN transaction may incorrectly get some of its data from a prior Periodic IN transaction that was initiated very late into the preceding microframe.

It is considered good practice for software to schedule Periodic Transactions at the start of a microframe. However, Periodic transactions may occur late into a microframe due to the following cases outlined below:

- Asynchronous transaction starting near the end of the proceeding microframe gets asynchronously retried.

Note: Transactions getting asynchronous retried would only occur for ill-behaved USB device or USB port with a signal integrity issue.

- Or two periodic transactions are scheduled by software to occur in the same microframe and the first needs to push the second Periodic IN transaction to the end of the microframe boundary.

Implication: The implication will be device-, driver-, or OS-specific.

Note: This issue has only been observed in a synthetic test environment.

Workaround: None.

Status: No Plan to Fix.

9. SATA Signal Voltage Level Violation

Problem: SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the SATA transmit signaling voltage levels may exceed the maximum motherboard Tx connector and device Rx connector voltage specifications as defined in section 7.2.1 of the Serial ATA specification, rev 3.0. This issue applies to Gen 1 (1.5 Gbps) and Gen 2 (3.0 Gbps).

Implication: None known.

Workaround: None.

Note: Intel recommends motherboard designers consult the Intel C600 Series Chipsets EDS/ EDS specification update and implement the recommended SATA initialization settings.

Status: No Plan to Fix.

10. SATA Differential Return Loss Violations

Problem: The Intel C600 Series Chipset's SATA buffer capacitance may be higher than expected.

Implication: There are no known functional failures. This may cause a violation of the SATA-IO compliance test for Receiver or Transmitter Differential Return Loss.

Workaround: None.

Note: Intel has obtained a waiver for the SATA-IO building block status.

Status: No Plan to Fix.

11. High-speed USB 2.0 Transmit Signal Amplitude

Problem: Intel C600 Series Chipset's High-speed USB 2.0 transmit signal amplitude may exceed the USB 2.0 specification.

- USB 2.0 Specification Transmit Eye template maximum boundary is ±525 mV following bit transitions and ±475 mV for nontransitional bit patterns.
- USB 2.0 Specification V_{HSOH} maximum is 440 mV.

Implication: There are no known functional failures.

Workaround: None.

- Motherboard designers are recommended to consult the Intel C600 Series Chipsets EDS and ensure they implement USB initialization settings most appropriate for the specific USB port implementation.

Status: No Plan to Fix.

12. Delayed Periodic Traffic Timeout Issue

Problem: If a periodic interrupt transaction is pushed out to the x+4 microframe boundary, the RMH may not wait for the transaction to timeout before starting the next transaction.

Implication: If the next full-speed or low-speed transaction is intended for the same device targeted by the periodic interrupt, the successful completion of that transaction is device dependent and cannot be guaranteed. The implication may differ depending on the nature of the transaction:

- If the transaction is asynchronous and the device does not respond, it will eventually be retried with no impact.
- If the transaction is periodic and the device does not respond, the transfer may be dropped. A single dropped periodic transaction should not be noticeable by the end-user.

Note: This issue has only been seen in a synthetic environment.

Workaround: None.

Status: No Plan to Fix.

13. USB Full-speed/low-speed Port Reset or Clear TT Buffer Request

Problem: One or more full-speed/low-speed USB devices on the same RMH controller may be affected if the devices are not suspended and either (a) software issues a Port Reset *or* (b) software issues a Clear TT Buffer request to a port executing a split full-speed/low-speed Asynchronous Out command.

- The Small window of exposure for full-speed device is around 1.5 microseconds and around 12 microseconds for a low-speed device.

Implication: The affected port may stall or receive stale data for a newly arrived split transfer occurring at the time of the Port Reset or Clear TT Buffer request.

Note: This issue has only been observed in a synthetic test environment.

Workaround: None.

Status: No Plan to Fix.

14. Intel® 82579 Gigabit Ethernet Controller Transmission Issue

Problem: Intel® 82579 Gigabit Ethernet Controller with the Intel C600 Series Chipsets and Intel® Management Engine (Intel® ME) Firmware 7.x 5 MB may stop transmitting during a data transfer.

Implication: Intel 82579 Gigabit Ethernet Controller may stop transmitting packets, the link LED will blink, and a power cycle may be required to resume transmission activity.

Note: This issue has only been observed in a focused test environment where data is constantly transferred over an extended period of time (more than approximately 3 hours).

Workaround: A workaround exists using the combination of the Intel 82579 Gigabit Ethernet Controller LAN Driver releases 16.4 or later, and the Intel ME FW 7.1.14 HF (Hot Fix) 5 MB release or later.

Status: No Plan to Fix.

15. USB RMH Think Time Issue

Problem: The Intel C600 Series Chipset USB RMH Think Time may exceed its declared value in the RMH hub descriptor register of 8 full-speed bit times.

Implication: If the OS USB driver fully subscribes a USB microframe, full-speed/low-speed transactions may exceed the microframe boundary.

Note: No functional failures have been observed.

Workaround: None.

Status: No Plan to Fix.

16. EVA SMBus controller fails to log completer abort error

Problem: The Intel C600 Series Chipset issues a completer abort (CA) for SMBUS MemRd of length greater than 1DW, but does not log the errors in the PCISTS register. All the appropriate PCIe* registers are logged and the correct PCIe* error message is issued.

Implication: This sighting affects only the Intel® C608 chipset. Driver software authors must be aware of the 1DW restriction.

Workaround: None needed. Driver software must abide by the 1DW restriction.

Status: No Plan to Fix.

17. Intel® AMT and Intel® Standard Manageability KT/SOL interrupt status cleared prematurely

Problem: A read of the Intel® AMT and Intel® Standard Manageability enabled SOL KTIIR (KT Interrupt Identification Register) or KTLSR (KT Line Status Register) that occurs simultaneous to the arrival of an SOL Host interrupt event may result in a read of the Interrupt Status (INTSTS) bit 0 returning the status of “No Pending interrupt to Host” despite KTLSR reporting a serviceable event.

Implication: Implication of a missed SOL Host interrupt is software implementation dependent. Subsequent interrupts not aligned to a KTIIR or KTLSR read will clear "0" bit 0 (INTSTS) to indicate a pending interrupt to the Host.

Workaround: Software should not rely on reading only bit 0 (INTSTS) of the KTIIR register and should also poll the KTLSR to determine if an SOL Host interrupt is pending.

Status: No Plan to Fix.

18. Incorrect IRQ(x) Vector Returned for 8259 Interrupts With RAEOI Enabled

Problem: If multiple interrupts are active prior to an interrupt acknowledge cycle with Rotating Automatic End of Interrupt (RAEOI) mode of operation enabled for 8259 interrupts (0 to 7), an incorrect IRQ(x) vector may be returned to the processor.

Implication: Implications of an incorrect IRQ(x) vector being returned to the CPU are SW implementation dependent.

Note: This issue has only been observed in a synthetic test environment.

Workaround: None.

Status: No Plan to Fix.

19. USB RMH False Disconnect Issue

Problem: The PCH may falsely detect a USB High-Speed (HS) device disconnect if all of the following conditions are met:

- The HS Device is connected through the Rate Matching Hub (RMH) of the PCH's EHCI controller.
- The device is resuming from selective suspend or port reset.
- The resume occurs within a narrow time window during the EOP (End of Packet) portion of the SOF (Start of Frame) Packet on the USB bus.

Implication: Following the false disconnect, the HS device will be automatically reenumerated. The system implication will depend on the resume event cause:

- If the resume event is a port reset, a second port reset will be automatically generated and the device reenumerated. No end-user impact is expected.
- If the resume event is a hardware or software initiated resume from selective suspend, the implication will be device and software specific, which may result in anomalous system behavior.

Note: If the HS device is a hub, then all of the devices behind the hub, independent of the device speed, may also be reenumerated.

Workaround: None.

Status: No Plan to Fix.

20. Packet Loss on Intel® 82579 Gigabit Ethernet Controller

Problem: Systems with Intel® C600 Series Chipset and Intel® X79 Express Chipset using the Intel 82579 Gigabit Ethernet Controller may experience packet Loss at 100 Mbps and 1 Gbps speeds when the link between the Intel 82579 Gigabit Ethernet Controller and the PCH Integrated LAN Controller is exiting the Low Power Link (K1) State.

Implication: Implications are application and Internet Protocol dependent.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum. Refer to BIOS Specification Update version 1.3.1 or later.

Status: No Plan to Fix.

21. PCI Express* root ports unsupported request completion issue

Problem: Intel® C600 Series Chipset and Intel® X79 Express Chipset family PCI Express* Root Ports in receipt of a Memory Read TLP may return a Unsupported Request (UR) Completion with an incorrect lower address field if:

- Bus Master Enable is disabled in the PCI Express* Root Port's Command register (PCICMD bit2 =0).
- AT field of the TLP header is nonzero.
- The requested upstream address falls within the memory range claimed by the secondary side of the bridge.
- Requester ID with Bus Number of 0.

Implication: The UR Completion with an incorrect lower address field may be handled as a malformed TLP causing the Requestor to send a ERR_NONFATAL upstream to the root port.

Workaround: None.

Status: No Plan to Fix.

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Specification Changes

There are no specification changes in this revision of the specification update.

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Specification Clarifications

There are no specification clarifications in this revision of the specification update.

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Documentation Changes

There are no documentation changes in this revision of the specification update.

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