

Intel® Atom™ Processor Z2760

Specification Update

November 2013

Revision 003



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Revision History

Revision	Description	Date
001	<ul style="list-style-type: none">Initial release	November 2012
002	<ul style="list-style-type: none">Addition of two new errata, CC24, CC25.	September 2013
003	<ul style="list-style-type: none">Addition of new errata: CC26, CC27	November 2013

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Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents

Document Title	Document Number
Intel® Atom™ Processor Z2760 Datasheet	328104-001

Nomenclature

Errata are design defects or errors in engineering samples. Errata may cause the processor behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping assumes that all errata documented for that stepping are present on all devices.

S-Spec Number is a five-digit code used to identify products. Products are differentiated by their unique characteristics, that is, core speed, L2 cache size, and package type as described in the processor identification information table. Read all notes associated with each S-Spec number.

QDF Number is a four digit code used to distinguish between engineering samples. These samples are used for qualification and early design validation. The functionality of these parts can range from mechanical only to fully functional. This document has a processor identification information table that lists these QDF numbers and the corresponding product details.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.



Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, and so forth).

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Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes, which apply to the listed steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X: Erratum, Specification Change or Clarification that applies to this stepping.

(No mark) or (Blank Box): This erratum is fixed in listed stepping or specification change does not apply to list stepping.

Status

Doc: Document change or update that will be implemented.

Plan Fix: This erratum may be fixed in a future stepping of the product.

Fixed: This erratum has been previously fixed.

No Fix: There are no plans to fix this erratum.

Row

Shaded: This item is either new or modified from the previous version of the document.
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Number	Stepping	Status	Errata Title
	SROWW, SROZ4		
CC1	X	No Fix	GP and Fixed Performance Monitoring Counters With AnyThread Bit Set May Not Accurately Count Only OS or Only USR Events
CC2	X	No Fix	Logical Processor May Stall While Logical Processors on Other Core Perform Split I/O Operations
CC3	X	No Fix	THERMTRIP# Will Not Assert Prior to RESET# De-assertion
CC4	X	No Fix	Synchronous Reset of IA32_MPERF on IA32_APERF Overflow May Not Work
CC5	X	No Fix	EOI Transaction May Not be Sent if Software Enters Core C6 During an Interrupt Service Routine
CC6	X	No Fix	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
CC7	X	No Fix	VID Information in IA32_PERF_STS MSR Bits [7:0] May be Incorrect
CC8	X	No Fix	APIC Timer Can Expire Earlier Than Expected
CC9	X	No Fix	A Write to The USB ASYNCLISTADDR Register Hangs When The USB PHY is in Low-Power Mode
CC10	X	No Fix	PROCHOT_LOG May be Incorrectly Set
CC11	X	No Fix	Interrupt Status Registers For CSI x1 And x4 Ports Reflect The Same Value
CC12	X	No Fix	Pending USB transfers May Not Complete When USB Port Enters Low-Power Mode
CC13	X	No Fix	Soft Reset When SD Clock is Off May Result in Stale Data Reads From SD Card
CC14	X	No Fix	Complex Conditions Associated With Instruction Page Remapping or Self/Cross-Modifying Code Execution May Lead to Unpredictable System Behavior
CC15	X	No Fix	Lowest Priority Arbitration Mechanism May Not Work as Expected



Number	Stepping	Status	Errata Title
	SROWW, SROZ4		
CC16	X	No Fix	The Upper Four Bits of The APIC LDR Are Not Supported
CC17	X	No Fix	No Graphic Device's PCI BAR Covers The UEFI GOP Frame Buffer
CC18	X	No Fix	Back to Back Graphics Read/Write Cycles May Cause Missing Pixels
CC19	X	No Fix	Vertex Attribute Interpolation May Cause up to 3 ULPs of Rounding Errors During Rasterization
CC20	X	No Fix	UART DMA Rx Timeout Interrupt May Not be Generated
CC21	X	No Fix	Thermal Interrupt May Occur on Exit From S0i3
CC22	X	No Fix	USB May Drop Multiple Micro-Frame Packets
CC23	X	No Fix	Clock Modulation Events May Cause Measured Frequency to be Incorrect
CC24	X	No Fix	The Display May Flicker After an MIPI-DSI LP to HS Transition
CC25	X	No Fix	Paging Structure Entry May be Used Before Accessed And Dirty Flags Are Updated
CC26	X	No Fix	HDMI Interface May Sink Excessive Current
CC27	X	No Fix	SD Card Controller Does Not Disable The Clock During Card Power Down

Number	SPECIFICATION CHANGES
	None



Number	SPECIFICATION CLARIFICATIONS
	None

Number	DOCUMENTATION CHANGES
	None

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Identification Information

Intel® Atom™ Processor Z2760 samples on 32-nm process processor signature can be identified by the following register contents:

Table 1. Processor Signature by Using the Programming Interface

Reserved	Extended Family ¹	Extended Model ²	Reserved	Processor Type ³	Family Code ⁴	Model Number ⁵	Stepping ID ⁶
31:28	27:20	19:16	15:13	12	11:8	7:4	3:0
0000	00000000b	0011b	000b	0b	0110b	0101b	0001b

NOTE:

1. The Extended Family bits [27:20] are used in conjunction with the Family Code specified in bits [11:8], to indicate whether the processor belongs to the Intel386™, Intel486™, Pentium®, Pentium® Pro, Pentium® 4, Intel® Core™2, or Intel® Atom™ processor series.
2. The Extended Model bits [19:16] in conjunction with the Model Number specified in bits [7:4] are used to identify the model of the processor within the processor's family.
3. The Processor Type specified in bits [13:12] indicates whether the processor is an original OEM processor, an OverDrive processor, or a Dual processor (capable of being used in a dual processor system).
4. The Family Code corresponds to bits [11:8] of the EDX register after RESET, bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register is accessible through Boundary Scan.
5. The Model Number corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register is accessible through Boundary Scan.
6. The Stepping ID in bits [3:0] indicates the revision number of that model.

When EAX is initialized to a value of 1, the CPUID instruction returns the Extended Family, Extended Model, Type, Family, Model and Stepping value in the EAX register.

Note: The EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.



Table 2. Identification Table for Intel® Atom™ Processor Z2760

Product Stepping	QDF/ S-Spec	Processor Signature	Core Speed			Memory Frequency	Integrated Graphics Core Frequency	H-DID/ H-RID ¹	G-DID/ G-RID ²	I-DID/ I-RID ³
			Burst Frequency Mode (BFM)	High Frequency Mode (HFM)	Low Frequency Mode (LFM)					
Revenue-Tray	SR0WW	00030651h	1800 MHz	1500 MHz	600 MHz	800MT/s	533 MHz	08C0h/05h	08CFh/05h	08D0h/05h
Revenue-T&R	SR0Z4	00030651h	1800 MHz	1500 MHz	600 MHz	800MT/s	533 MHz	08C0h/05h	08CFh/05h	08D0h/05h

NOTE:

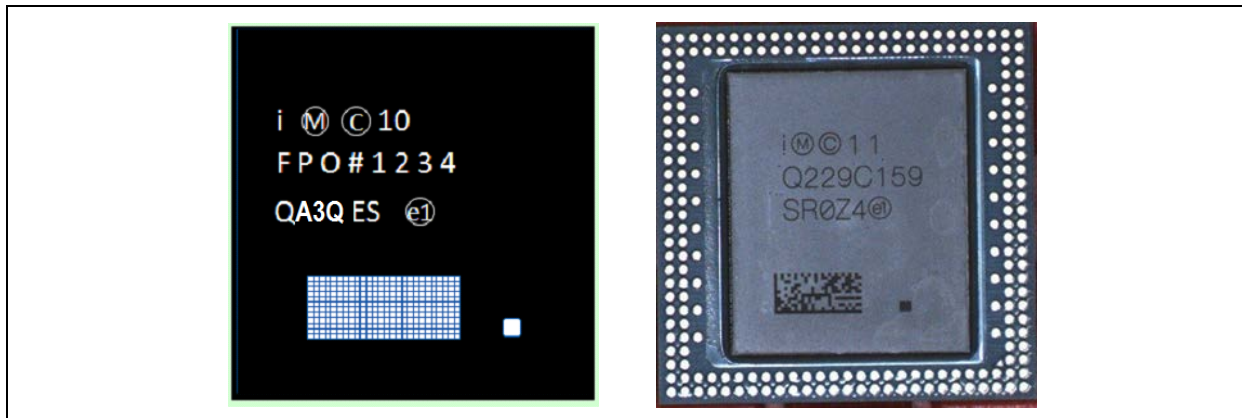
1. H-DID – Host Device ID; H-RID – Host Revision ID (H-RID are last three bits of H-DID)
2. G-DID – Graphics Device ID; G-RID – Graphics Revision ID (G-RID are last three bits of G-DID)
3. I-DID – Imaging Device ID; I-RID – Imaging Revision ID (I-RID are last three bits of I-DID)

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Component Marking Information

Processor shipments can be identified by the following component markings and example pictures.

Figure 1. Intel® Atom™ Processor Z2760 Component Marking Information



NOTE: Package Marking Legend

1. LINE 1 - INTEL TM C '10 (trademark, copyright information, year assy.)
2. LINE 2 - FPO# (Fab Lot number)
3. LINE 3 - e1 (RoHS indicator)
4. BOTTOM -2DID (Barcode information assy. lot code), Pin 1 indicator

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Errata

CC1. GP and Fixed Performance Monitoring Counters With AnyThread Bit Set May Not Accurately Count Only OS or Only USR Events

Problem: A fixed or GP (general purpose) performance counter with the AnyThread bit (IA32_FIXED_CTR_CTRL MSR (38DH) bit [2] for IA32_FIXED_CTR0 bit [6] for IA32_FIXED_CTR1 bit [10] for IA32_FIXED_CTR2; IA32_PERFEVTSEL{0,1} MSR (186H, 187H) bit [21]) set may not count correctly when counting only OS (ring 0) events or only USR (ring >0) events. The counters will count correctly if they are counting both OS and USR events or if the AnyThread bit is clear.

Implication: A performance monitor counter may be incorrect when it is counting for all logical processors on that core and not counting at all privilege levels. This erratum will only occur on processors supporting multiple logical processors per core.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CC2. Logical Processor May Stall While Logical Processors on Other Core Perform Split I/O Operations

Problem: A logical processor may stall as long as two logical processors in another core are doing either I/O instructions which split a 4-byte boundary or memory mapped I/O operations which split an 8-byte boundary. The stalled logical processor will make forward progress when either of the other logical processors stops doing split I/O operations.

Implication: Due to this erratum, a logical processor may stall until two other logical processors in the system stop executing split I/O operations. Intel has not observed this erratum with any commercially available software or system.

Workaround: Software should not continually execute split I/O operations.

Status: For the steppings affected, see the Summary Tables of Changes.

CC3. THERMTRIP# Will Not Assert Prior to RESET# De-assertion

Problem: Potentially catastrophic temperature should be detected and signaled using the THERMTRIP# mechanism after PWRGD assertion. Due to this erratum, THERMTRIP# functionality is not supported during the period from PWRGD assertion to RESET# de-assertion. After RESET# de-assertion, THERMTRIP# functions correctly.

Implication: Due to this erratum, THERMTRIP# will not function until after RESET# de-assertion.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.



CC4. Synchronous Reset of IA32_MPERF on IA32_APERF Overflow May Not Work

Problem: When either the IA32_MPERF or IA32_APERF MSR (E7H, E8H) increments to its maximum value of 0xFFFF_FFFF_FFFF_FFFF, both MSRs are supposed to synchronously reset to 0x0 on the next clock. Due to this erratum, IA32_MPERF may not be reset when IA32_APERF overflows. Instead, IA32_MPERF may continue to increment without being reset.

Implication: Due to this erratum, software cannot rely on synchronous reset of the IA32_MPERF register. The typical usage of IA32_MPERF/IA32_APERF is to initialize them with a value of 0; in this case the overflow of the counter wouldn't happen for over 10 years.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CC5. EOI Transaction May Not be Sent if Software Enters Core C6 During an Interrupt Service Routine

Problem: If core C6 is entered after the start of an interrupt service routine but before a write to the APIC EOI (End of Interrupt) register, and the core is woken up by an event other than a fixed interrupt source the core may drop the EOI transaction the next time APIC EOI register is written and further interrupts from the same or lower priority level will be blocked.

Implication: EOI transactions may be lost and interrupts may be blocked when core C6 is used during interrupt service routines.

Workaround: Software should check the ISR register and if any interrupts are in service only enter C1.

Status: For the steppings affected, see the Summary Tables of Changes.

CC6. Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results

Problem: The act of one processor, or system bus master, writing data into a currently executing code segment of a second processor with the intent of having the second processor execute that data as code is called XMC (cross-modifying code). XMC that does not force the second processor to execute a synchronizing instruction, prior to execution of the new code, is called unsynchronized XMC. Software using unsynchronized XMC to modify the instruction byte stream of a processor can see unexpected or unpredictable execution behavior from the processor that is executing the modified code.

Implication: In this case, the phrase "unexpected or unpredictable execution behavior" encompasses the generation of most of the exceptions listed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide, including a GPF (General Protection Fault) or other unexpected behaviors. In the event that unpredictable execution causes a GPF the application executing the unsynchronized XMC operation would be terminated by the operating system.

Workaround: In order to avoid this erratum, programmers should use the XMC synchronization algorithm as detailed in the [Intel Architecture Software Developer's Manual Volume 3: System Programming Guide](#), Section: Handling Self- and Cross-Modifying Code.



Status: For the steppings affected, see the Summary Tables of Changes.

CC7. VID Information in IA32_PERF_STS MSR Bits [7:0] May be Incorrect

Problem: IA32_PERF_STS MSR (198H) bits [7:0] are supposed to indicate the VID (Voltage ID) after an Enhanced Intel SpeedStep(R) Technology transition. Due to this erratum, one core in a dual core CPU may report incorrect VID values in certain corner cases.

Implication: IA32_PERF_STS MSR bits [7:0] may contain incorrect VID values after certain EIST transitions.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CC8. APIC Timer Can Expire Earlier Than Expected

Problem: Under certain circumstances, the APIC Timer may expire early on the first expiration after the CCR (Current Count Register) of the Local APIC is programmed. If the CCR in the APIC is written when BUS clock frequency is twice as fast as the nominal BUS clock, the first countdown of the APIC Timer may expire n-nominal BUS clocks early, where n can be [1, 2, 4, 8, 16, 32, 64, 128] as determined by the DCR (Divide Configuration Register) in the Local APIC. In the worst case, for a nominal BUS frequency of 100 MHz and a DCR of 128 the APIC Timer can expire 1280 ns early.

Implication: When the CCR is written while BUS clock frequency is twice as fast as the nominal BUS clock the APIC timer may expire early on the first expiration.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CC9. A Write to The USB ASYNCLISTADDR Register Hangs When The USB PHY is in Low-Power Mode

Problem: When USB controller issues a write to the ASYNCLISTADDR (ULPI Sync List Address register), due to this erratum, the write may hang when USB PHY is in low-power mode (ULPI asynchronous mode).

Implication: Intel has not observed this erratum with any commercially available software. USB drivers are not expected to configure when in low-power mode.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CC10. PROCHOT_LOG May be Incorrectly Set

Problem: If the processor core overheats when bidirectional PROCHOT, IA32_THERM_INTERRUPT MSR (19BH) bit 2 are enabled then IA32_THERM_STATUS.PROCHOT_LOG MSR (19CH) bit 3 is incorrectly set.

Implication: Due to this erratum, PROCHOT_LOG may be incorrectly set. Thermal control of the processor is not affected.



Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CC11. Interrupt Status Registers For CSI x1 And x4 Ports Reflect The Same Value

Problem: The Interrupt status register is muxed for both ports.

Implication: Interrupt status registers for CSI x1 and x4 ports reflect the last written value for each port.

Workaround: Only one CSI port is used at a given time, software driver can monitor the CSI ports and clear the interrupt status when there is port switch.

Status: For the steppings affected, see the Summary Tables of Changes.

CC12. Pending USB transfers May Not Complete When USB Port Enters Low-Power Mode

Problem: Pending USB transfers are expected to be completed when run/stop bit is set. Due to this erratum, when USB port is in low-power mode with run/stop bit set pending USB transfers will not be completed.

Implication: Due to this erratum, the system may hang.

Workaround: To avoid this erratum, firmware should delay disabling the clock for the USB PHY until all transfers are completed.

Status: For the steppings affected, see the Summary Tables of Changes.

CC13. Soft Reset When SD Clock is Off May Result in Stale Data Reads From SD Card

Problem: If a soft reset is issued when the SD (Secure Digital) clock is off, the read buffer is not reset. When the SCR (SD Configuration Register) is read, stale data could be read from the buffer even though the card has sent the correct data.

Implication: Due to this erratum, the SD card drive may appear as an invalid file system and files will not be visible.

Workaround: OS driver software should enable SD clock before soft reset is issued.

Status: For the steppings affected, see the Summary Tables of Changes.

CC14. Complex Conditions Associated With Instruction Page Remapping or Self/Cross-Modifying Code Execution May Lead to Unpredictable System Behavior

Problem: Under a complex set of internal conditions, instruction page remapping, or self/cross modifying code events may lead to unpredictable system behavior

Implication: Due to this Erratum, unpredictable system behavior may be observed. Intel has not observed this erratum with any commercially available software.

Workaround: None identified.



Status: For the affected steppings, see the Summary Tables of Changes.

CC15. Lowest Priority Arbitration Mechanism May Not Work as Expected

Problem: Lowest priority arbitration mechanism for selecting the interrupt target may not behave as expected.

Implication: Due to this erratum, selecting an arbitration mechanism other than round robin for lowest priority processor selection may result in lost interrupts.

Workaround: None identified. To avoid this erratum firmware should always select round robin for the lowest priority interrupt arbitration mechanism.

Status: For the steppings affected, see the Summary Tables of Changes.

CC16. The Upper Four Bits of The APIC LDR Are Not Supported

Problem: Only the lower four bits, [3:0], of the APIC's LDR (Logical Destination Register, offset 0D0H) are supported for specifying the logical APIC IDs for all of the logical processors in the system. Programming the upper four bits can result in the interrupts not being delivered or being delivered to the wrong processor.

Implication: Due to this erratum, interrupts may not be delivered to the intended processor.

Workaround: None identified. To avoid this erratum software should never set any of the upper four bits in the LDR.

Status: For the steppings affected, see the Summary Tables of Changes.

CC17. No Graphic Device's PCI BAR Covers The UEFI GOP Frame Buffer

Problem: The UEFI GOP (Graphics Output Protocol) frame buffer is not in a memory range covered by the graphics device's PCI BARs (Base Address Registers).

Implication: Due to this erratum display output may be lost or corrupted when the operating system tries to use the UEFI GOP frame buffer.

Workaround: The operating system must use something other than the PCI BARs to determine the location of the UEFI GOP frame buffer.

Status: For the steppings affected, see the Summary Tables of Changes.

CC18. Back to Back Graphics Read/Write Cycles May Cause Missing Pixels

Problem: Under a complex set of internal conditions, simultaneous occurrence of back to back graphics read/write request to the same internal cache entry, combined with a cache miss and additional memory latency may result in missing pixels.

Implication: Due to this erratum, pixels may be missing on certain frames. Intel has not observed this erratum with any commercially available software.

Workaround: None identified.

Status: For the affected steppings, see the Summary Tables of Changes.



CC19. Vertex Attribute Interpolation May Cause up to 3 ULPs of Rounding Errors During Rasterization

Problem: During rasterization, the vertex attribute interpolation step may cause up to 3 ULPs (Unit(s) of Least Precision) of rounding errors. These rounding errors are propagated to the pixel shader inputs, used to calculate pixel color or depth.

Implication: Due to this erratum, the color and depth of pixel output may be incorrect. Pixel shader code testing inputs for floating point equality or very close bounds may not operate as expected. Intel has not observed this erratum with any commercially available software

Workaround: None identified.

Status: For the affected steppings, see the Summary Tables of Changes.

CC20. UART DMA Rx Timeout Interrupt May Not be Generated

Problem: If the data received by the UART is less than the UART FIFO block size, a DMA timeout interrupt may not be generated.

Implication: Due to this erratum, a DMA interrupt timeout may not be generated.

Workaround: Software may use UART character timeout instead of DMA timeout to detect incomplete packets.

Status: For the steppings affected, see the Summary Tables of Changes.

CC21. Thermal Interrupt May Occur on Exit From S0i3

Problem: DTS (Digital Thermal Sensor state) cannot be restored after S0i3 exit. This can result in spurious thermal interrupts being generated on exit from S0i3.

Implication: Thermal interrupts may occur during exit from S0i3 when temperature is below the enabled thermal thresholds.

Workaround: Thermal management software must recognize and clear spurious interrupts during exit from S0i3.

Status: For the steppings affected, see the Summary Tables of Changes.

CC22. USB May Drop Multiple Micro-Frame Packets

Problem: If multiple high-bandwidth USB devices are attached to the system, the USB subsystem may drop multiple consecutive micro-frame packets.

Implication: Due to this erratum, isochronous devices such as audio or video devices may experience observable artifacts. For example, errant noises (ticks) may be heard on a USB headset when using a high-bandwidth webcam or other high-bandwidth device.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.



CC23. Clock Modulation Events May Cause Measured Frequency to be Incorrect

Problem: During on-demand clock modulation or thermal throttling events, the ACNT/MCNT ratio may appear to show the processor operating at a higher frequency than the actual frequency.

Implication: This erratum may cause the measured frequency to be calculated higher than the actual modulated frequency. There is no effect to the proper functionality of clock modulation.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CC24. The Display May Flicker After an MIPI-DSI LP to HS Transition

Problem: Due to this erratum, when the MIPI (Mobile Industry Processor Interface) display PHY switches from LP (low power) mode to HS (high speed) mode, there is a brief interval (50 ns) where the four MIPI DSI (Display Serial Interface) data lanes may not be synchronized.

Implication: The effects are MIPI Panel dependent. Intel has observed persistent display flicker on some MIPI Panels.

Workaround: Intel® Graphics Media Accelerator driver version 9.14.3.1133 or later contains the workaround for this erratum.

Status: For the steppings affected, see the Summary Tables of Changes.

CC25. Paging Structure Entry May be Used Before Accessed And Dirty Flags Are Updated

Problem: If software modifies a paging structure entry while the processor is using the entry for linear address translation, the processor may erroneously use the old value of the entry to form a translation in a TLB (or an entry in a paging structure cache) and then update the entry's new value to set the accessed flag or dirty flag. This will occur only if both the old and new values of the entry result in valid translations.

Implication: Incorrect behavior may occur with algorithms that atomically check that the accessed flag or the dirty flag of a paging structure entry is clear and modify other parts of that paging structure entry in a manner that results in a different valid translation.

Workaround: Affected algorithms must ensure that appropriate TLB invalidation is done before assuming that future accesses do not use translations based on the old value of the paging structure entry.

Status: For the steppings affected, see the Summary Tables of Changes.



CC26. HDMI Interface May Sink Excessive Current

Problem: If the HDMI Interface is connected to an active HDMI display and the system subsequently goes into S4 or S5 state, the SOC HDMI interface may sink more current from the HDMI device than allowed by the specification in the HDMI-OFF condition.

Implication: This may lead to HDMI compliance Test ID 7-3 "TMDS – Voff" failure.

Workaround: A board level work around is available. Please refer to the latest Platform Design Guidelines for additional details.

Status: For the steppings affected, see the Summary Tables of Changes.

CC27. SD Card Controller Does Not Disable The Clock During Card Power Down

Problem: Due to this erratum, the SD card controller does not automatically disable the SD card clock when the SD card power is disabled.

Implication: : When an SD card is in the system and powered off, the clock to the SD card may continue to be driven causing current leakage through the SD card and may prevent card re-enumeration. This behavior does not comply with the SD Card Specification 2.0.

Workaround: Software must enable and disable the SD card clock in conjunction with SD card power enable and disable.

Status: For the steppings affected, see the Summary Tables of Changes.

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Specification Changes

There are no specification changes in this revision of the Specification Update.

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Specification Clarifications

There are no specification clarifications in this revision of the Specification Update.

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Documentation Changes

There are no documentation changes in this revision of the Specification Update.

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