Intel® Atom™ Processor N2000 and D2000 Series

Specification Update

May 2013

Revision 013
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Intel® Atom™ Processor D2000 and N2000 series may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. Over time processor numbers will increment based on changes in clock, speed, cache, FSB, or other features, and increments are not intended to represent proportional or quantitative increases in any particular feature. Current roadmap processor number progression is not necessarily representative of future roadmaps. See www.intel.com/products/processor_number for details.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Enhanced Intel SpeedStep® Technology: See the Processor Spec Finder at http://processorfinder.intel.com or contact your Intel representative for more information.

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# Revision History

<table>
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<th>Revision</th>
<th>Description</th>
<th>Date</th>
</tr>
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<tbody>
<tr>
<td>001</td>
<td>• Initial Release</td>
<td>September 2011</td>
</tr>
</tbody>
</table>
| 002      | • Updated Figure 1 Marking detail  
• Added errata BQ5 to BQ10 | November 2011 |
| 003      | • Added errata BQ11, BQ12, BQ13 and BQ14 | November 2011 |
| 004      | • Added N2000 series to title, content and Table 2.  
• Added errata BQ15 and BQ16  
• Corrected implication lost in previous version | December 2011 |
| 005      | • Updated Table 2 for new SKU information  
• Updated new errata—BQ17 | January 2012 |
| 006      | • Updated Table 2 for new SKU information  
• Updated new errata—BQ18 and BQ19 | February 2012 |
| 007      | • Updated Table 2 for new SKU information  
• Added new errata—**BQ20** and **BQ21** | March 2012 |
| 008      | • Added new errata BQ22 | May 2012 |
| 009      | • Updated Table 2 for B3 conversion SKU information  
• Updated Summary Table of Changes to add B3 column and change BQ22 status from No Fix to Fixed.  
| 010      | • Included new errata—BQ27 and BQ28 | October 2012 |
| 011      | • Included new errata—BQ29 and BQ30 | December 2012 |
| 012      | • Added new erratum BQ31 | March 2013 |
| 013      | • Updated erratum BQ30 | May 2013 |
Preface

This document contains specification updates for Intel® Atom™ Processor N2000 and D2000 series. It is intended for hardware system manufacturers and software developers.

This document provides:
- Device Errata
- Document Errata
- Specification Clarifications
- Specification Changes

Note: Information types defined in the Nomenclature section of this document are consolidated and are no longer published in other documents.

Affected Documents

<table>
<thead>
<tr>
<th>Document Title</th>
<th>Document Number/Location</th>
</tr>
</thead>
</table>

Related Documents

<table>
<thead>
<tr>
<th>Document Title</th>
<th>Document Number/Location</th>
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<tr>
<td>Intel® 64 and IA-32 Architectures Software Developer’s Manual Documentation Changes</td>
<td>252046</td>
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<tr>
<td>Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1: Basic Architecture</td>
<td>253665</td>
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<tr>
<td>Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B: Instruction Set Reference, N-Z</td>
<td>253667</td>
</tr>
<tr>
<td>Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B: System Programming Guide</td>
<td>253669</td>
</tr>
<tr>
<td>IA-32 Intel® Architectures Optimization Reference Manual</td>
<td>248966</td>
</tr>
<tr>
<td>Intel® Processor Identification and the CPUID Instruction Application Note (AP-485)</td>
<td>241618</td>
</tr>
</tbody>
</table>
**Nomenclature**

**Errata** are design defects or errors. These may cause the processor behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**S-Spec Number** is a five-digit code used to identify products. Products are differentiated by their unique characteristics, for example, core speed, L2 cache size, package type, etc. as described in the processor identification information table. Read all notes associated with each S-Spec number.

**QDF Number** is a four digit code used to distinguish between engineering samples. These samples are used for qualification and early design validation. The functionality of these parts can range from mechanical only to fully functional. This document has a processor identification information table that lists these QDF numbers and the corresponding product details.

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

**Note:** Errata remain in the specification update throughout the product’s lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).
Intel® Atom™ Processor N2000 and D2000 series on 32-nm process stepping can be identified by the following Register contents:

### Table 1: Component Identification via Programming Interface

<table>
<thead>
<tr>
<th>Reserved</th>
<th>Extended Family&lt;sup&gt;1&lt;/sup&gt;</th>
<th>Extended Model&lt;sup&gt;1&lt;/sup&gt;</th>
<th>Reserved</th>
<th>Processor Type&lt;sup&gt;2&lt;/sup&gt;</th>
<th>Family Code&lt;sup&gt;3&lt;/sup&gt;</th>
<th>Model Number&lt;sup&gt;4&lt;/sup&gt;</th>
<th>Stepping ID&lt;sup&gt;5&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000b</td>
<td>0000000b</td>
<td>0011b</td>
<td>000b</td>
<td>0b</td>
<td>0110b</td>
<td>0110b</td>
<td>0000b</td>
</tr>
</tbody>
</table>

### NOTES:

1. The Extended Family, bits [27:20] are used in conjunction with the Family Code, specified in bits [11:8], to indicate whether the processor belongs to the Intel386®, Intel486®, Pentium®, Pentium Pro, Pentium 4, Atom or Intel Core processor family.
2. The Extended Model, bits [19:16] in conjunction with the Model Number, specified in bits [7:4], are used to identify the model of the processor within the processor’s family.
3. The Processor Type, specified in bits [13:12] indicates whether the processor is an original OEM processor, an OverDrive processor, or a dual processor (capable of being used in a dual processor system).
5. The Model Number corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed with 1 in the EAX register, and the model field of the Device ID register, accessible through Boundary Scan.
6. The Stepping ID in bits [3:0] indicates the revision number of that model. See Table 2 for the processor stepping ID number in the CPUID information.

When EAX is initialized to a value of 1, the CPUID instruction returns the Extended Family, Extended Model, Type, Family, Model and Stepping value in the EAX register. Note that the EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.
Component Marking Information

Intel® Atom™ Processor N2000 and D2000 series is identified by the following component markings.

Figure 1: Intel® Atom™ Processor N2000 and D2000 Series (Micro-FCBGA11) Markings

SAMPLE MARKING INFORMATION:
GRP1LINE1: i{M}{C}10Q139C062 SR0DB
GRP2LINE1: {e1}

Table 2: Identification Table for Intel® Atom™ Processor D2000 and N2000 Series

<table>
<thead>
<tr>
<th>QDF / S-Spec</th>
<th>MM#</th>
<th>Product Stepping</th>
<th>Processor #</th>
<th>CPUID</th>
<th>Core Speed</th>
<th>Package</th>
<th>Cache Size (KB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lowest Freq. Mode (LFM)</td>
<td>Highest Freq. Mode (HFM)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>QB0W</td>
<td>916456</td>
<td>B1</td>
<td>D2700</td>
<td>0x30661</td>
<td>2.13 GHz</td>
<td>N/A</td>
<td>Micro-FCBGA11</td>
</tr>
<tr>
<td>QB0X</td>
<td>916457</td>
<td>B2</td>
<td>D2700</td>
<td>0x30661</td>
<td>2.13 GHz</td>
<td>N/A</td>
<td>Micro-FCBGA11</td>
</tr>
<tr>
<td>QB0V</td>
<td>916455</td>
<td>B2</td>
<td>D2500</td>
<td>0x30661</td>
<td>1.86 GHz</td>
<td>N/A</td>
<td>Micro-FCBGA11</td>
</tr>
<tr>
<td>SR0D9</td>
<td>915981</td>
<td>B2</td>
<td>D2700</td>
<td>0x30661</td>
<td>2.13 GHz</td>
<td>N/A</td>
<td>Micro-FCBGA11</td>
</tr>
<tr>
<td>SR0D8</td>
<td>915980</td>
<td>B2</td>
<td>D2500</td>
<td>0x30661</td>
<td>1.86 GHz</td>
<td>N/A</td>
<td>Micro-FCBGA11</td>
</tr>
<tr>
<td>SR0DB</td>
<td>915984</td>
<td>B2</td>
<td>N2600</td>
<td>0x30661</td>
<td>1.6 GHz</td>
<td>600 MHz</td>
<td>Micro-FCBGA11</td>
</tr>
<tr>
<td>QDF / S-Spec</td>
<td>MM#</td>
<td>Product Stepping</td>
<td>Processor #</td>
<td>CPUID</td>
<td>Core Speed</td>
<td>Package</td>
<td>Cache Size (KB)</td>
</tr>
<tr>
<td>-------------</td>
<td>-------</td>
<td>------------------</td>
<td>-------------</td>
<td>---------</td>
<td>------------</td>
<td>-----------</td>
<td>-----------------</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Highest Freq. Mode (HFM)</td>
<td>Lowest Freq. Mode (LFM)</td>
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<tr>
<td>SR0DA</td>
<td>915983</td>
<td>B2</td>
<td>N2800</td>
<td>0x30661</td>
<td>1.86 GHz</td>
<td>800 MHz</td>
<td>Micro-FCBGA11</td>
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<tr>
<td>QC36</td>
<td>920185</td>
<td>B2</td>
<td>D2550</td>
<td>0x30661</td>
<td>1.86 GHz</td>
<td>N/A</td>
<td>Micro-FCBGA11</td>
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<tr>
<td>QC3E</td>
<td>920197</td>
<td>B2</td>
<td>N2850</td>
<td>0x30661</td>
<td>2.0 GHz</td>
<td>800 MHz</td>
<td>Micro-FCBGA11</td>
</tr>
<tr>
<td>QC3C</td>
<td>920194</td>
<td>B2</td>
<td>N2650</td>
<td>0x30661</td>
<td>1.7 GHz</td>
<td>600 MHz</td>
<td>Micro-FCBGA11</td>
</tr>
<tr>
<td>SR0QB</td>
<td>920186</td>
<td>B2</td>
<td>D2550</td>
<td>0x30661</td>
<td>1.86 GHz</td>
<td>N/A</td>
<td>Micro-FCBGA11</td>
</tr>
<tr>
<td>QCYC</td>
<td>922910</td>
<td>B3</td>
<td>N2600</td>
<td>0x30661</td>
<td>1.6 GHz</td>
<td>600 MHz</td>
<td>Micro-FCBGA11</td>
</tr>
<tr>
<td>QCYB</td>
<td>922906</td>
<td>B3</td>
<td>N2800</td>
<td>0x30661</td>
<td>1.86 GHz</td>
<td>800 MHz</td>
<td>Micro-FCBGA11</td>
</tr>
<tr>
<td>QCYA</td>
<td>922892</td>
<td>B3</td>
<td>D2500</td>
<td>0x30661</td>
<td>1.86 GHz</td>
<td>N/A</td>
<td>Micro-FCBGA11</td>
</tr>
<tr>
<td>QCY8</td>
<td>922868</td>
<td>B3</td>
<td>D2550</td>
<td>0x30661</td>
<td>1.86 GHz</td>
<td>N/A</td>
<td>Micro-FCBGA11</td>
</tr>
<tr>
<td>SR0W2</td>
<td>922909</td>
<td>B3</td>
<td>N2600</td>
<td>0x30661</td>
<td>1.6 GHz</td>
<td>600 MHz</td>
<td>Micro-FCBGA11</td>
</tr>
<tr>
<td>SR0W1</td>
<td>922908</td>
<td>B3</td>
<td>N2800</td>
<td>0x30661</td>
<td>1.86 GHz</td>
<td>800 MHz</td>
<td>Micro-FCBGA11</td>
</tr>
<tr>
<td>SROW0</td>
<td>922893</td>
<td>B3</td>
<td>D2500</td>
<td>0x30661</td>
<td>1.86 GHz</td>
<td>N/A</td>
<td>Micro-FCBGA11</td>
</tr>
<tr>
<td>SR0VY</td>
<td>922869</td>
<td>B3</td>
<td>D2550</td>
<td>0x30661</td>
<td>1.86 GHz</td>
<td>N/A</td>
<td>Micro-FCBGA11</td>
</tr>
</tbody>
</table>
**Summary Table of Changes**

The table included in this section indicates the sightings that apply to the Intel® Atom™ Processor N2000 and D2000 series. If a sighting becomes an Erratum, Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations.

### Codes Used in Summary Table

#### Stepping

- **X:** This sighting applies to this stepping.
- **Blank (No mark):** This sighting is fixed, or does not exist, in the listed stepping.

#### Status

- **Doc:** Document change or update will be implemented.
- **Plan Fix:** Root caused to a silicon issue and will be fixed in a future stepping.
- **Fixed:** Root caused to a silicon issue and has been fixed in a subsequent stepping.
- **No Fix:** Root caused to a silicon issue that will not be fixed.
- **Shaded:** This item is either new or modified from the previous version of the document.

**Note:** Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. See [http://www.intel.com/products/processor_number](http://www.intel.com/products/processor_number) for details.
<table>
<thead>
<tr>
<th>Number</th>
<th>Stepping Processor (D2000, N2000 series)</th>
<th>Status</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BQ1</td>
<td>x x x All</td>
<td>No Fix</td>
<td>Intel® HD Audio Buffer Slew Rate Rise Does Not Meet Specification</td>
</tr>
<tr>
<td>BQ2</td>
<td>x x x All</td>
<td>No Fix</td>
<td>PLL Misaligned Clock Sources on Boot May Cause System Hang or Reset</td>
</tr>
<tr>
<td>BQ3</td>
<td>x x x All</td>
<td>No Fix</td>
<td>Extreme Stress on Multiple USB Devices May Cause Unexpected Noise on USB Speaker Device While Connected Behind a Hub</td>
</tr>
<tr>
<td>BQ4</td>
<td>x x x All</td>
<td>No Fix</td>
<td>Sporadic scan line artifacts may be seen while running HD video</td>
</tr>
<tr>
<td>BQ5</td>
<td>x x x All</td>
<td>No Fix</td>
<td>Writes to IA32_DEBUGCTL MSR May Fail when FREEZE_LBRS_ON_PMI is Set</td>
</tr>
<tr>
<td>BQ6</td>
<td>x x x All</td>
<td>No Fix</td>
<td>Synchronous Reset of IA32_MPERF on IA32_APERF Overflow May Not Work</td>
</tr>
<tr>
<td>BQ7</td>
<td>x x x All</td>
<td>No Fix</td>
<td>A Page Fault May Not be Generated When the PS bit is set to “1” in a PML4E or PDPT</td>
</tr>
<tr>
<td>BQ8</td>
<td>x x x All</td>
<td>No Fix</td>
<td>LBR/BTM/BTS Information Immediately After a Transition From Legacy/Compatibility Mode to 64-bit Mode May be Incorrect</td>
</tr>
<tr>
<td>BQ9</td>
<td>x x x All</td>
<td>No Fix</td>
<td>VID Information in IA32_PERF_STS MSR Bits [7:0] May be Incorrect</td>
</tr>
<tr>
<td>BQ10</td>
<td>x x x All</td>
<td>No Fix</td>
<td>GP and Fixed Performance Monitoring Counters With Any Thread Bit Set May Not Accurately Count Only OS or Only USR Events</td>
</tr>
<tr>
<td>BQ11</td>
<td>x x x All</td>
<td>No Fix</td>
<td>C6 Auto-Demotion Does Not Occur as Expected</td>
</tr>
<tr>
<td>BQ12</td>
<td>x x x All</td>
<td>No Fix</td>
<td>APIC Timer Can Expire Earlier Than Expected</td>
</tr>
<tr>
<td>BQ13</td>
<td>x x x All</td>
<td>No Fix</td>
<td>Core C-state Residency MSR Values Are Incorrect</td>
</tr>
<tr>
<td>BQ14</td>
<td>x x x All</td>
<td>No Fix</td>
<td>Local APIC Timer Expiration May Not be Honored if Software Requests Different Deep C-states For Each Logical Processor</td>
</tr>
<tr>
<td>BQ15</td>
<td>x x x All</td>
<td>No Fix</td>
<td>Task-switching IRET May Not Guarantee That All Memory Writes Have Become Globally Visible</td>
</tr>
<tr>
<td>BQ16</td>
<td>x x x All</td>
<td>No Fix</td>
<td>An Indirect Jump Instruction May Execute to An Incorrect Target</td>
</tr>
<tr>
<td>BQ17</td>
<td>x x x All</td>
<td>No Fix</td>
<td>A VM Exit as a Result of a Task-Switching IRET May Not Properly Save the State of NMI Blocking</td>
</tr>
<tr>
<td>BQ18</td>
<td>x x x All</td>
<td>No Fix</td>
<td>680 Ohms Pull Down Resistor for CRT_IREF May Violate VESA Specs</td>
</tr>
<tr>
<td>BQ19</td>
<td>x x x All</td>
<td>No Fix</td>
<td>Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results</td>
</tr>
<tr>
<td>Number</td>
<td>Stepping Processor (D2000, N2000 series)</td>
<td>Status</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>----------------------------------------</td>
<td>--------</td>
<td>-------------</td>
</tr>
<tr>
<td>BQ20</td>
<td>x x x All No Fix</td>
<td>Software Requested or Thermal Based Clock Modulation May Not Result in an Accurate Stop-Clock Duty Cycle</td>
<td></td>
</tr>
<tr>
<td>BQ21</td>
<td>x x x All No Fix</td>
<td>Programming MSR_PKG_CST_CONFIG_CONTROL Package C-state Limit Field to 0x3 May Result in a System Hang</td>
<td></td>
</tr>
<tr>
<td>BQ22</td>
<td>x x All Fixed</td>
<td>Display Corruption May be Observed</td>
<td></td>
</tr>
<tr>
<td>BQ23</td>
<td>x x x All No Fix</td>
<td>The Value Reported For Last C-state May be Incorrect</td>
<td></td>
</tr>
<tr>
<td>BQ24</td>
<td>x x x All No Fix</td>
<td>CS Limit Violations May Not be Detected After VM Entry</td>
<td></td>
</tr>
<tr>
<td>BQ25</td>
<td>x x x All No Fix</td>
<td>Non-BSP Core May Hang When Exiting Processor C-state With DDR Self Refresh Enabled</td>
<td></td>
</tr>
<tr>
<td>BQ26</td>
<td>x x x All No Fix</td>
<td>GFX Throttling above 12.5% May Cause a System Hang</td>
<td></td>
</tr>
<tr>
<td>BQ27</td>
<td>x x x All No Fix</td>
<td>Graphics Unit May Not Thermal Throttle</td>
<td></td>
</tr>
<tr>
<td>BQ28</td>
<td>x x x All No Fix</td>
<td>CPUID Instruction Returns Incorrect Brand String</td>
<td></td>
</tr>
<tr>
<td>BQ29</td>
<td>x x x All No Fix</td>
<td>REP MOVST/STOS Executing With Fast Strings Enabled And Crossing Page Boundaries With Inconsistent Memory Types May Use an Incorrect Data Size or Lead to Memory-Ordering Violations</td>
<td></td>
</tr>
<tr>
<td>BQ30</td>
<td>x x x All No Fix</td>
<td>Complex Conditions Associated With Instruction Page Remapping or Self/Cross-Modifying Code Execution May Lead to Unpredictable System Behavior</td>
<td></td>
</tr>
<tr>
<td>BQ31</td>
<td>x x x All No Fix</td>
<td>Paging Structure Entry May be Used Before Accessed And Dirty Flags Are Updated</td>
<td></td>
</tr>
</tbody>
</table>
Summary Table of Changes

<table>
<thead>
<tr>
<th>Number</th>
<th>SPECIFICATION CHANGES</th>
</tr>
</thead>
<tbody>
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**Errata**

**BQ1  Intel® High Definition Audio (Intel® HD Audio) Buffer Slew Rate Rise Does Not Meet Specification**

**Problem:** Intel HD Audio rising edge slew rate is less than 1-V/ns. This violates the High Definition Audio Specification of being greater than 1-V/ns.

**Implication:** Intel HD Audio will not meet the High Definition Audio specification. This does not impact platform functionality.

**Workaround:** None identified.

**Status:** For the steppings affected, see the Summary Table of Changes.

**BQ2  PLL Misaligned Clock Sources on Boot May Cause System Hang or Reset**

**Problem:** The DMI, DDR3 and processor reference clock may become misaligned due to clock jitter on system startup (cold boot, warm reset or S3 resume) causing unpredictable system behavior including additional resets.

**Implication:** Due to this erratum, excessive clock jitter may cause unpredictable system behavior.

**Workaround:** A CK NET clock chip must be used that meets jitter specification of 85 ps. The processor clocks (HPLL_REFCLK, DMI_REFCLK & DDR3_REF) and Intel® NM10 chipset (DMI_CLK) require clocks that are from the same PLL source.

**Status:** For the steppings affected, see the Summary Table of Changes.

**BQ3  Extreme Stress on Multiple USB Devices May Cause Unexpected Noise on USB Speaker Device While Connected Behind a Hub**

**Problem:** When multiple USB devices are generating heavy traffic and audio is playing through an USB speaker device behind a hub, up to several clicks per minute may be heard on the USB speaker device on back to back I/O accesses. An example of the configuration in which this occurs is USB audio behind a hub with a USB 8MP webcam and 2 USB thumb drives transferring data. Failures were not observed after reducing the USB webcam bandwidth.

**Implication:** Due to the limitations on bus transactions and heavy traffic on back to back I/O accesses, users may hear up to several clicks per minute on USB audio devices.

**Workaround:** None Identified.

**Status:** For the steppings affected, see the Summary Table of Changes.
BQ4  **Sporadic Scan Lines Artifacts May be Seen While Running HD Video**

**Problem:** When the media player software uses the graphics engine for video post processing and the OS provided synchronization between graphics and display engine is not used, occasional scan line artifacts may be seen with certain HD video clips on high resolution displays if media player does not use overlay.

**Implication:** If the media player software uses the graphics engine for video post processing and writes to the same frame buffer that display engine is reading (scanning), partial scan line artifacts may be seen occasionally during certain HD video playback. This does not impact functionality.

**Workaround:**

A. Run media player software in an environment with OS provided sync enabled (using double buffer or buffer chains). An example in the Windows environment is with aero on.

Or

B. Use of overlay interface by the media player software.

**Status:** For the steppings affected, see the Summary Table of Changes.

BQ5  ** Writes to IA32_DEBUGCTL MSR May Fail when FREEZE_LBRS_ON_PMI is Set**

**Problem:** When the FREEZE_LBRS_ON_PMI, IA32_DEBUGCTL MSR (1D9H) bit [11], is set, future writes to IA32_DEBUGCTL MSR may not occur in certain rare corner cases. Writes to this register by software or during certain processor operations are affected.

**Implication:** Under certain circumstances, the IA32_DEBUGCTL MSR value may not be updated properly and will retain the old value. Intel has not observed this erratum with any commercially available software.

**Workaround:** Do not set the FREEZE_LBRS_ON_PMI bit of IA32_DEBUGCTL MSR.

**Status:** For the steppings affected, see the Summary Table of Changes.
BQ6  Synchronous Reset of IA32_MPERF on IA32_APERF Overflow May Not Work

Problem: When either the IA32_MPERF or IA32_APERF MSR (E7H, E8H) increments to its maximum value of 0xFFFF_FFFF_FFFF_FFFF, both MSRs are supposed to synchronously reset to 0x0 on the next clock. Due to this erratum, IA32_MPERF may not be reset when IA32_APERF overflows. Instead, IA32_MPERF may continue to increment without being reset.

Implication: Due to this erratum, software cannot rely on synchronous reset of the IA32_MPERF register. The typical usage of IA32_MPERF/IA32_APERF is to initialize them with a value of 0; in this case the overflow of the counter wouldn’t happen for over 10 years.

Workaround: None Identified.

Status: For the steppings affected, see the Summary Table of Changes.

BQ7  A Page Fault May Not be Generated When the PS bit is set to “1” in a PML4E or PDPTEx

Problem: On processors supporting Intel® 64 architecture, the PS bit (Page Size, bit 7) is reserved in PML4Es and PDPTExs. If the translation of the linear address of a memory access encounters a PML4E or a PDPTEx with PS set to 1, a page fault should occur. Due to this erratum, PS of such an entry is ignored and no page fault will occur due to it being set.

Implication: Software may not operate properly if it relies on the processor to deliver page faults when reserved bits are set in paging-structure entries.

Workaround: Software should not set bit 7 in any PML4E or PDPTEx that has Present Bit (Bit 0) set to “1”.

Status: For the steppings affected, see the Summary Table of Changes.

BQ8  LBR/BTM/BTS Information Immediately after a Transition from Legacy/Compatibility Mode to 64-bit Mode May be Incorrect

Problem: If a transition from legacy/compatibility mode to 64-bit mode occurs and another branch event occurs before the first instruction executes (for example an external interrupt or trap) then any FROM address recorded by LBR (Last Branch Record), BTM (Branch Trace Message) or BTS (Branch Trace Store) on that second event may incorrectly report the upper 32-bits as zero.

Implication: Due to this erratum, bits 63:32 of the ‘FROM’ value for LBR/BTM/BTS may be improperly zeroed after a transition to 64-bit mode when the RIP (Instruction Pointer Register) is greater than 4 Gigabyte.

Workaround: None identified. This erratum may be detected by a ‘FROM’ address having its upper 32-bits zero but its lower 32-bits matching the previous ‘TO’ address recorded.

Status: For the steppings affected, see the Summary Table of Changes.
**BQ9**  
**VID Information in IA32_PERF_STS MSR Bits [7:0] May be Incorrect**

**Problem:**  
IA32_PERF_STS MSR (198H) bits [7:0] are supposed to indicate the VID (Voltage ID) after an EIST (Enhanced Intel SpeedStep® Technology) transition. Due to this erratum, one core in a dual-core CPU may report incorrect VID values in certain corner cases.

**Implication:**  
IA32_PERF_STS MSR bits [7:0] may contain incorrect VID values after certain EIST transitions.

**Workaround:**  
None identified.

**Status:**  
For the steppings affected, see the Summary Table of Changes.

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**BQ10**  
**GP and Fixed Performance Monitoring Counters with Any Thread Bit Set May Not Accurately Count Only OS or Only USR Events**

**Problem:**  
A fixed or GP (general purpose) performance counter with the Any Thread bit (IA32_FIXED_CTR_CTRL MSR (38DH) bit [2] for IA32_FIXED CTR0, bit [6] for IA32 FIXED CTR1, bit [10] for IA32 FIXED CTR2; IA32_PERFEVTSEL0 MSR (186H)/ IA32_PERFEVTSEL1 MSR (187H) bit [21]) set may not count correctly when counting only OS (ring 0) events or only USR (ring >0) events. The counters will count correctly if they are counting both OS and USR events or if the Any Thread bit is clear.

**Implication:**  
A performance monitor counter may be incorrect when it is counting for all logical processors on that core and not counting all privilege levels. This erratum will only occur on processors supporting multiple logical processors per core.

**Workaround:**  
None Identified.

**Status:**  
For the steppings affected, see the Summary Table of Changes.

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**BQ11**  
**C6 Auto-Demotion Does Not Occur as Expected**

**Problem:**  
C6 auto-demotion is enabled by setting PMG_CST_CONFIG_CONTROL MSR (E2H) bit 25 to 1. When enabled, C6 C-state is demoted to a lower C-state if average C6 residency time is low. Due to this erratum auto-demotion will not occur even when this bit is set and the average C6 residency time is low.

**Implication:**  
Due to this erratum the C6 transition may occur more frequently than desired.

**Workaround:**  
The BIOS contains a workaround for this erratum.

**Status:**  
For the steppings affected, see the Summary Table of Changes.
BQ12  APIC Timer Can Expire Earlier Than Expected

Problem: Under certain circumstances, the APIC Timer may expire early on the first expiration after the CCR (Current Count Register) of the Local APIC is programmed. If the CCR in the APIC is written when BUS clock frequency is twice as fast as the nominal BUS clock, the first countdown of the APIC Timer may or may not expire ‘n’ nominal BUS clocks early, where n can be [1, 2, 4, 8, 16, 32, 64, 128] as determined by the DCR ( Divide Configuration Register) in the Local APIC. In the worst case, for a nominal BUS frequency of 100 MHz and a DCR of 128 the APIC Timer can expire, 1280 ns early.

Implication: When CCR is written while BUS clock frequency is twice as fast as the normal BUS clock. The APIC timer may expire early on the first expiration.

Workaround: None Identified.

Status: For the steppings affected, see the Summary Table of Changes.

BQ13  Core C-state Residency MSR Values Are Incorrect

Problem: RDMSR of the core C-state residency MSRs will return a value of zero regardless of the actual residency time. This affects the following MSRs:

- C2_RESIDENCY_TIMER (3F8H)
- C4_RESIDENCY_TIMER (3F9H)
- C6_RESIDENCY_TIMER (3FAH)

Implication: Software cannot determine core C-state residencies by reading these MSRs.

Workaround: The BIOS contains a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

BQ14  Local APIC Timer Expiration May Not be Honored if Software Requests Different Deep C-states For Each Logical Processor

Problem: If one logical processor requests the C6 state and the other logical processor requests the C4 state in close temporal proximity, the local APIC timer expiration event of the logical processor going to C6 may be dropped.

Implication: The platform will wake based only on the local APIC timer of the logical processor going to C4, or can hang if the timer is disabled.

Workaround: The BIOS contains a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.
Errata

BQ15  Task-switching IRET May Not Guarantee That All Memory Writes Have Become Globally Visible

Problem: Serializing instructions ensure that all preceding memory writes have become globally visible before any subsequent load or store instruction. An IRET is a serializing instruction. Due to this erratum, an IRET instruction that performs a task-switch does not guarantee serializing behavior.

Implication: Memory writes may not be observed in the correct order with respect to the task-switching IRET instruction.

Workaround: It is possible for the BIOS to contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

BQ16  An Indirect Jump Instruction May Execute to An Incorrect Target

Problem: An indirect jump instruction may execute incorrectly to the target from a previous instance of the jump instead of the correct target. This may occur only when the indirect jump is part of a short loop.

Implication: Due to this erratum, an indirect jump may cause unpredictable system behavior.

Workaround: It is possible for the BIOS to contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

BQ17  A VM Exit as a Result of a Task-switching IRET May Not Properly Save the Status of NMI Blocking

Problem: A VM exit due to a fault or an EPT violation caused by an IRET instruction should set bit 12 (NMI unblocking due to IRET) of the VM-exit interruption-information field or the exit qualification. This is required if IRET begins execution when either (1) the "NMI exiting" VM-execution control w is 0 and blocking by NMI is in effect; or (2) the "virtual NMI's" VM-execution control w is 1 and virtual-NMI blocking w is in effect. Due to this erratum, such VM exits may clear this bit if the IRET was causing a task switch.

Implication: If a VMM resumes a guest at the IRET instruction after handling such a VM exit, an NMI or a VM exit due to the 1-setting of the "NMI-window exiting", VM-execution control may be delivered prematurely.

Workaround: It is possible for the BIOS to contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

BQ18  680 Ohms Pull Down Resistor for CRT_IREF May Violate VESA Spec

Problem: At maximum luminance, the RGB output may be up to 3% below the "max luminance specification" (0.665V) on some system when using a 680 Ohms IREF resistor.

Implication: Customers may observe lower brightness on a CRT monitor.

Workaround: None identified.

Status: For the steppings affected, see the Summary Table of Changes.
BQ19 **Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results**

**Problem:** The act of one processor, or system bus master, writing data into a currently executing code segment of a second processor with the intent of having the second processor execute that data as code is called cross-modifying (XMC). XMC that does not force the second processor to execute a synchronizing instruction, prior to execution of the new code, is called unsynchronized XMC. Software using unsynchronized XMC to modify the instruction byte stream of a processor can see unexpected or unpredictable execution behavior from the processor that is executing the modified code.

**Implication:** In this case, the phrase “unexpected or unpredictable execution behavior” encompassed the generation of the most of the exception listed in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A: System Programming Guide*, including a General Protection Fault (#GP) or other unexpected behaviors.

**Workaround:** In order to avoid this erratum, programmers should use the XMC synchronization algorithm as detailed in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A: System Programming Guide*, Section: Handling Self- and Cross-Modifying Code.

**Status:** For the steppings affected, see the Summary Table of Changes.

BQ20 **Software Requested or Thermal Based Clock Modulation May Not Result in an Accurate Stop-Clock Duty Cycle**

**Problem:** Clock modulation can be requested either by software through the IA32_CLOCK_MODULATION MSR (19AH) or based on thermal conditions through the TM1 feature enabled (bit 3) in IA32_MISC_ENABLE (1A0H). Both engage internal stop-clock circuitry to create the requested duty cycle. This duty cycle ranges from 12.5% to 87.5%. The actual measured duty cycle may not be accurate if either clock modulation method is enabled.

**Implication:** Software which is sensitive to the accuracy of the requested clock modulation duty cycle may not operate properly.

**Workaround:** It is possible for the BIOS to contain a workaround for this erratum.

**Status:** For the steppings affected, see the Summary Table of Changes.

BQ21 **Programming MSR_PKG_CST_CONFIG_CONTROL Package C-state Limit Field to 0x3 May Result in a System Hang**

**Problem:** When software requests an MWAIT with a target state of 2 or greater and the MSR_PKG_CST_CONFIG_CONTROL MSR (0E2H) Package C-state Limit (bits 2:0) is programmed with a value of 0x3 it is possible for the system to hang.

**Implication:** Due to this erratum, an MWAIT instruction could result in a system hang.

**Workaround:** It is possible for the BIOS to contain a workaround for this erratum.

**Status:** For the steppings affected, see the Summary Table of Changes.

BQ22 **Display Corruption May be Observed**
Errata

Problem: Anomalies in graphics sampler cache may cause the cache to return incorrect data, which may result in unexpected graphics subsystem behavior.

Implication: Due to this erratum visual artifacts, sometimes in form of single horizontal line, or other unexpected graphics subsystem behavior may be observed during normal operation. In some cases, these artifacts may persist across an S3/S4/reboot cycle.

Workaround: The Intel® Graphics Media Accelerator Driver 3600 Series Hot Fix Production Version 8.0.0.3.1075 or later, contains a Workaround for this Erratum.

Status: For the steppings affected, see the Summary Table of Changes.

BQ23 The Value Reported For Last C-state May be Incorrect

Problem: The value of last C-state as reported in the C6C entry bits of 30:27 of PMBA register (70H) may be incorrect.

Implication: Due to this erratum, the value of last C-state may be incorrect.

Workaround: It is possible for the BIOS to contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

BQ24 CS Limit Violations May Not be Detected After VM Entry

Problem: The processor may fail to detect a CS limit violation on fetching the first instruction after VM entry if the first byte of that instruction is outside the CS limit but the last byte of the instruction is inside the limit.

Implication: The processor may erroneously execute an instruction that should have caused a general protection exception.

Workaround: When a VMM emulates a branch instruction, it should inject a general protection exception if the instruction’s target EIP is beyond the CS limit.

Status: For the steppings affected, see the Summary Table of Changes.

BQ25 Non-BSP Core May Hang When Exiting Processor C-state With DDR Self Refresh Enabled

Problem: Exiting processor C-state with DDR Self Refresh enabled may cause non-BSP core to hang.

Implication: Due to this erratum, the non-BSP core may hang while exiting the processor C-state.

Workaround: It is possible for the BIOS to contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Table of Changes.

BQ26 GFX Throttling above 12.5% May Cause a System Hang

Problem: When throttling is set to above 12.5% the graphics processor may hang.
**Implication:** Due to this erratum, the graphics processor may hang, leading to a system hang.

**Workaround:** It is possible for the BIOS to contain a workaround for this erratum. This workaround will limit the GFX throttling to 12.5%.

**Status:** For the steppings affected, see the Summary Table of Changes.

**BQ27 Graphics Unit May Not Thermal Throttle**

**Problem:** At high temperature the graphics unit may fail to thermal throttle.

**Implication:** Due to this erratum, under periods of high temperature the absence of thermal throttling may cause the processor to experience a thermal shut down event.

**Workaround:** It is possible for the BIOS to contain a workaround for this erratum.

**Status:** For the steppings affected, see the Summary Table of Changes.

**BQ28 CPUID Instruction Returns Incorrect Brand String**

**Problem:** When the CPUID instruction is executed with $EAX = 80000002H, 80000003H, or 80000004H$, the returned brand string will be incorrect; it will be missing D2 or N2 prefix.

**Implication:** When this erratum occurs, the processor will report an incorrect model number in the brand string.

**Workaround:** It is possible for the BIOS to contain a workaround for this erratum.

**Status:** For the steppings affected, see the Summary Table of Changes.

**BQ29 REP MOV$S$/STOS Executing With Fast Strings Enabled And Crossing Page Boundaries With Inconsistent Memory Types May Use an Incorrect Data Size or Lead to Memory-Ordering Violations**

**Problem:** Under the conditions described in the Software Developers Manual section "Fast String Operation," the processor performs REP MOV$S$ or REP STOS as fast strings. Due to this erratum, fast string REP MOV$S$/REP STOS instructions that cross page boundaries from WB/WC memory types to UC/WP/WT memory types, may start using an incorrect data size or may observe memory ordering violations.

**Implication:** Upon crossing the page boundary, the following may occur, dependent on the new page memory type:

- **UC:** The data size of each read and write may be different than the original data size.
- **WP:** The data size of each read and write may be different than the original data size and there may be a memory ordering violation.
- **WT:** There may be a memory ordering violation.

**Workaround:** Software should avoid crossing page boundaries from WB or WC memory type to UC, WP or WT memory type within a single REP MOV$S$ or REP STOS instruction that will execute with fast strings enabled.

**Status:** For the steppings affected, see the Summary Table of Changes.
BQ30  Complex Conditions Associated With Instruction Page Remapping or Self/Cross-Modifying Code Execution May Lead to Unpredictable System Behavior

**Problem:** Under a complex set of internal conditions, instruction page remapping, or self/cross modifying code events may lead to unpredictable system behavior.

**Implication:** Due to this Erratum, unpredictable system behavior may be observed.

**Workaround:** None identified.

**Status:** For the steppings affected, see the Summary Table of Changes.

BQ31  Paging Structure Entry May be Used Before Accessed And Dirty Flags Are Updated

**Problem:** If software modifies a paging structure entry while the processor is using the entry for linear address translation, the processor may erroneously use the old value of the entry to form a translation in a TLB (or an entry in a paging structure cache) and then update the entry’s new value to set the accessed flag or dirty flag. This will occur only if both the old and new values of the entry result in valid translations.

**Implication:** Incorrect behavior may occur with algorithms that atomically check that the accessed flag or the dirty flag of a paging structure entry is clear and modify other parts of that paging structure entry in a manner that results in a different valid translation.

**Workaround:** Affected algorithms must ensure that appropriate TLB invalidation is done before assuming that future accesses do not use translations based on the old value of the paging structure entry.

**Status:** For the steppings affected, see the Summary Table of Changes.
There are no specification changes in this revision of the specification update.

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There are no specification clarifications in this revision of the specification update.
Documentation Changes

There are no documentation changes in this revision of the specification update.

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