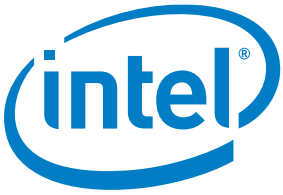


Intel® Celeron® Processor J1800, J1900, N2807, and N2930 for Internet of Things

Specification Update Addendum

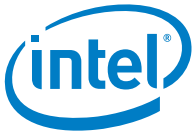
June 2018

Document Number: 335864-002

Contents

Revision History

Date	Revision	Description
May 2018	002	Updated to include Intel® Celeron® J1800 Processor and VLPI2 information
July 2017	001	Initial release.



1.0 Preface

This document is an update to the specifications in the following Affected Documents and Related Documents tables. It is a compilation of device and document errata, and specification clarifications and changes. This document is intended for hardware system manufacturers and software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Note: This document is a supplement to the *Intel® Celeron® and Pentium® Processor N – and J – Series Specification Update*. The document contains specification updates unique to the implementation and operation of the Intel® Celeron® processors J1800, J1900, N2807, and N2930 in Internet of Things platforms.

1.1 Affected Documents

Document Title	Document Number/Location
Intel® Pentium® Processor N3500-series, J2850, J2900, and Intel® Celeron® Processor N2900-series, N2800-series, J1800-series, J1900, J1750 Datasheet	329670

1.2 Related Documents

Document Title	Document Number/Location
Intel® Celeron® and Pentium® Processor N – and J – Series Specification Update	329671

1.3 Nomenclature

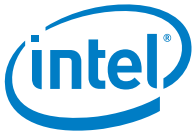
Errata are design defects or errors. Errata may cause the processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).



2.0 Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed processor steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

2.1 Codes Used in Summary Table

2.2 Stepping

X:	Erratum, Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to list stepping.

2.3 Status

Doc:	Document change or update that will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

2.4 Row

Shaded:	This item is either new or modified from the previous version of the document.

3.0 Errata Summary

Table 1. Errata Summary

Number	Status	Steppings				ERRATA
		B2	B3	C0	D1	
VLPI11	Fixed	X	X	X	-	System May Experience Inability to Boot or May Cease Operation
VLPI2	Fixed	X	X	X	-	Reset Sequence May Not Complete Under Certain Conditions

NOTE:

1. This erratum is not relevant to Intel® Celeron® Processor J1800 since it is not supported for use in embedded use conditions

3.1 SPECIFICATION CHANGES

Number	SPECIFICATION CHANGES
	There are no Specification Changes in this Specification Update revision.

3.2 SPECIFICATION CLARIFICATIONS

Number	SPECIFICATION CLARIFICATIONS
	There are no Specification Clarifications in this Specification Update revision.

3.3 DOCUMENTATION CHANGES

Number	DOCUMENTATION CHANGES
	There are no Documentation Changes in this Specification Update revision.

4.0 Identification Information

4.1 Component Identification via Programming Interface

The Intel® Celeron® processor J1800, J1900, N2807, and N2930 steppings can be identified by the following register contents:

Table 2. Component Identification via Programming Interface

Reserved	Extended Family	Extended Model	Reserved	Processor Type	Family Code	Model Number	Stepping ID
31:28	27:20	19:16	15:13	12	11:8	7:4	3:0
0000b	0000000b	0011b	000b	0b	0110b	0111b	B3: 0011b C0: 0100b D1:1001b

NOTES:

1. The Extended Family, bits [27:20] are used in conjunction with the Family Code, specified in bits [11:8], to indicate whether the processor belongs to the Intel386™, Intel486™, Pentium®, Pentium® Pro, Pentium® 4, or Intel® Core™ processor family.
2. The Extended Model, bits [19:16] in conjunction with the Model Number, specified in bits [7:4], are used to identify the model of the processor within the processor's family.
3. The Processor Type, specified in bits [13:12] indicates whether the processor is an original OEM processor, an OverDrive processor, or a dual processor (capable of being used in a dual processor system).
4. The Family Code corresponds to bits [11:8] of the EDX register after RESET, bits [11:8] of the EAX register after the CPUID instruction is executed with 1 in the EAX register, and the generation field of the Device ID register, accessible through Boundary Scan.
5. The Model Number corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed with 1 in the EAX register, and the model field of the Device ID register, accessible through Boundary Scan.
6. The Stepping ID in bits [3:0] indicates the revision number of that model. See Table 3 for the processor stepping ID number in the CPUID information.

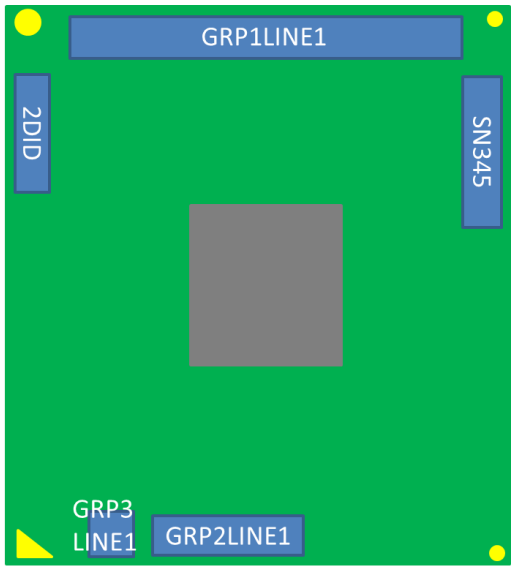
When EAX is initialized to a value of 1, the CPUID instruction returns the Extended Family, Extended Model, Type, Family, Model, and Stepping value in the EAX register.

Note: The EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

4.2 Component Marking Information

The Intel® Celeron® processor J1800, J1900, N2807, and N2930 are identified by the following component markings:

Figure 1. Intel® Celeron® Processor (Micro-FPBGA13 Package) Markings

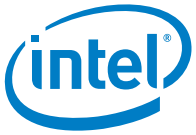


SAMPLE MARKING INFORMATION:
GRP1LINE1: i{M}{C}YY_FPO12345
GRP2LINE1: QDF / SSPEC
GRP3LINE1: {e1}

Table 3. Identification Table for Intel® Celeron® Processor J1800, J1900, N2807, and N2930

QDF / S-Spec	MM#	Product Stepping	Processor #	CPUID	Core Speed		Package	Cache Size (KB)
					Highest Freq. Mode (HFM)/ Burst GHz	Lowest Freq. Mode (LFM) MHz		
SR1SC	932481	B3	J1900	30673	2.00/2.42 (B)	1333	Micro-FCBGA13	2 x1024
SR1UT	934010	C0	J1900	30678	2.00/2.42 (B)	1333	Micro-FCBGA13	2 x1024
SR1W3	934896	C0	N2930	30678	1.83/2.17 (B)	1333	Micro-FCBGA13	2 x1024
SR1W5	934898	C0	N2807	30678	1.58/2.17 (B)	1333	Micro-FCBGA13	1 x1024

NOTE: 'B' is the Intel® Burst Technology x.x (x.x is a placeholder for future versions) feature that is included in the Refresh SKU.



5.0 Errata

5.1 VLPI1. System May Experience Inability to Boot or May Cease Operation

Problem: Under certain conditions where activity is high for several years the LPC, USB (low speed and full speed) and SD Card circuitry may stop functioning in the outer years of use.

Implication: LPC circuitry that stops functioning may cause operation to cease or inability to boot. SD Card or USB circuitry that stops functioning may cause SD Cards to be unrecognized or Low Speed or Full Speed USB devices to not function. Intel has only observed this behavior in simulation. Designs that implement the LPC interface at the 1.8V signal voltage are not affected by the LPC part of this erratum.

Workaround: Firmware code changes for LPC circuitry and mitigations for SD Card & USB circuitry have been identified and may be implemented for this erratum.

Status: For the steppings affected, see the *Summary Tables of Changes*.

5.2 VLPI2. Reset Sequence may Not Complete Under Certain Conditions

Problem: Under certain conditions, the SoC may not complete initalization either during a reset issued while the system is running, or from the G3 (mechanical off) global system state.

Implication: When this erratum occurs, the SoC will detect an initialization problem and halt the initalization sequence prior to normal operation, leading to a system hang. The system will subsequently require a power cycle via the system power button.

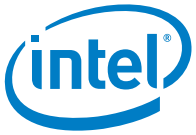
Workaround: For the erratum occurring during reset, while the system is running, a firmware code change has been identified. This change significantly reduces the likelihood of this initalization erratum after initial reset, at power on.

In the rare situation of this sighting occourring, the end user is expected to execute a global reset by performing a Power Button Overrride (press and hold the power button for approximetly 4 seconds.

Status: For the steppings affected, see the Summary Tables of Changes.

6.0 Specification Changes

There are no Specification Changes in this Specification Update revision.



7.0 Specification Clarifications

There are no specification clarifications in this Specification Update revision.

8.0 Documentation Changes

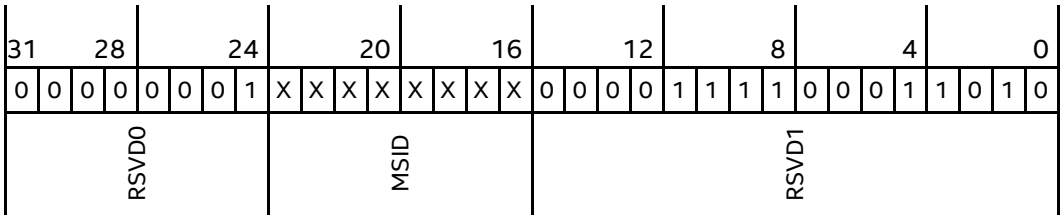
The following register is an addition to section 32.12 of the Datasheet that implements an incremental method for software to differentiate between processor steppings.

Manufacturer ID (PCIE_REG_MANUFACTURER_ID) - Offset F8h

Access Method

Type: PCI Configuration Register **PCIE_REG_MANUFACTURER_ID**: [B:0, D:31, F:0] + F8h (Size 32 bits)

Default: 01xx0F1Ah



Bit Range	Default & Access	Field Name (ID): Description
31:24	01h RO	RSVD0: Reserved
23:16	xxh RO	Manufacturing Stepping ID (MSID): This value of this filed depends on the stepping of the processor — B2: 0Ah — B3: 0Ch — C0: 0Eh — D1: 13h
15:0	0F1Ah RO	RSVD1: Reserved