



# Intel<sup>®</sup> Core<sup>™</sup> X-Series Processor Family

**Specification Update**

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*May 2017*

*Revision 001*



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# Revision History

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Version	Description	Date
001	Initial release.	May 2017

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# Preface

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This document is an update to the specifications contained in the [Affected Documents](#) table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in [Nomenclature](#) are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

## Affected Documents

Document Title	Document Number/Location
Intel® Core™ X-Processor Family Datasheet Volume 1 of 2	335899
Intel® Core™ X-Processor Family Datasheet Volume 2 of 2	335900

## Related Documents

Document Title	Document Number/Location
Intel® 64 and IA-32 Architecture Software Developer's Manual <ul style="list-style-type: none"><li>• Volume 1: Basic Architecture</li><li>• Volume 2A: Instruction Set Reference Manual A-M</li><li>• Volume 2B: Instruction Set Reference Manual N-Z</li><li>• Volume 3A: System Programming Guide</li><li>• Volume 3B: System Programming Guide</li><li>• A-32 Intel® Architecture Optimization Reference Manual</li></ul>	<a href="http://www.intel.com/products/processor/manuals/index.htm">http://www.intel.com/products/processor/manuals/index.htm</a>



## Nomenclature

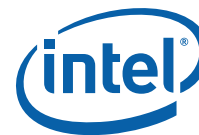
**Errata** are design defects or errors. These may cause the processor behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

**Note:** Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, and so forth).



# Identification Information

## Component Identification via Programming Interface

The processor Stepping can be identified by the following register contents:

Reserved	Extended Family <sup>1</sup>	Extended Model <sup>2</sup>	Reserved	Processor Type <sup>3</sup>	Family Code <sup>4</sup>	Model Number <sup>5</sup>	Stepping ID <sup>6</sup>
31:28	27:20	19:16	15:13	12	11:8	7:4	3:0
	00000000b	0101b		0b	0110b	0101b	varies per stepping

**Notes:**

1. The Extended Family, Bits [27:20] are used in conjunction with the Family Code, specified in Bits [11:8], to indicate whether the processor belongs to the Intel386™, Intel486™, Pentium®, Pentium 4, or Intel® Core™ processor family.
2. The Extended Model, Bits [19:16] in conjunction with the Model Number, specified in Bits [7:4], are used to identify the model of the processor within the processor's family.
3. The Family Code corresponds to Bits [11:8] of the EDX register after RESET, Bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
4. The Model Number corresponds to Bits [7:4] of the EDX register after RESET, Bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
5. The Stepping ID in Bits [3:0] indicates the revision number of that model.

When EAX is initialized to a value of '1', the CPUID instruction returns the *Extended Family, Extended Model, Processor Type, Family Code, Model Number and Stepping ID* value in the EAX register. Note that the EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX and EDX registers after the CPUID instruction is executed with a 2 in the EAX register.



# Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the Product Name product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

## Codes Used in Summary Tables

### Stepping

- X: Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
- (No mark)  
or (Blank box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

### Page

- (Page): Page location of item in this document.

### Status

- Doc: Document change or update will be implemented.
- Plan Fix: This erratum may be fixed in a future stepping of the product.
- Fixed: This erratum has been previously fixed.
- No Fix: There are no plans to fix this erratum.

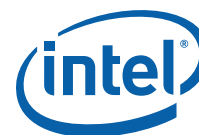
### Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

**Table 1. Errata Summary Table (Sheet 1 of 2)**

Number	Steppings	Status	ERRATA
	U-0		
SKZ1	X	No Fix	A CAP Error While Entering Package C6 May Cause DRAM to Fail to Enter Self-Refresh
SKZ2	X	No Fix	PCIe* Lane Error Status Register May Log False Correctable Error
SKZ3	X	No Fix	In Memory Mirror Mode, DataErrorChunk Field May be Incorrect
SKZ4	X	No Fix	Intel® RDT MBM Does Not Accurately Track Write Bandwidth
SKZ5	X	No Fix	Intel UPI Initialization Aborts May be Logged
SKZ6	X	No Fix	PCIe* Port May Incorrectly Log Malformed_TLP Error
SKZ7	X	No Fix	Short Loops Which Use AH/BH/CH/DH Registers May Cause Unpredictable System Behavior
SKZ8	X	No Fix	Credits Not Returned For PCIe* Packets That Fail ECRC Check
SKZ9	X	No Fix	Link Training Error Due to Single Polarity of a PCIe* Differential Data Pair Being Disconnected
SKZ10	X	No Fix	UPI CRC32 Rolling Mode is Not Functional





**Table 1. Errata Summary Table (Sheet 2 of 2)**

Number	Steppings	Status	ERRATA
	U-0		
SKZ11	X	No Fix	IODC Entry 0 Cannot be Masked
SKZ12	X	No Fix	With eMCA2 Enabled a 3-Strike May Cause an Unnecessary CATERR# Instead of Only MSMI
SKZ13	X	No Fix	CMCI May Not be Signalled for Corrected Error
SKZ14	X	No Fix	A UPI Phy Reset And Rx CRC Error on The Same Packet May Cause Link Layer LLRSM Aborts
SKZ15	X	No Fix	CSRs SVID And SDID Are Not Implemented For Some DDRIO And PCU devices
SKZ16	X	No Fix	Register Broadcast Read From DDRIO May Return a Zero Value
SKZ17	X	No Fix	Intel® CMT Counters May Not Count Accurately
SKZ18	X	No Fix	Intel® CAT May Not Restrict Cacheline Allocation Under Certain Conditions
SKZ19	X	No Fix	Intel® MBM Counters May Undercount
SKZ20	X	No Fix	Intel® PCIe* Corrected Error Threshold Does Not Consider Overflow Count When Incrementing Error Counter
SKZ21	X	No Fix	IIO RAS VPP Hangs During The Warm Reset Test

## Specification Changes

Number	SPECIFICATION CHANGES
	None for this revision of this specification update.

## Specification Clarifications

No.	SPECIFICATION CLARIFICATIONS
	None for this revision of this specification update.

## Documentation Changes

No.	DOCUMENTATION CHANGES
	None for this revision of this specification update.



# Errata

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## **SKZ1 A CAP Error While Entering Package C6 May Cause DRAM to Fail to Enter Self-Refresh**

**Problem:** A CAP (Command/Address Parity) error that occurs on the command to direct DRAM to enter self-refresh may cause the DRAM to fail to enter self-refresh although the processor enters-Package-C6.

**Implication:** Due to this erratum, DRAM may fail to be refreshed, which may result in uncorrected errors being reported from the DRAM.

**Workaround:** None Identified.

**Status:** For the Steppings affected, see the *Summary Tables of Changes*.

## **SKZ2 PCIe\* Lane Error Status Register May Log False Correctable Error**

**Problem:** Due to this erratum, PCIe\* LNERRSTS (Device 0; Function 0; Offset 258h; bits [3:0]) may log false lane-based correctable errors.

**Implication:** Diagnostics cannot reliably use LNERRSTS to report correctable errors.

**Workaround:** None Identified

**Status:** For the Steppings affected, see the *Summary Tables of Changes*.

## **SKZ3 In Memory Mirror Mode, DataErrorChunk Field May be Incorrect**

**Problem:** In Memory Mirror Mode, DataErrorChunk bits (IA32\_MC7\_MISC register MSR(41FH) bits [61:60]) may not correctly report the chunk containing an error.

**Implication:** Due to this erratum, this field is not accurate when Memory Mirror Mode is enabled.

**Workaround:** None Identified.

**Status:** For the Steppings affected, see the *Summary Tables of Changes*.

## **SKZ4 Intel® RDT MBM Does Not Accurately Track Write Bandwidth**

**Problem:** Intel® RDT (Resource Director Technology) MBM (Memory Bandwidth Monitoring) does not count cacheable write-back traffic to local memory. This will result in the RDT MBM feature under counting total bandwidth consumed.

**Implication:** Applications using this feature may report incorrect memory bandwidth.

**Workaround:** None Identified.

**Status:** For the Steppings affected, see the *Summary Tables of Changes*.

## **SKZ5 Intel UPI Initialization Aborts May be Logged**

**Problem:** If Intel® UPI (Ultra Path Interconnect) is configured for slow mode operation, initialization aborts may occur.

**Implication:** Unexpected Initialization aborts may be logged in the ktireut\_ph\_ctr1 register (Bus: 3; Device: 16-14; Function 1; Offset 12h; Bit 4).

**Workaround:** None Identified.

**Status:** For the Steppings affected, see the *Summary Tables of Changes*.

## **SKZ6 PCIe\* Port May Incorrectly Log Malformed\_TLP Error**

**Problem:** If the PCIe port receives a TLP that triggers both a Malformed\_TLP error and an ECRC\_TLP error, the processor should only log an ECRC\_TLP error. However, the processor logs both errors.

**Implication:** Due to this erratum, the processor may incorrectly log Malformed\_TLP errors.

**Workaround:** None Identified



Status: For the Steppings affected, see the *Summary Tables of Changes*.

### **SKZ7 Short Loops Which Use AH/BH/CH/DH Registers May Cause Unpredictable System Behavior**

**Problem:** Under complex micro-architectural conditions, short loops of less than 64 instructions that use AH, BH, CH or DH registers as well as their corresponding wider register (e.g. RAX, EAX or AX for AH) may cause unpredictable system behavior. This can only happen when both logical processors on the same physical processor are active.

**Implication:** Due to this erratum, the system may experience unpredictable system behavior

**Workaround:** It is possible for the BIOS to contain a workaround for this erratum.

Status: For the Steppings affected, see the *Summary Tables of Changes*.

### **SKZ8 Credits Not Returned For PCIe\* Packets That Fail ECRC Check**

**Problem:** The processor's IIO does not return credits back to the PCIe\* link in case of end-to-end CRC (ECRC) errors.

**Implication:** Due to this erratum, the link may experience degraded performance or may eventually fail due to a loss of credits.

**Workaround:** For processors that support LER (Live Error Recovery) the link would be reset and credits would be restored. Processors that do not support LER should configure ECRC errors to be fatal.

Status: For the Steppings affected, see the *Summary Tables of Changes*.

### **SKZ9 Link Training Error Due to Single Polarity of a PCIe\* Differential Data Pair Being Disconnected**

**Problem:** A PCIe Port may not reach L0 state if a single polarity of a PCIe\* differential data pair is disconnected.

**Implication:** Due to this erratum, the Port will not downlink and be able to train up to L0.

**Workaround:** None Identified.

Status: For the Steppings affected, see the *Summary Tables of Changes*.

### **SKZ10 UPI CRC32 Rolling Mode is Not Functional**

**Problem:** With UPI CRC32 Rolling Mode enabled, UPI Rx CRC errors may be seen.

**Implication:** Due to this erratum, when UPI CRC32 Rolling Mode is enabled, UPI Rx CRC errors may be seen.

**Workaround:** None. Do not enable UPI CRC32 setting in BIOS.

Status: For the Steppings affected, see the *Summary Tables of Changes*.

### **SKZ11 IODC Entry 0 Cannot be Masked**

**Problem:** The Individual IODC (IO Directory Cache) Entry 0 cannot be masked using HA\_COH\_CFG\_1, (Bus 1; Devices 11-8; Functions 7-0, Offset 0x11C, bit 0) therefore entry 0 is always allocated.

**Implication:** No functional implications.

**Workaround:** None.

Status: For the Steppings affected, see the *Summary Tables of Changes*.

### **SKZ12 With eMCA2 Enabled a 3-Strike May Cause an Unnecessary CATERR# Instead of Only MSMI**

**Problem:** When eMCA2 is enabled to cause an MSMI due to a 3-strike event, a pulsed CATERR# and MSMI# event may both be observed on the pins.

**Implication:** When this erratum occurs, an unnecessary CATERR# pulse may be observed.

**Workaround:** None.



Status: For the Steppings affected, see the *Summary Tables of Changes*.

### **SKZ13 CMCI May Not be Signalled for Corrected Error**

Problem: Machine check banks 9, 10, and 11 may not signal CMCI after the first corrected error is reported in the bank even if the MCI\_STATUS register has been cleared.

Implication: After the first corrected error is reported in one of the affected machine check banks, subsequent errors will be logged but may not result in a CMCI.

Workaround: It is possible for the BIOS to contain a workaround for this erratum.

Status: For the Steppings affected, see the *Summary Tables of Changes*.

### **SKZ14 A UPI Phy Reset And Rx CRC Error on The Same Packet May Cause Link Layer LLRSN Aborts**

Problem: A UPI Phy Reset and Rx CRC error on same packet-are causing the retry sequence to abort leading to a UPI Phy re-initialization.

Implication: Due to this erratum, an unexpected UPI Phy re-initialization may occur before the program LLSRM threshold has been hit.

Workaround: None Identified.

Status: For the Steppings affected, see the *Summary Tables of Changes*.

### **SKZ15 CSRs SVID And SDID Are Not Implemented For Some DDRIO And PCU devices**

Problem: The DDRIO (Bus: 3; Device 19,22; Function 6,7 and "Bus: 0; Device: 20,23; Function: 4,5,6,7;) and PCU (Bus: 3; Device 31; Functions 0,2) do not implement the SVID (Offset 0x2C) and SDID (Offset 0x2E) CSRs.

Implication: SW relying on DDRIO and PCU SVID and SDID CSR support may not function correctly.

Workaround: None. Do not use SVID and SDID for these devices and functions.

Status: For the Steppings affected, see the *Summary Tables of Changes*.

### **SKZ16 Register Broadcast Read From DDRIO May Return a Zero Value**

Problem: When performing a BIOS broadcast register read to DDRIO a value of 0 is always returned.

Implication: When this erratum occurs, BIOS may not be able to proceed due to always reading a value of 0.

Workaround: None. Use unicast register read for each instance instead of broadcast register read for all instances at once.

Status: For the Steppings affected, see the *Summary Tables of Changes*.

### **SKZ17 Intel® CMT Counters May Not Count Accurately**

Problem: Under complex microarchitectural conditions, the CMT (Cache Monitoring Technology) counters may overcount.

Implication: Software relying on CMT registers to enable resource allocation may not operate correctly. This may lead to reporting of more cachelines used than the cache supports or the counter wrapping and returning a too small value. WBINVD may not result in the CMT counters being zeroed. Intel has not observed this erratum in commercially available software.

Workaround: None.

Status: For the Steppings affected, see the *Summary Tables of Changes*.



### **SKZ18 Intel® CAT May Not Restrict Cacheline Allocation Under Certain Conditions**

- Problem:** Under certain microarchitectural conditions involving heavy memory traffic , cachelines may fill outside the allocated L3 capacity bitmask (CBM) associated with the current Class of Service (CLOS).
- Implication:** CAT (Cache Allocation Technology) may appear less effective at protecting certain classes of applications, including cache-sensitive workloads than on previous platforms.
- Workaround:** None identified.
- Status:** For the Steppings affected, see the *Summary Tables of Changes*.

### **SKZ19 Intel® MBM Counters May Undercount**

- Problem:** The MBM (Memory Bandwidth Monitoring) counters will increment for reads but will not increment for memory writes. The performance counters in the IMC (integrated memory controller) are not affected and can report the read and write memory bandwidths.
- Implication:** MBM accuracy may be reduced, which can affect performance monitoring or bandwidth-aware scheduling. Applications may be unevenly charged for bandwidth depending on their characteristics.
- Workaround:** None identified. This erratum can be mitigated by using the IMC performance monitoring counters to derive a read/write ratio that can be used to adjust the MBM counters.
- Status:** For the Steppings affected, see the *Summary Tables of Changes*.

### **SKZ20 Intel® PCIe\* Corrected Error Threshold Does Not Consider Overflow Count When Incrementing Error Counter**

- Problem:** The PCIe\* corrected error counter feature does not take the overflow bit in the count (bit 15 of XPCORERRCOUNTER (Bus; RootBus Device; 0 Function; 0 Offset; 4D0h)) into account when comparing the count to the threshold in XPCORERRTHRESHOLD.ERROR\_THRESHOLD. Therefore, you end up with another interrupt once the counter has rolled over and hit your threshold + 0x8000.
- Implication:** Due to this erratum, the PCIe\* corrected error signaling may occur even after the error count has exceeded the corrected error count threshold, not just a single time when reaching the threshold. Intel has not observed this erratum with any commercially available system.
- Workaround:** None Identified
- Status:** For the Steppings affected, see the *Summary Tables of Changes*.

### **SKZ21 IIO RAS VPP Hangs During The Warm Reset Test**

- Problem:** When VPPCL bit 0 of VPP\_reset\_Mode (Bus 1; Device 30; Function 5; Offset 0xF0) bit is set to 0, and the CPU is undergoing reset flow while PCIe\* hotplug operation is in process, the VPP (Virtual Pin Port) hotplug commands may stop responding.
- Implication:** Due to this erratum, during CPU reset hotplug commands may not get completed.
- Workaround:** None. Do not set VPP reset mode to 0.
- Status:** For the Steppings affected, see the *Summary Tables of Changes*.

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