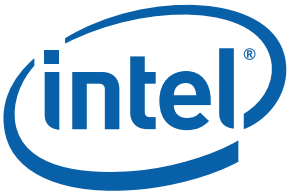

Intel® 200 (Including X299 Chipset)and Intel® Z370 Series Chipset Families Platform Controller Hub

Specification Update

May 2020

Revision 008

Document Number: 335194-008

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Revision History

Revision	Description	Date
001	• Initial Release	January 2017
002	• Added Intel X299 Series Chipset - Updated Identification Information table with SKU information	May 2017
003	• Added Intel Z370 Series Chipset - Updated Identification Information table with SKU information	October 2017
004	• The following errata is added - — USB DbC or Device Mode Port When Resuming from S3, S4, S5, or G3 State	February 2019
005	• The following errata is added - — PCIe* Root Port CLKREQ# Asserted Low to Clock Active Timing	March 2019
006	• The following errata is added - — xHCI USB 2.0 ISOCH Device Missed Service Interval	August 2019
007	• The following errata is added - — xHCI Short Packet Event Using Non-Event Data TRB — eSPI SBLCL Register Bit Not Cleared by PLTRST# — SATA Enclosure Management LED Messaging • The following errata is updated — USB DbC or Device Mode Port When Resuming from S3, S4, S5, or G3 State	January 2020
008	• The following errata is updated — Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment	May 2020

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Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata and specification changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents

Title	Document Number
Intel® 200 Series Chipset Family Platform Controller Hub (PCH), Datasheet Volume 1 of 2	335192
Intel® 200 Series Chipset Family Platform Controller Hub (PCH), Datasheet Volume 2 of 2	335193

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Stepping

X:	Erratum exists in the stepping indicated. Specification Change that applies to the stepping indicated.
(No mark) or (Blank box):	This erratum is fixed or not applicable in listed stepping or Specification Change does not apply to listed stepping.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Errata

Erratum Number	Stepping	Status	ERRATA
	A0		
1	X	No Plan to Fix	xHC Data Packet Header and Payload Mismatch Error Condition
2	X	No Plan to Fix	USB SuperSpeed Packet with Invalid Type Field Issue
3	X	No Plan to Fix	xHC Behavior with Three Consecutive Failed U3 Entry Attempts
4	X	No Plan to Fix	xHCI Controller OC# Issue
5	X	No Plan to Fix	xHCI USB2.0 Split-Transactions Error Counter Reset Issue
6	X	No Plan to Fix	USB xHCI Controller May Not Re-enter a D3 State After a USB Wake Event
7	X	No Plan to Fix	USB 3.0 Devices Not Detected After Sx Resume
8	X	No Plan to Fix	PCI Express* Unexpected Completion Status Bit May Get Set
9	X	No Plan to Fix	eSPI Concurrent Get-Config and Flash Cycles
10	X	No Plan to Fix	xHCI U3 Wake Exit Issue
11	X	No Plan to Fix	xHCI controller USB Debug Port Disconnect Issue
12	X	No Plan to Fix	PSIC Field Incorrect Value
13	X	No Plan to Fix	xHCI Extended Capabilities Registers are Incorrectly Implemented as Read/Write
14	X	No Plan to Fix	eSPI Turn Around (TAR) Specification Violation
15	X	No Plan to Fix	SMBus Transaction Using Memory Mapped I/O Registers
16	X	No Plan to Fix	xHCI Warm Reset to Unused USB3 Port May Hang the Platform
17	X	No Plan to Fix	xHCI Host Controller USB 2.0 Control Transfer May Cause IN Data to be Dropped
18	X	No Plan to Fix	System May Hang While Restoring HSIO ModPHY Configuration
19	X	No Plan to Fix	xHCI Host Controller Reset May Cause a System Hang
20	X	No Plan to Fix	PCI Express* Gen2 x4 Device may cause a Machine Check Exception
21	X	No Plan to Fix	PCIe* L1 Sub-States Premature Termination of PCI Express* PME_Turn_Off Messaging Handshake
22	X	No Plan to Fix	PCH PCIe* Controller Root Port (ACSCTLR) Appear as Read Only
23	X	No Plan to Fix	eSPI Error Reporting
24	X	No Plan to Fix	USB 3.0 DCI Control Packet Issue
25	X	No Plan to Fix	eSPI Fatal Error Handling
26	X	No Plan to Fix	Subsequent Deep S5 and S5 Exits Impacted After "Straight to S5 (Host Stays There)" Resets
27	X	No Plan to Fix	eSPI Bus Mastering
28	X	No Plan to Fix	Intermittent CATERR May Occur When Back to Back xHCI Host controller Resets are Performed
29	X	No Plan to Fix	USB DbC or Device Mode Port When Resuming from S3, S4, S5, or G3 State
30	X	No Plan to Fix	PCIe* Root Port CLKREQ# Asserted Low to Clock Active Timing
31	X	No Plan to Fix	xHCI USB 2.0 ISOCH Device Missed Service Interval
32	X	No Plan to Fix	xHCI Short Packet Event Using Non-Event Data TRB
33	X	No Plan to Fix	eSPI SBLCL Register Bit Not Cleared by PLTRST#
34	X	No Plan to Fix	SATA Enclosure Management LED Messaging
35	X	No Plan to Fix	Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment

Specification Changes

Number	Stepping	Specification Changes
	A0	
		No specification changes in this revision of the Specification Update

Identification Information

Markings

PCH Stepping	Top Marking (S-Spec)	Notes
A0	SR2WB	Desktop Intel® Chipset Z270
A0	SR2WA	Desktop Intel® Chipset H270
A0	SR2WE	Desktop Intel® Chipset Q270
A0	SR2WD	Desktop Intel® Chipset Q250
A0	SR2WC	Desktop Intel® Chipset B250
A0	SR2Z2	High-End Desktop (HEDT) Intel® Chipset X299
A0	SR3MD	Desktop Intel® Chipset Z370

Errata

1. xHC Data Packet Header and Payload Mismatch Error Condition

Problem: If a SuperSpeed device sends a DPH (Data Packet Header) to the xHC with a data length field that specifies less data than is actually sent in the DPP (Data Packet Payload), the xHC will accept the packet instead of discarding the packet as invalid.

Note: The USB 3.0 specification requires a device to send a DPP matching the amount of data specified by the DPH.

Implication: The amount of data specified in the DPH will be accepted by the xHC and the remaining data will be discarded and may result in anomalous system behavior.

Note: This issue has only been observed in a synthetic test environment with a synthetic device.

Workaround: None.

Status: No Plan to Fix.

2. USB SuperSpeed Packet with Invalid Type Field Issue

Problem: If the encoding for the "type" field for a SuperSpeed packet is set to a reserved value and the encoding for the "subtype" field is set to "ACK", the xHC may accept the packet as a valid acknowledgement transaction packet instead of ignoring the packet.

Note: The USB 3.0 specification requires that a device never set any defined fields to reserved values.

Implication: System implication is dependent on the misbehaving device and may result in anomalous system behavior.

Note: This issue has only been observed in a synthetic test environment with a synthetic device.

Workaround: None.

Status: No Plan to Fix.

3. xHC Behavior with Three Consecutive Failed U3 Entry Attempts

Problem: The xHC does not transition to the SS.Inactive USB 3.0 LTSSM (Link Training and Status State Machine) state after a SuperSpeed device fails to enter U3 upon three consecutive attempts.

Note: The USB 3.0 specification requires a SuperSpeed device to enter U3 when directed.

Implication: The xHC will continue to try to initiate U3. The implication is driver and operating system dependent.

Workaround: None.

Status: No Plan to Fix.

4. xHCI Controller OC# Issue

Problem: xHCI Host Controller Reset (HCRST) may not complete if a USB over-current event occurs while powering on or resuming from S5 or S4.

Implication: Upon resume all xHCI Ports may become non-functional.

Note: To recover xHCI port functionality requires the USB Device causing an overcurrent event to be removed and the system to be reset.

Workaround: None.

Status: No Plan to Fix.

5. xHCI USB2.0 Split-Transactions Error Counter Reset Issue

Problem: The xHCI controller may not reset its split transaction error counter if a high-speed USB hub propagates a mal-formed bit from a low-speed or full-speed USB device exhibiting non-USB specification compliant signal quality.

Implication: The implication is device dependent.

Full Speed and Low Speed devices behind the hub may be re-enumerated and may cause a device to not function as expected.

Workaround: None.

Status: No Plan to Fix.

6. USB xHCI Controller May Not Re-enter a D3 State After a USB Wake Event

Problem: After processing a USB 3.0 wake event, the USB xHCI controller may not re-enter D3 state.

Implication: When the failure occurs, the system will not enter an Sx state.

Workaround: A code change has been identified and may be implemented as a workaround for this erratum.

For Microsoft* Windows* 7, workaround is included in Intel® USB 3.0 eXtensible Host Controller Driver, version 4.0.0.23 or later.

For Microsoft* Windows* 8.1, workaround is included in Intel® USB 3.0 Host Controller Adaptation Driver, version 1.0.0.27 or later.

Status: No Plan to Fix.

7. USB 3.0 Devices Not Detected After Sx Resume

Problem: While the system is in S3/S4/S5 and a USB 3.0 device is disconnected and reconnected to a system, the Cold Attach Status (CAS) bit 24 of PORTSCNUSB3-xHCI USB3 Port N Status and Control Register may be overwritten.

Implication: The system may not detect USB 3.0 devices after wake from S3/S4/S5.

Workaround: A Software code change has been identified and may be implemented as a workaround for this erratum.

Status: No Plan to Fix.

8. PCI Express* Unexpected Completion Status Bit May Get Set

Problem: A PCI Express* Device replaying an Completion TLP may incorrectly cause an Unexpected Completion Error.

Note: This has only been observed when a PCIe* device causes frequent link corruptions and recovery events to occur.

Implication: Bit 16 Unexpected Completion Status (UC) may get set in the UnCorrectable Error Status (UES) Register (PCI Express*-D28:F0/F1/F2/F3/F4/F5:offset 104h).

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No plan to Fix.

9. eSPI Concurrent Get-Config and Flash Cycles

Problem: When an eSPI Get_Config cycle occurs concurrently with a flash cycle, the eSPI controller may stop working.

Note: The issue has only been observed in a synthetic test environment only.

Implication: System may hang.

Workaround: None.

Status: No Plan to Fix.

10. xHCI U3 Wake Exit Issue

Problem: xHCI Controller does not send the LFPS wake handshake for the full 10 ms and reattempts U3 wakeup prior to the minimum 100ms wait time following a tNoLFPSResponseTimeout.

Note: USB3 Specification Section 7.5.9.2 Exit from U3 specifies the port shall remain in U3 when the 10-ms LFPS handshake timer times out (tNoLFPSResponseTimeout). And 7.2.4.2.7 Low Power Link State Exit Flow specifies a minimum of 100 ms delay between attempts to reinitiate U3 wakeup again.

Implication: Implication will be USB3 Super-Speed Device and OS / Host Driver dependent.

Note: Intel has Only observed this in a Synthetic Test Environment.

Workaround: None.

Status: No Plan to Fix.

11. xHCI controller USB Debug Port Disconnect Issue

Problem: USB 3.0 Debug Port may hang when removing USB debug device.

Note: This issue has only been observed infrequently during USB debug connector unplug events.

Implication: The Port will not function and require a Platform Reset to recover.

Workaround: None.

Status: No Plan to Fix.

12. PSIC Field Incorrect Value

Problem: PSIC (The Protocol Speed ID Count) field incorrectly reports a value of 3. PSIC should report 6 indicating SSIC support.

Implication: If software utilizes PSIC, it may incorrectly determine SSIC is not supported. Additionally xHCI CV TD 1.09 Protocol Speed ID Test fails. Intel has obtained a waiver for PSIC.

Workaround: None Identified.

Status: No Plan to Fix.

13. xHCI Extended Capabilities Registers are Incorrectly Implemented as Read/Write

Problem: Bits [15:0] of xHCI Extended Capabilities CSR (Debug Capability Descriptor Parameters – XHCI_BAR, Offset 8740H) are incorrectly implemented as Read/Write, instead of Read-Only.

Implication: This erratum causes the USB-IF xHCI CV TD 1.05 Extended Capabilities Registers Tests to report a failure; Intel has obtained a waiver for TD1.05. Intel has not observed this erratum with any commercially available software.

Workaround: None.

Status: No Plan to Fix.

14. eSPI Turn Around (TAR) Specification Violation

Problem: During the Turn Around (TAR) window, the eSPI controller does not drive the data lines to logic ‘1’ for the first clock as specified by the eSPI specification.

Implication: There are no known functional failures due to this issue.

Workaround: None.

Status: No Plan to Fix.

15. SMBus Transaction Using Memory Mapped I/O Registers

Problem: When using memory-mapped-I/O DATA register for a SMBus write transaction, data transmitted from the register for Byte Write, Block Write, or Send Byte operation with Packet Error Check (PEC) enabled may not match the data programmed by software.

Implication: The SMBus transaction may fail. Implication depends on the failing transaction.

Workaround: Platform software should use IO-mapped registers for SMBus transactions.

Status: No Plan to Fix.

16. xHCI Warm Reset to Unused USB3 Port May Hang the Platform

Problem: Setting the USB3 Port Disable Override (USB3PDO) bit in xHCI Memory Mapped register USB3 Port Disable Override (USB3PDO)—Offset 84FCh Bits 9:0 for an unused port may cause the port to get stuck in RXDetect State not allowing a platform to reboot or enter S3, S4 or S5.

Implication: Platform may hang upon rebooting or entering S3, S4 or S5.

Status: A BIOS code change has been identified and may be implemented as a workaround for this erratum. No Plan to Fix.

17. xHCI Host Controller USB 2.0 Control Transfer May Cause IN Data to be Dropped

Problem: USB 2.0 Control Transfers may incorrectly clear a USB 2.0 flow control condition to a USB 2.0 IN endpoint resulting in the dropping of IN Data to the flow controlled endpoint. Exposure is sensitive to high volume of unrelated OUT transactions occurring on the xHCI Host controller.

Implication: USB 2.0 Device dependent and may result in anomalous USB 2.0 Device behavior.

Note: Intel has only observed this with a single USB2.0 Device which frequently used USB 2.0 Control Transfers during operation

Workaround: None. A BIOS code change has been identified and may be implemented as a workaround to significantly minimize exposure to the occurrence of this erratum.

Status: No Plan to Fix.

18. System May Hang While Restoring HSIO ModPHY Configuration

Problem: While Power Management Controller (PMC) is restoring High Speed I/O (HSIO) Modular Physical Layer (ModPHY) configuration during resume from S3, S4, S5 or while performing a platform reset the PMC may hang if a PMC managed timer expires during this time period.

Implication: System may hang during resume.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Plan to Fix.

19. xHCI Host Controller Reset May Cause a System Hang

Problem: xHCI Host Controller may not respond following system software setting (Bit 1 = '1') the Host Controller Reset (HCRST) of the USB Command Register (xHCIBAR + 80h).

Implication: CATERR may occur resulting in a system hang.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Plan to Fix.

20. PCI Express* Gen2 x4 Device may cause a Machine Check Exception

Problem: PCH PCI Express* Host Controller when configured as Gen2 x4 may not properly handle an abrupt link transition to electrical idle without receiving Electrical Idle Ordered Set (EIOS) such as during hot unplug event.

Implication: Platform May Hang due to a Machine Check Exception if all of the following conditions are met when the link is terminated abruptly:

- No 8b10b errors occur,
- A TLP of exactly 3DWords is received (length started to count from STP as the first byte) **Note:** A valid TLP length is 5DWords at least,
- The TLP must end with END or EDB,
- And dependent on the specific internal timing of the DW alignment.

Workaround: None.

Status: No Plan to Fix.

21. PCIe* L1 Sub-States Premature Termination of PCI Express* PME_Turn_Off Messaging Handshake

Problem: Power Management Controller (PMC) may prematurely power gate a PCIe* Root Port with L1 Sub-States (L1.1 and L1.2) enabled without waiting for the PME_TO_Ack response from attached PCIe* device entry into S3, S4, S5 or while preforming a platform reset with or without Power Cycle.

Implication: Wake capable PCIe* Devices may not be able to be armed to assert WAKE# due to the premature termination of the PME_Turn_Off messaging handshake and may not

function upon resume from S3, S4, or S5.

There is no impact for non-wake capable PCIe* devices.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Plan to Fix.

22. PCH PCIe* Controller Root Port (ACSCTLR) Appear as Read Only

Problem: ACSCTLR (Access Control Services Control Registers) is implemented and documented in theDatasheet at Offset 0x148 instead of at Offset 0x146 as documented in the PCI-SIG PCI Express* Base Specification.

Implication: ACS aware software will not be able to access and configure ACSCTLR at Offset 0x146.

Workaround: ACS aware software must account for and access ACSCTLR at Offset 0x148 as documented in the Datasheet.

Status: No Plan to Fix.

23. eSPI Error Reporting

Problem: When errors occur on the eSPI interface, the eSPI error reporting registers (VWERR_SLV, LNKERR_SLV, FCERR_SLV, PCERR_SLV, SLV_CFG_REG_CTL) may not be updated correctly.

Implication: Platform implication depends on the software usage of the registers.

Workaround: None

Note: eSPI error handling software may issue an in-band reset to the eSPI device when detecting an error associated with these registers.

Status: No Plan to Fix.

24. USB 3.0 DCI Control Packet Issue

Problem: DbC (Debug Capability) Device connection may hang if the USB 3.0 host controller DCI (Direct Connect Interface) does not send Control Packets in multiples of 16.

Implication: USB 3.0 host controller DCI may hang.

Workaround: DbC software must ensure DCI Control Packets are sent in multiples of 16. And no concurrent OUT EP traffic is occurring while the Control Packets are in progress to the DCI device.

Status: No Plan to Fix.

25. eSPI Fatal Error Handling

Problem: The eSPI controller may not correctly handle fatal errors occurring on the eSPI bus.

Implication: System implication depends on the type of the fatal error and may result in a system hang.

Note: A fatal error is a rare event on the eSPI interface and this issue has only been observed by Intel in a synthetic test environment.

Workaround: None.

Status: No Plan to Fix.

26. Subsequent Deep S5 and S5 Exits Impacted After "Straight to S5 (Host Stays There)" Resets

Problem: Following a S0 resume from a "Straight to S5 (Host Stays There)" reset, the PCH may enforce earlier wake event restrictions from the "Straight to S5 (Host Stays There)" reset on subsequent Deep S5 and S5 exits causing some wake events not to be recognized by the PCH.

Note: This issue only occurs on platforms where Deep S5 is enabled. This issue does not impact S3/S4 exits.

Implication:

- On subsequent Deep S5 exits, the following events will not be able to wake the system:
  - RTC Alarm, PCIe* WAKE# pin, and Wake Alarm Device.
- On subsequent S5 exits if the S5 entry is due leaving Deep Sx because of ACPRESENT assertion, the following events will not be able to wake the system:
  - RTC Alarm, PCIe* WAKE# pin, Wake Alarm Device, GPIOs and Secondary PME#
- If system is in S5 for any other reason, this issue will not be present.

Workaround: None

Note: The Deep S5 / S5 exit restrictions will be cleared after DSW_PWROK assertion (G3 power state) or after another global reset occurs (as long as global reset is not of the type "Straight to S5 (Host Stays There)").

Status: No Plan to Fix.

27. eSPI Bus Mastering

Problem: The eSPI controller may not successfully complete bus mastering cycles from a slave device as described below:

1. Upstream memory write from EC may have the last DW dropped if there is an upstream completion of a configuration cycle occurring at the same time.
2. The controller may prevent the system from entering a warm reset if an upstream non-posted cycle is pending.
3. The controller may not perform ordering between posted/non-posted/completion requests.

The issue has only been observed in synthetic testing environment**.**

Implication: System may hang.

Workaround: None.

Status: No Plan to Fix.

28. Intermittent CATERR May Occur When Back to Back xHCI Host controller Resets are Performed

Problem: The xHCI host controller may fail to respond, due to an internal race condition, if consecutive xHCI Host Controller resets are performed.

Implication: A processor CATERR may occur during warm boot testing or S4/S5 cycling tests.

Workaround: Software should add a 120ms delay in between consecutive xHCI host controller resets.

Status: No Plan to Fix.

29. USB DbC or Device Mode Port When Resuming from S3, S4, S5, or G3 State

Problem: If a PCH USB Type-C* port is configured in Device Mode (or in DbC mode) and connected to an external USB 3.2 host controller, it may cause the USB port to go into a non-functional state in the following scenarios:

1. The PCH resumes from S3, S4, or S5 state, the port may remain in U2.
2. The port is connected to a USB 3.2 Gen 1x1 host controller when resuming from S3, S4, S5, or G3, the port may enter into Compliance Mode or an inactive state if Compliance Mode is disabled.
3. The port is connected to a USB 3.2 Gen 2x1 host controller when resuming from S3, S4, S5, or G3, the port may enter an inactive state.

Implication: PCH USB Type-C* port configured in Device Mode (or in DbC mode) may fail to enumerate or become unavailable.

Workaround: None identified.

Status: No Plan to Fix.

30. PCIe* Root Port CLKREQ# Asserted Low to Clock Active Timing

Problem: During L1 exit, the PCH PCIe* Root Ports may exceed the CLKREQ# asserted low to clock active maximum specification due to PCH PCIe* clock un-gate path delays.

Implication: PCIe* end point device L1 exit instabilities may be observed.

Note: PCIe* end point devices that message LTR latency greater than or equal to 1 us are not affected by this.

Workaround: None.

- Platforms not supporting S0ix with PCIe* end point devices that do not support LTR may disable the associated PCH SRCCLKREQ# signal to keep the PCIe* clock active during L1.
- Platforms supporting S0ix with PCIe* end point devices that have LTR latencies less than 1 us may disable the associated PCH SRCCLKREQ# signal to keep the PCIe* clock active during L1.

Status: No Plan to Fix.

31. xHCI USB 2.0 ISOCH Device Missed Service Interval

Problem: When the xHCI controller is stressed with concurrent traffic across multiple USB ports, the xHCI controller may fail to service USB 2.0 Isochronous IN endpoints within the required service interval.

Implication: USB 2.0 isochronous devices connected to the xHCI controller may experience dropped packets.

Note: This issue has only been observed in a synthetic environment.

Workaround: None.

Status: No Plan to Fix.

32. xHCI Short Packet Event Using Non-Event Data TRB

Problem: The xHCI may generate an unexpected short packet event for the last transfer's Transfer Request Block (TRB) when using Non-Event Data TRB with multiples TRBs.

Implication: Transfer may fail due to the packet size error.

Note: This issue has only been observed in an synthetic environment. No known implication has been identified with commercial software.

Workaround: None identified. Intel recommends software to use Data Event TRBs for short packet completion.

Status: No Plan to Fix.

33. eSPI SBLCL Register Bit Not Cleared by PLTRST#

Problem: The IOSF-SB eSPI Link Configuration Lock (SBLCL) bit (offset 4000h, bit 27 in eSPI PCR space) is reset by RSMRST# assertion instead of PLTRST# assertion.

Implication: If the SBLCL bit is set to 1, software will not be able to access the eSPI device Capabilities and Configuration register in the reserved address range (0h - 7FFh) until RSMRST# asserts.

Workaround: If software needs to access the eSPI device reserved range 0h - 7FFh while SBLCL bit is set to 1, a RSMRST# assertion should be performed.

Status: No Plan to Fix.

34. SATA Enclosure Management LED Messaging

Problem: When sending a SATA enclosure LED message and all SATA ports are either idle or disabled, the PCH may not transmit the LED message due to an internal clock gating issue.

Implication: The LED status for SATA enclosure may be incorrect.

Workaround: None Identified. Enclosure Management SW can poll the Enclosure Management (EM_CTL) - Offset 20h bit 8 register for a 0 value immediately before writing LED messages.

Status: No Fix

35. Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment

Problem: If software assigns a 4 GB-aligned address to the Linked List Pointer (LLP_LOn = 0h) for Intel® Serial I/O Controller DMA engine, then the DMA engine interprets this as an empty link list and will not perform DMA transfers.

Implication: An Intel Serial IO controller (i.e., I2C, GSPI, or UART) may stop operating which may cause the system to hang.

Workaround: Driver software should not assign LLP to a 4 GB-aligned address.

Note: This issue has been addressed in the Intel Serial IO drivers in the following versions or later: For Microsoft* Windows* 10, I2C device driver rev 30.100.1724.2, SPI device driver rev 30.100.1725.1, and UART device driver rev 30.100.1725.1.

Status: No Plan to fix.

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Specification Changes

There are no Specification Changes in this revision of the Specification Update.

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