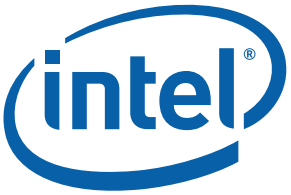

Intel® 100 Series and C230 Series Chipset Family Platform Controller Hub

Specification Update

December 2018

Revision 015

Document #: 332692-015

Contents

Revision History

Revision	Description	Date
001	• Initial Release	August 2015
002	• Added Intel® C230 Series Chipset • Added Identification Information section • Errata: Updated Errata 5, 8, 9, 10	February 2016
003	• Errata: Added errata 12-25	March 2016
004	• Errata: Added errata 26-29	May 2016
005	• Revision number skipped	N/A
006	• Errata: — Removed erratum 11 in previous revision as it was replaced with erratum 26, iSPI Error Reporting — Removed erratum 5 in previous revision — Added errata 29-30	August 2016
007	• Identification Information — Updated Markings table • Errata — Added errata 31-32	February 2017
008	• Revision number skipped	N/A
009	• Errata — Updated erratum 20 — Added errata 33-39	March 2017
010	• Errata — Added erratum 40	June 2017
011	• Errata — Added erratum 41	July 2017
012	• Errata — Added erratum 42	August 2017
013	• Errata — Added errata 43-44 — Added erratum 45	July 2018
014	• Errata — Added erratum 46	November 2018
015	• Errata — Added erratum 47	December 2018

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Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata and specification changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents

Title	Document Number
Intel® 100 Series and C230 Series Chipset Family Platform Controller Hub Datasheet - Volume 1 of 2	332690

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Stepping

X:	Erratum exists in the stepping indicated. Specification Change that applies to the stepping indicated.
(No mark) or (Blank box):	This erratum is fixed or not applicable in listed stepping or Specification Change does not apply to listed stepping.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata (Sheet 1 of 2)

Erratum Number	Stepping	Status	ERRATA
	D1		
1	X	No Fix	xHC Data Packet Header and Payload Mismatch Error Condition
2	X	No Fix	USB SuperSpeed Packet with Invalid Type Field Issue
3	X	No Fix	xHC Behavior with Three Consecutive Failed U3 Entry Attempts
4	X	No Fix	Max Packet Size and Transfer Descriptor Length Mismatch
5	X	No Fix	xHCI Controller OC# Issue
6	X	No Fix	xHCI USB2.0 Split-Transactions Error Counter Reset Issue
7	X	No Fix	USB xHCI Controller May Not Re-enter a D3 State After a USB Wake Event
8	X	No Fix	USB 3.0 Devices Not Detected After Sx Resume
9	X	No Fix	PCI Express Unexpected Completion Status Bit May Get Set
10	X	No Fix	eSPI Concurrent Get-Config and Flash Cycles
11	X	No Fix	xHCI U3 Wake exit Issue
12	X	No Fix	xHCI controller USB Debug Port Disconnect Issue
13	X	No Fix	PSIC field incorrect value
14	X	No Fix	xHCI Extended Capabilities Registers are Incorrectly Implemented as Read/Write
15	X	No Fix	eSPI Turn Around (TAR) Spec Violation
16	X	No Fix	SMBus Transaction Using Memory Mapped I/O Registers
17	X	No Fix	xHCI Warm Reset to Unused USB3 port may hang the platform
18	X	No Fix	xHCI Host Controller USB 2.0 Control Transfer may cause IN Data to be dropped
19	X	No Fix	System may hang while restoring HSIO ModPHY configuration
20	X	No Fix	xHCI Host Controller Reset May Lead to a System Hang
21	X	No Fix	PCI Express Gen2 x4 Device may cause a Machine Check Exception
22	X	No Fix	PCIe L1 Sub-States Premature Termination of PCI Express PME_Turn_Off Messaging Handshake
23	X	No Fix	PCH PCIe* Controller Root Port (ACSCTLR) Appear as Read Only
24	X	No Fix	Pull-up and Pull-down on SPI CS# and CLK Signals
25	X	No Fix	eSPI Error Reporting
26	X	No Fix	USB 3.0 DCI Control Packet issue
27	X	No Fix	eSPI Fatal Error Handling
28	X	No Fix	PCH PCIe* TX Pin State During L1.0 and L1.1 Substates
29	X	No Fix	Subsequent Deep S5 and S5 Exits Impacted After “Straight to S5 (Host Stays There)” Resets
30	X	No Fix	eSPI Bus Mastering
31	X	No Fix	Intermittent CATERR may occur when back to back xHCI Host controller resets are performed
32	X	No Fix	The DMI/PCIe Gen3 PLL May Not Wake From Link Low Power States
33	X	No Fix	Dual PCIe*/SATA Muxing Configurations May Prevent HSIO Phy Power Gating
34	X	No Fix	Voltage Floating on USB - Device Mode Capable Port
35	X	No Fix	USB3.0 – Jitter Tolerance Margin
36	X	No Fix	Failure of USB compliance test TD 7.01 Link Bring-up Test (Subtests 1 & 2)
37	X	No Fix	Intermittent failure of USB compliance test TD3.08

Errata (Sheet 2 of 2)

Erratum Number	Stepping	Status	ERRATA
	D1		
38	X	No Fix	Intel® RST for PCIe Storage - SATA PCI Configuration Read
39	X	No Fix	SUSPWRDNACK not driven High when Intel® ME is power gated
40	X	No Fix	xHCI Controller may hang on D3 entry following a Hog-plug event
41	X	No Fix	USB2.0 PLL may fail to lock during S3 resume
42	X	No Fix	PCIEXP_WAKE_STS bit not set as expected
43	X	No Fix	xHCI USB Hardware LPM Capability (HLC) register reset to the default value during D3-D0 transition
44	X	No Fix	Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment
45	X	No Fix	xHCI Controller May Delayed Transactions Due to Short Packets Issue
46	X	No Fix	USB DbC or Device Mode Port When Resuming from Sx/G3 State
47	X	No Fix	PCIe Root Port CLKREQ# Asserted Low to Clock Active Timing

Specification Changes

Number	Stepping	SPECIFICATION CHANGES
	D1	
	X	There are no Specification Changes in this revision of the specification update.

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Identification Information

Markings

PCH Stepping	Top Marking (S-Spec)	Notes
D1	SR2CB	Server Intel® Series Chipset C232
D1	SR2CC	Server Intel® Series Chipset C236
D1	SR2C3	Mobile Intel® Series Chipset HM170
D1	SR2C4	Mobile Intel® Series Chipset QM170
D1	SR2CE	Mobile Intel® Series Chipset CM236
D1	SR2C5	Desktop Intel® Series Chipset Q170
D1	SR2C6	Desktop Intel® Series Chipset Q150
D1	SR2C7	Desktop Intel® Series Chipset B150
D1	SR2C8	Desktop Intel® Series Chipset H170
D1	SR2C9	Desktop Intel® Series Chipset Z170
D1	SR2CA	Desktop Intel® Series Chipset H110
D1	SR30V	Mobile Intel® Series Chipset QM175
D1	SR30W	Mobile Intel® Series Chipset HM175

Errata

1. xHC Data Packet Header and Payload Mismatch Error Condition

Problem: If a SuperSpeed device sends a DPH (Data Packet Header) to the xHC with a data length field that specifies less data than is actually sent in the DPP (Data Packet Payload), the xHC will accept the packet instead of discarding the packet as invalid.

Note: The USB 3.0 specification requires a device to send a DPP matching the amount of data specified by the DPH.

Implication: The amount of data specified in the DPH will be accepted by the xHC and the remaining data will be discarded and may result in anomalous system behavior.

Note: This issue has only been observed in a synthetic test environment with a synthetic device.

Workaround: None.

Status: No Plan to Fix.

2. USB SuperSpeed Packet with Invalid Type Field Issue

Problem: If the encoding for the "type" field for a SuperSpeed packet is set to a reserved value and the encoding for the "subtype" field is set to "ACK", the xHC may accept the packet as a valid acknowledgment transaction packet instead of ignoring the packet.

Note: The USB 3.0 specification requires that a device never set any defined fields to reserved values.

Implication: System implication is dependent on the misbehaving device and may result in anomalous system behavior.

Note: This issue has only been observed in a synthetic test environment with a synthetic device.

Workaround: None.

Status: No Plan to Fix.

3. xHC Behavior with Three Consecutive Failed U3 Entry Attempts

Problem: The xHC does not transition to the SS.Inactive USB 3.0 LTSSM (Link Training and Status State Machine) state after a SuperSpeed device fails to enter U3 upon three consecutive attempts.

Note: The USB 3.0 specification requires a SuperSpeed device to enter U3 when directed.

Implication: The xHC will continue to try to initiate U3. The implication is driver and operating system dependent.

Workaround: None.

Status: No Plan to Fix.

4. Max Packet Size and Transfer Descriptor Length Mismatch

Problem: The xHC may incorrectly handle a request from a low-speed or full-speed device when all the following conditions are true:

- The sum of the packet fragments equals the length specified by the TD (Transfer Descriptor)
- The TD length is less than the MPS (Max Packet Size) for the device
- The last packet received in the transfer is "0" or babble bytes

Implication: The xHC will halt the endpoint if all the above conditions are met. All functions associated with the endpoint will stop functioning until the device is unplugged and reinserted.

Workaround: None.

Status: No Plan to Fix.

5. xHCI Controller OC# Issue

Problem: xHCI Host Controller Reset (HCRST) may not complete if a USB over-current event occurs while powering on or resuming from S5 or S4.

Implication: Upon resume all xHCI Ports may become non-functional.

Note: To recover xHCI port functionality requires the USB Device causing an over-current event to be removed and the system to be reset.

Workaround: None.

Status: No plan to fix.

6. xHCI USB2.0 Split-Transactions Error Counter Reset Issue

Problem: The xHCI controller may not reset its split transaction error counter if a high-speed USB hub propagates a malformed bit from a low-speed or full-speed USB device exhibiting non-USB specification compliant signal quality.

Implication: The implication is device-dependent.

- Full Speed and Low Speed devices behind the hub may be re-enumerated and may cause a device to not function as expected.

Workaround: None.

Status: No plan to fix.

7. USB xHCI Controller May Not Re-enter a D3 State After a USB Wake Event

Problem: After processing a USB 3.0 wake event, the USB xHCI controller may not re-enter D3 state.

Implication: When the failure occurs, the system will not enter a Sx state.

Workaround: A code change has been identified and may be implemented as a workaround for this erratum.

For Microsoft* Windows* 7, workaround is included in Intel® USB 3.0 eXtensible Host Controller Driver, version 4.0.0.23 or later.

For Microsoft* Windows* 8.1, workaround is included in Intel® USB 3.0 Host Controller Adaptation Driver, version 1.0.0.27 or later.

Status: No plan to fix.

8. USB 3.0 Devices Not Detected After Sx Resume

Problem: While the system is in S3/S4/S5 and a USB 3.0 device is disconnected and reconnected to a system, the Cold Attach Status (CAS) bit 24 of PORTSCNUSB3-xHCI USB3 Port N Status and Control Register may be overwritten.

Implication: The system may not detect USB 3.0 devices after wake from S3/S4/S5.

Workaround: A Software code change has been identified and may be implemented as a workaround for this erratum.

Status: No plan to fix.

9. PCI Express Unexpected Completion Status Bit May Get Set

Problem: A PCI Express Device replaying a Completion TLP may incorrectly cause an Unexpected Completion Error.

Note: This has only been observed when a PCIe device causes frequent link corruptions and recovery events to occur.

Implication: Bit 16 Unexpected Completion Status (UC) may get set in the UnCorrectable Error Status (UES) Register (PCI Express*-D28:F0/F1/F2/F3/F4/F5:offset 104h).

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No plan to fix.

10. eSPI Concurrent Get-Config and Flash Cycles

Problem: When an eSPI Get_Config cycle occurs concurrently with a flash cycle, the eSPI controller may stop working.

Note: The issue has only been observed in a synthetic test environment only.

Implication: System may hang.

Workaround: None.

Status: No Plan to Fix.

11. xHCI U3 Wake exit Issue

Problem: xHCI Controller does not send the LFPS wake handshake for the full 10ms and reattempts U3 wakeup prior to the minimum 100ms wait time following a tNoLFPSResponseTimeout.

Note: USB3 Specification Section 7.5.9.2 Exit from U3 specifies the port shall remain in U3 when the 10-ms LFPS handshake timer times out (tNoLFPSResponseTimeout). And 7.2.4.2.7 Low-Power Link State Exit Flow specifies a minimum of 100-ms delay between attempts to reinitiate U3 wakeup again.

Implication: Implication will be USB3 Super-Speed Device and OS / Host Driver dependent.

Note: Intel has Only observed this in a Synthetic Test Environment.

Workaround: None.

Status: No Plan To Fix.

12. xHCI controller USB Debug Port Disconnect Issue

Problem: USB 3.0 Debug Port may hang when removing USB debug device.

Note: This issue has only been observed infrequently during USB debug connector unplug events

Implication: The Port will not function and require a Platform Reset to recover.

Workaround: None.

Status: No Plan To Fix.

13. PSIC field incorrect value

Problem: PSIC (The Protocol Speed ID Count) field incorrectly reports a value of 3. PSIC should report 6 indicating SSIC support.

Implication: If software utilizes PSIC, it may incorrectly determine SSIC is not supported. Additionally xHCI CV TD 1.09 Protocol Speed ID Test fails. Intel has obtained a waiver for PSIC.

Workaround: None Identified.

Status: No Plan To Fix.

14. xHCI Extended Capabilities Registers are Incorrectly Implemented as Read/Write

Problem: Bits [15:0] of xHCI Extended Capabilities CSR (Debug Capability Descriptor Parameters – XHCI_BAR, Offset 8740H) are incorrectly implemented as Read/Write, instead of Read-Only.

Implication: This erratum causes the USB-IF xHCI CV TD 1.05 Extended Capabilities Registers Tests to report a failure; Intel has obtained a waiver for TD1.05. Intel has not observed this erratum with any commercially available software.

Workaround: None.

Status: No Plan To Fix.

15. eSPI Turn Around (TAR) Spec Violation

Problem: During the Turn Around (TAR) window, the eSPI controller does not drive the data lines to logic ‘1’ for the first clock as specified by the eSPI specification.

Implication: There are no known functional failures due to this issue.

Workaround: None.

Status: No Plan to Fix.

16. SMBus Transaction Using Memory Mapped I/O Registers

Problem: When using memory-mapped-I/O DATA register for a SMBus write transaction, data transmitted from the register for Byte Write, Block Write, or Send Byte operation with Packet Error Check (PEC) enabled may not match the data programmed by software.

Implication: The SMBus transaction may fail. Implication depends on the failing transaction.

Workaround: Platform software should use IO-mapped registers for SMBus transactions.

Status: No Plan to Fix.

17. xHCI Warm Reset to Unused USB3 port may hang the platform

Problem: Setting the USB3 Port Disable Override (USB3PDO) bit in xHCI Memory Mapped register USB3 Port Disable Override (USB3PDO)—Offset 84FCh Bits 9:0 for an unused port may cause the port to get stuck in RXDetect State not allowing a platform to reboot or enter S3, S4 or S5.

Implication: Platform may hang upon rebooting or entering S3, S4 or S5.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Plan to Fix.

18. xHCI Host Controller USB 2.0 Control Transfer may cause IN Data to be dropped

Problem: USB 2.0 Control Transfers may incorrectly clear a USB 2.0 flow control condition to a USB 2.0 IN endpoint resulting in the dropping of IN Data to the flow-controlled endpoint. Exposure is sensitive to high volume of unrelated OUT transactions occurring on the xHCI Host controller.

Implication: USB 2.0 Device dependent and may result in anomalous USB 2.0 Device behavior.

Note: Intel has only observed this with a single USB2.0 Device which frequently used USB 2.0 Control Transfers during operation

Workaround: None. A BIOS code change has been identified and may be implemented as a workaround to significantly minimize exposure to the occurrence of this erratum.

Status: No Plan To Fix.

19. System may hang while restoring HSIO ModPHY configuration

Problem: While Power Management Controller (PMC) is restoring High Speed I/O (HSIO) Modular Physical Layer (ModPHY) configuration during resume from S3, S4, S5 or while performing a platform reset the PMC may hang if a PMC-managed timer expires during this time period.

Implication: System may hang during resume.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Plan To Fix.

20. xHCI Host Controller Reset May Lead to a System Hang

Problem: An access to xHCI configuration space within 1ms of setting the xHCI HCRST (Host Controller Reset) bit of the USB Command Register (xHCIBAR, offset 80h, Bit [1]) or a second setting of the HCRST bit within 120ms may cause the xHCI host controller to fail to respond.

Implication: Due to this erratum, the system may hang.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Plan To Fix.

21. PCI Express Gen2 x4 Device may cause a Machine Check Exception

Problem: PCH PCI Express Host Controller when configured as Gen2 x4 may not properly handle an abrupt link transition to electrical idle without receiving Electrical Idle Ordered Set (EIOS) such as during hot unplug event.

Implication: Platform May Hang due to a Machine Check Exception if all of the following conditions are met when the link is terminated abruptly:

- No 8b10b errors occur,
- A TLP of exactly 3DWords is received (length started to count from STP as the first byte) **Note:** A valid TLP length is 5DWords at least,
- The TLP must end with END or EDB,
- And dependent on the specific internal timing of the DW alignment.

Workaround: None.

Status: No Plan To Fix.

22. PCIe L1 Sub-States Premature Termination of PCI Express PME_Turn_Off Messaging Handshake

Problem: Power Management Controller (PMC) may prematurely power gate a PCIe Root Port with L1 Sub-States (L1.1 and L1.2) enabled without waiting for the PME_TO_Ack response from attached PCIe device entry into S3, S4, S5 or while performing a platform reset with or without Power Cycle.

Implication: Wake capable PCIe Devices may not be able to be armed to assert WAKE# due to the premature termination of the PME_Turn_Off messaging handshake and may not function upon resume from S3, S4, or S5.

There is no impact for non-wake capable PCIe devices.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Plan To Fix.

23. PCH PCIe* Controller Root Port (ACSCTLR) Appear as Read Only

Problem: ACSCTLR (Access Control Services Control Registers) is implemented and documented in the Datasheet at Offset 0x148 instead of at Offset 0x146 as documented in the PCI-SIG PCI Express® Base Specification.

Implication: ACS aware software will not be able to access and configure ACSCTLR at Offset 0x146.

Workaround: ACS aware software must account for and access ACSCTLR at Offset 0x148 as documented in the Datasheet.

Status: No Plan To Fix.

24. Pull-up and Pull-down on SPI CS# and CLK Signals

Problem: The pull up/pull down implementation before RSMRST# assertion on SPI chip select (CS#) and clock (CLK) signals does not match the specified behavior. The actual implementation has a ~20K pull down before RSMRST# assertion.

Implication: System implication depends on the external device requirements sampling the SPI CS# and CLK signals.

Workaround: Implement an external pull-up, depending on the external device requirements.

Status: No Plan to Fix.
The correct implementation information will be updated in Revision 002 of the Intel® 100 Series and C230 Series Chipset PCH Datasheet.

25. eSPI Error Reporting

Problem: When errors occur on the eSPI interface, the eSPI error reporting registers (VWERR_SLV, LNKERR_SLV, FCERR_SLV, PCERR_SLV, SLV_CFG_REG_CTL) may not be updated correctly.

Implication: Platform implication depends on the software usage of the registers.

Workaround: None.

Note: eSPI error handling software may issue an in-band reset to the eSPI device when detecting an error associated with these registers.

Status: No Plan to Fix.

26. USB 3.0 DCI Control Packet issue

Problem: DbC (Debug Capability) Device connection may hang if the USB 3.0 host controller DCI (Direct Connect Interface) does not send Control Packets in multiples of 16.

Implication: USB 3.0 host controller DCI may hang.

Workaround: DbC software must ensure DCI Control Packets are sent in multiples of 16. And no concurrent OUT EP traffic is occurring while the Control Packets are in progress to the DCI device.

Status: No Plan to fix.

27. eSPI Fatal Error Handling

Problem: The eSPI controller may not correctly handle fatal errors occurring on the eSPI bus.

Implication: System implication depends on the type of the fatal error and may result in a system hang.

Note: A fatal error is a rare event on the eSPI interface and this issue has only been observed by Intel in a synthetic test environment.

Workaround: None.

Status: No Plan to Fix.

28. PCH PCIe* TX Pin State During L1.0 and L1.1 Substates

Problem: Upon entry to L1.0 or L1.1 Substates the PCH PCIe* TX pins may internally get pulled down to ground instead of maintaining the link common mode voltage.

Implication: PCIe* devices that are in L1.0 or L1.1 may interpret the grounding of the TX pins as an exit event from electrical idle which may cause them to assert their CLKREQ# and exit the L1 Power Management.

Notes

- The issue has only been observed with a single 3rd Party PCIe* Device.
- The issue is depended on the end point device input squelch sensitivity and if the device sends a Latency Tolerance and Reporting (LTR) Snoop/Non-Snoop Latency Message above 50 Microseconds while entering L1.0 or L1.1 with CLKREQ# de-asserted.

Workaround: None.

Status: No Plan to Fix.

29. Subsequent Deep S5 and S5 Exits Impacted After "Straight to S5 (Host Stays There)" Resets

Problem: Following a S0 resume from a "Straight to S5 (Host Stays There)" reset, the PCH may enforce earlier wake event restrictions from the "Straight to S5 (Host Stays There)" reset on subsequent Deep S5 and S5 exits causing some wake events not to be recognized by the PCH.

Note: This issue only occurs on platforms where Deep S5 is enabled. This issue does not impact S3/S4 exits.

Implication:

- On subsequent Deep S5 exits, the following events will not be able to wake the system:
  - — RTC Alarm, PCIe WAKE# pin, and Wake Alarm Device.
- On subsequent S5 exits if the S5 entry is due leaving Deep Sx because of ACPRESENT assertion, the following events will not be able to wake the system:
  - — RTC Alarm, PCIe WAKE# pin, Wake Alarm Device, GPIOs and Secondary PME#
- If system is in S5 for any other reason, this issue will not be present.

Workaround: None.

Note: The Deep S5 / S5 exit restrictions will be cleared after DSW_PWROK assertion (G3 power state) or after another global reset occurs (as long as global reset is not of the type "Straight to S5 (Host Stays There)").

Status: No Plan to Fix.

30. eSPI Bus Mastering

Problem: The eSPI controller may not successfully complete bus mastering cycles from a slave device as described below:

1. Upstream memory write from EC may have the last DW dropped if there's an upstream completion of a configuration cycle occurring at the same time.
2. The controller may prevent the system from entering a warm reset if an upstream non-posted cycle is pending.
3. The controller may not perform ordering between posted/non-posted/completion requests.

The issue has only been observed in synthetic testing environment.

Implication: System may hang.

Workaround: None.

Status: No Plan to Fix.

31. Intermittent CATERR may occur when back to back xHCI Host controller resets are performed

Problem: The xHCI host controller may fail to respond, due to an internal race condition, if consecutive xHCI Host Controller resets are performed.

Implication: A processor CATERR may occur during warm boot testing or S4/S5 cycling tests.

Workaround: Software should add a 120ms delay in between consecutive xHCI host controller resets.

Status: No Plan to fix.

32. The DMI/PCIe Gen3 PLL May Not Wake From Link Low Power States

Problem: The DMI/PCIe Gen3 PLL may not wake from link low power states.

Implication: The system may hang or PCIe 3.0 device(s) may not function. A reboot will likely recover the system.
Note: The occurrence of the issue is rare and has only been observed on a small subset of units on a small number of platform designs.

Workaround: None.

Status: No Planned Fix

33. Dual PCIe*/SATA Muxing Configurations May Prevent HSIO Phy Power Gating

Problem: Muxed PCIe* Controller x2 or x4 configurations where logical lane 0 is assigned as SATA and the upper logical lanes are assigned to PCIe*, may prevent HSIO Phy Power Gating for the assigned PCIe* lanes.

Implication: SLP_S0# may not assert as expected.

Workaround: None Identified.

Status: No Fix.

34. Voltage Floating on USB - Device Mode Capable Port

Problem: During warm reset or host deep reset, the USB port 1 defaults to Device Controller mode and may take ~250 ms to switch back to Host Controller mode. During this time, the USB2 integrated pull downs are disabled and the D+/D- lines may float.

Implication: Device susceptible to SE1 will respond unexpectedly and may fail to enumerate.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix.

35. USB3.0 – Jitter Tolerance Margin

Problem: Following a Sx exit, or Cold Reset, BIOS and Intel® ME Firmware may not restore the electrical parameters associated with Rx jitter tolerance margin for the USB 3.0 interface.
The issue does not occur on an initial boot from G3 or warm reboot.

Implication: Degradation of jitter tolerance margin on USB3.0 port may be observed.

Workaround: None.

Status: No Fix.

36. Failure of USB compliance test TD 7.01 Link Bring-up Test (Subtests 1 & 2)

Problem: Upon receiving Polling.LFPS burst, the xHCI controller sends 3 consecutive Polling.LFPS bursts instead of 4 as per xHCI spec - section 7.5.4.3.2.

Implication: USB-IF TD 7.01 Link Bring-up Test (Subtests 1 & 2) may report a failure. Intel has obtained a waiver for TD 7.01.
Note: Intel has not observed any functional failure.

Workaround: None.

Status: No plans fix.

37. Intermittent failure of USB compliance test TD3.08

Problem: USB 2.0 port on the xHCI controller may remain in RESUME state for up to additional 20ms after software writes PORTSC.PLS to U0.

Implication: USB-IF xHCI CV TD 3.08 may report a failure. Intel has obtained a waiver for TD 3.08.
Note: Intel has not observed any functional failure with any commercially available software.

Workaround: None.

Status: No Fix.

38. Intel® RST for PCIe Storage - SATA PCI Configuration Read

Problem: If a PCIe link configured for Intel® RST for PCIe Storage is not trained to L0 due to an error condition (such as device misbehavior, board instability, or system mis-configuration, etc.), a read to any SATA PCI Configuration Space register may not be completed.
Note: this issue has only been observed in a synthetic test environment.

Implication: The incomplete transaction may cause a CATERR, resulting in a system hang.

Workaround: None.

Status: No Fix.

39. SUSPWRDNACK not driven High when Intel® ME is power gated

Problem: When the platform is in Sx (S3, S4 or S5) and the Intel® ME is in the power gated state (CM3-PG), the PCH does not drive SUSPWRDNACK as expected.

Implication: When the Intel® ME is in power gated state, the PCH Primary Well will not be turned off on platforms that use SUSPWRDNACK to control the well.
Note: Platforms that support Deep Sx are not impacted as SUSPWRDNACK is not used.

Workaround: None.

Status: No Fix.

40. xHCI Controller may hang on D3 entry following a Hog-plug event

Problem: The xHCI controller may hang on D3 entry if the xHCI driver is unable to service a port status change in between disconnect and re-connect of Super Speed device.

Implication: Due to this erratum, the system may hang.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix.

41. USB2.0 PLL may fail to lock during S3 resume

Problem: When a system is woken from S3 using a USB2.0 device, the USB2.0 PLL may fail to lock during the initialization process. Then, the eXtensible Host Controller may not send the Start of Frame (SOF) packets at the correct interval as specified per USB 2.0 specification.

Implication: USB2.0 devices may not enumerate correctly or yellow bang after resuming from S3.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix.

42. PCIEXP_WAKE_STS bit not set as expected

Problem: PCIEXP_WAKE_STS bit (PMC Controller D31:F2, Bit 14) is not set as expected after a PCI Express WAKE# event.

Implication: System Software may not be able to identify wake from PCI Express wake event using PCIEXP_WAKE_STS bit.

Workaround: None.

Status: No Fix.

43. xHCI USB Hardware LPM Capability (HLC) registers reset to the default value during D3-D0 transition

Problem: xHCI USB Hardware LPM Capability (HLC) registers 19 offset 8008 defaults back to its default value of "1" after D3-D0 transition.

Implication: System software may read this value and may enable LPM capability on a platform which is configured to disable LPM.
Note: Intel has only observed this in the Intel Windows* 7 xHCI driver (4.0.5.55 and older) which may check this bit during a driver upgrade.

Workaround: System software (driver) should not rely on the HLC bit. Fixed in Intel xHCI driver 4.0.6.60

Status: No Fix.

44. Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment

Problem: If software assigns a 4 GB-aligned address to the Linked List Pointer (LLP_LOn = 0h) for Intel® Serial I/O Controller DMA engine, then the DMA engine interprets this as an empty link list and will not perform DMA transfers.

Implication: An Intel® Serial IO controller (i.e. I2C, GSPI, or UART) may stop operating which may cause the system to hang.

Workaround: Driver software should not assign LLP to a 4 GB-aligned address.
Note: This issue has been addressed in the Intel Serial IO drivers in the following versions or later: For Microsoft* Windows* 10, I2C device driver rev 30.100.1724.2, SPI device driver rev 30.100.1725.1, and UART device driver rev 30.100.1725.1

Status: No Fix.

45. xHCI Controller May Delayed Transactions Due to Short Packets Issue

Problem: If the software driver for a device continuously schedules large Transfer Descriptors (TDs) and the device frequently responds with a short packet (defined in the USB specification), the xHCI Host controller may delay service to other device's endpoints.

Implication: The implication is device dependent.

- Full-speed and Low-speed devices with Interrupt IN endpoints connected to the xHCI controller behind a USB 2.0 hub may experience split transaction errors causing the USB 2.0 hub and USB devices behind the hub to be re-enumerated.
- Isochronous devices connected to the xHCI controller may experience dropped packets.
  - Dropped audio or video packets may or may not result in end user detectable impact.
    Note: This issue has been addressed in the Intel Serial IO drivers in the following versions or later: For Microsoft* Windows* 10, I2C device driver rev 30.100.1724.2, SPI device driver rev 30.100.1725.1, and UART device driver rev 30.100.1725.1

Workaround: None.

Status: No Plan to Fix.

46. USB DbC or Device Mode Port When Resuming from Sx/G3 State

Problem: If a PCH USB 3.1 Type-C port is configured in Device Mode (or in DbC mode) and connected to an external USB 3.1 host controller, it may cause the USB port to go into a non-functional state in the following scenarios:

1. The PCH resumes from Sx state, the port may remain in U2.

2. The port is connected to a USB 3.1 Gen1 host controller when resuming from Sx or G3, the port may enter into Compliance Mode or an inactive state if Compliance mode is disabled.
3. The port is connected to a USB 3.1 Gen2 host controller when resuming from Sx or G3, the port may enter an inactive state.

Implication: PCH USB 3.1 Type-C port configured in Device Mode (or in DbC mode) may fail to enumerate or become unavailable.

Workaround: None.

Status: No plan to fix.

47. PCIe Root Port CLKREQ# Asserted Low to Clock Active Timing

Problem: During L1 exit, the PCH PCIe Root Ports may exceed the CLKREQ# asserted low to clock active maximum specification due to PCH PCIe clock un-gate path delays.

Implication: PCIe end point device L1 exit instabilities may be observed.
Note: PCIe end point devices that message LTR latency greater than or equal to 1 µs are not affected by this.

Workaround: None.

- Platforms not supporting S0ix with PCIe end point devices that do not support LTR may disable the associated PCH SRCCLKREQ# signal to keep the PCIe clock active during L1.
- Platforms supporting S0ix with PCIe end point devices that have LTR latencies less than 1 µs may disable the associated PCH SRCCLKREQ# signal to keep the PCIe clock active during L1.

Status: No Fix.

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Specification Changes

There are no Specification Changes in this revision of the Specification Update.

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