Harnessing Highly Parallel Performance: CST Simulations Benefit from Intel® Xeon Phi™ Coprocessors

The computational challenges presented by complex simulations – in manufacturing, scientific research, financial forecasting, 3D imaging, and other fields – can often be met with highly parallel processor architectures and code optimized to dynamically exploit available compute resources. Depending on the nature of the simulation, the feasibility of a given simulation at a specific level of accuracy is largely determined by the time required for completion based on the available resources. Completion times can be shortened in some instances through the selection of an appropriate solver and solver settings. But in other cases the demands of complex modeling, extensive parameter studies, or the massive volumes of mesh cells being processed require compute resources beyond the typical capabilities of a standard workstation computer.

Computer Simulation Technology (CST) designed CST STUDIO SUITE® 2015 with the capabilities to harness available compute resources, achieving performance gains and enhanced simulation times through highly parallel processing. Workloads can effectively be distributed across available processor cores and run concurrently. For certain types of simulations – those adaptable to large-scale parallelism – CST STUDIO SUITE substantially reduces completion times beyond the capabilities of many traditional workstation environments. In systems where Intel® Xeon Phi™ coprocessors are present, the transient solver of CST MICROWAVE STUDIO®, which is the most widely used solver within the CST STUDIO SUITE, can detect and take advantage of the many-core environment, extended vectors, and wider memory bandwidths offered by the coprocessors.

This paper discusses the ways in which Intel Xeon Phi coprocessors complement the efficiency and performance of CST STUDIO SUITE simulations and how they dramatically reduce simulation times.
CST Capitalizes on Intel Xeon Phi Coprocessors

CST specializes in complex software simulations of electromagnetic fields in all frequency bands. With headquarters in Germany and offices around the world, CST has gained a substantial presence in a number of industry sectors, including telecommunications, defense, automotive, electronics, and medical equipment.

The latest release of CST’s flagship product, CST STUDIO SUITE 2015, equips engineers and researchers with an extensive tool set for modeling designs across the electromagnetic spectrum. New tools provided in the latest release include simulations to support development of any type of electromagnetic device. Combining synthesis and simulation capabilities, CST STUDIO SUITE bridges the differences between different simulation domains and diverse fields of engineering, letting users perform tasks beyond electromagnetic field simulation. Simulation tools support product analysis and optimization, while added synthesis capabilities make it easier to select, compare, and create designs.

Individual modules included with CST STUDIO SUITE perform simulations of the following:

- High-frequency devices (antennas, filters)
- Low-frequency electromagnetic devices (motors, transformers)
- Free-moving charged particles (electron guns, cathode ray tubes)
- Signal integrity and analysis of cable harnesses
- Signal integrity and electromagnetic compatibility and interference on printed circuit boards
- Thermal and mechanical stress

As an example of module capabilities, CST MICROWAVE STUDIO provides in-depth insight and analysis into the electromagnetic behavior in high-frequency designs. Engineers designing antennas, filters, couplers, plan and multilayer structures, and electromagnetic compatibility effects can access a Time Domain solver and Frequency Domain solver. A number of additional solvers are also available for addressing specific applications. Figure 1 shows a simulation produced by the Transient solver depicting surface currents excited by an in-vehicle antenna.
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With CST MICROWAVE STUDIO, users can alternately select the Time Domain solver or the Frequency Domain solver, as shown in Figure 2, when working with a simulation model.

![Figure 2. Use of the Time Domain solver and Frequency Domain solver on a single model.](image)

“Our customers are usually starting with workstations and solutions based on the Intel Xeon CPUs, either one- or two-socket systems and then scale up from that point to whatever the need of their specific application is on the hardware side. For example, our main solver has high demand for memory bandwidth. So, in this case the Intel Xeon Phi [coprocessor] helps us tremendously to speed up the performance as compared to a CPU system without a coprocessor. For this reason, we have implemented Intel Xeon Phi support for the latest release of our software.”

- Dr. Felix Wolfheimer, Senior Application Engineer, Manager High Performance Computing, CST

**Intel Xeon Phi Coprocessor Support**

The current version of CST STUDIO SUITE supports a maximum of eight Intel Xeon Phi coprocessors in a single host system. The Intel® MPI Library – with support for the MPI-3 standard – is also bundled with CST STUDIO SUITE 2015, enabling applications to take advantage of the high-performance Message Passing Interface in multiframe environments. CST STUDIO SUITE is also certified as Intel® Cluster Ready, for unlocking optimal parallel performance on preconfigured cluster solutions.

**Benchmarked Comparison of CST Transient Solver**

Transient solver benefits result from the high memory bandwidth and many-core microarchitecture available through the Intel Xeon Phi coprocessor family, producing faster performance than can be achieved in a system with a dual Intel® Xeon® processor E5-2643 v3, as shown in Figure 3.

![Figure 3. Solver performance comparison: Intel® Xeon Phi™ coprocessor 7120X versus a dual Intel® Xeon® processor E5-2643 v3.](image)

For system architects, developers, and decision makers evaluating solutions for high-performance computing (HPC) simulations, CST offers the CST Studio Suite® 2015: Xeon Phi Computing Guide to help configure systems for the optimal results, utilize the full range of cores efficiently, and troubleshoot any problems that might arise.

Intel also provides useful guidelines in the Intel® Xeon Phi™ Coprocessor System Software Developers Guide.
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Fabric Interconnects

Developers and system architects configuring systems for CST STUDIO SUITE simulations can use the native InfiniBand* interconnect, enabling high-speed communication across cluster nodes to boost performance further. Future versions of CST STUDIO SUITE will be able to take advantage of Intel® Omni-Path Architecture, which will be integrated into the Intel Xeon Phi coprocessor, code-named Knights Landing, delivering up to three times the performance of the previous generation coprocessor coupled with more efficient power use.

CST relies strongly on both hardware and software building blocks from Intel to equip applications within the STUDIO SUITE – including, for example, an application that provides mobile phone development simulations – with optimal performance on each target platform. As a part of its long-term relationship with Intel, to ensure that produced code is capable of exploiting upcoming technology advances on the Intel’s processor-based HPC platform, CST is embracing Modern Code techniques to take full advantage of the evolving HPC platform. For example, optimizations made for today’s Intel Xeon Phi coprocessor will apply to Knights Landing with a simple recompile. Additional functionality and technology advances will also be available through incremental tuning.

Establishing a Supercomputer Legacy: the Intel Xeon Phi Coprocessor

The Intel Xeon Phi coprocessor works in tandem with the Intel® Xeon® processor family to deliver supercomputer and high-performance computing capabilities for applications where extreme levels of parallelism are desirable. The coprocessor advantages aren’t directly applicable to more linear-oriented applications, but in those approximately 10–20 percent of applications that involve highly parallel operations – primarily in the scientific, medical, and financial sectors – performance boosts are substantial.

Supercomputing Leadership

Supercomputing innovation from Intel is evident in many of the highest performing systems in the world, including the Milky Way 2* in China, which achieves 35 petaflops on a system powered by current-generation Intel Xeon processors and Intel Xeon Phi coprocessors. Globally, Intel Xeon Phi coprocessors can be found in over 200 OEM designs, and Intel processor-based systems represent 85 percent of the supercomputer systems listed in the latest TOP500* ratings.

Forward-Looking Programming

With the Intel Xeon Phi coprocessor, developers can code optimized applications that scale to future versions of the coprocessor, as well as upcoming Intel Xeon processor generations that will feature highly parallel architectures. This enables applications to automatically take advantage of advanced hardware resources and additional processing cores as they are introduced into a system.

Because Intel Xeon Phi coprocessors fully support the x86 instruction set (as well as being binary compatible with the Intel Xeon processor), developers have access to extensive libraries and an enormous volume of software and can tap into expertise gained over many years of development history (extending as far back as the Intel® 8008 processor). Development projects can take advantage of a large and growing vendor ecosystem. The Intel® Xeon Phi™ Coprocessor Applications and Solutions Catalog offers a window into optimized, ported, and downloadable software, as well as news and insights into the latest developments across the software communities. Intel® Xeon Phi™ Coprocessor Proof Points illustrates the performance increases that have been achieved in key business sectors.

Using Modern Code techniques, developers can achieve performance breakthroughs with code that runs faster, using techniques that have been tested and benchmarked for successful results. Proven, standard-based development applications, such as Intel® Parallel Studio XE 2016, break down barriers to parallel coding, making it faster and easier to optimize programs for the Intel Xeon Phi coprocessor and to perform explicit vector programming.

Using Solid-State Drives to Optimize System Architecture Performance

Performance-driven applications, such as the simulation solutions that CST offers, clearly benefit from the advantages of massive parallelism. To further maximize performance, end-to-end optimizations across the system architecture can often identify areas where additional gains can be achieved. Network and system storage are two areas where the Intel® Solid-State Drive Data Center (Intel® SSD DC) Family provides a means to minimize data access latency, lower power requirements, and eliminate performance bottlenecks.

A new generation of data center class Intel SSDs, tested against data center workloads, is well suited to the type of large-scale concurrency supported by CST STUDIO SUITE and the Intel Xeon Phi coprocessor. The Intel SSD DC Family for Non-Volatile Memory Express* (NVMe) delivers outstanding performance, with 4 KB random read performance of up to 460,000 IOPS and 4 KB random write performance of up to 175,000 IOPS.* Excellent quality of service – less than 120 microseconds for 99 percent reads of Intel SSD DC P3700 Series – ensures quick, consistent command response times.
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With PCIe® Gen3 support and a NVMe queuing interface, the SSD delivers excellent sequential read performance of up to 2.8 GB/s and sequential write speeds of up to 2.0 GB/s depending on the drive capacity. The optimized NVMe command stack minimizes the number of processor cycles, improving drive efficiency for high-performance data solutions.

The Value of Intel® Many Integrated Core Architecture

Intel® Many Integrated Core Architecture (Intel® MIC Architecture) is characterized by the integration of large numbers of Intel® processor cores onto a single chip. Intel MIC products run in standard programming environments using familiar tools and methods. Developers can compile and run code written for Intel MIC products on systems powered by the Intel Xeon processor. The advent of Intel MIC Architecture heralded a new era of supercomputing speed, performance, and compatibility that has gained rapid acceptance for HPC applications throughout the industry. Within 18 months following the introduction of the Intel Xeon Phi coprocessors, systems based on this product constituted 18 percent of the aggregated performance of all TOP500 supercomputers.

Highly parallel applications are appearing in a number of different industry segments and the techniques for achieving high performance through parallelism are increasingly becoming more sophisticated and refined. Expertise and experience from three prior Intel research initiatives provided the framework for developing the Intel Xeon Phi coprocessor, drawing on work done in the 80-core Tera-Scale Computing Research Program, the Single-Chip Cloud Computer initiative, and the Many-Core Visual Computing Project (code-named Larrabee).

The resulting Intel MIC Architecture supports a high degree of parallelism using smaller, power-efficient processor cores. The upcoming release of the Intel Xeon Phi coprocessor, code-named Knights Landing, will feature more than 60 HPC-enhanced code-named Silvermont architecture-based cores and has a projected double-precision performance level of 3 teraflops.6

Used as a standalone server processor, support for DDR4 system memory will be equivalent—in terms of capacity and bandwidth—to Intel Xeon processor-based platforms, yielding a much larger memory footprint for applications.

Summary

Intel Xeon Phi coprocessors enable a direct, accessible pathway for unlocking the opportunities of massive-scale parallelism using familiar x86 instruction sets and Intel® Software Development tools and libraries.

CST STUDIO SUITE provides a perfect example of the results that can be achieved when applications tap into the power of many cores to enhance computer simulations and substantially reduce simulation times. Through co-engineering with Intel, CST has developed a future-proofed application—optimized for scalable multithreaded performance—with a means of harnessing available processing cores as they come on line. CST STUDIO SUITE has become the professional tool of choice for advanced electromagnetic simulations and design projects, largely due to the flexibility of taking full advantage of system resources and the ease with which solver operations can be distributed across cores of clusters.

The Intel Xeon Phi coprocessor and the CST STUDIO SUITE offer a straightforward path to advanced electromagnetic simulations that can scale effortlessly as additional coprocessors are installed in a system.

Learn more

System architects, developers, software engineers, and decision makers tasked with HPC responsibilities are invited to explore the ways in which Intel Xeon Phi coprocessor products can enhance performance for highly parallel workloads and support demanding applications in science, finance, manufacturing, and the life sciences.

The Modern Code developer community offers a number of resources to take maximum advantage of parallelism, including guidelines for mastering parallelism, how-to guides, forums staffed by parallel programming experts, training webinars, productivity tools, remote access to Intel Xeon processor and Intel Xeon Phi coprocessor-based clusters, and more. Visit the online community at software.intel.com/moderncode.

To learn more about HPC simulations with CST STUDIO SUITE 2015, visit www.cst.com/Products/HPC. CST STUDIO SUITE can also be accessed on the systems of select HPC cloud partners; for details visit www.cst.com/cloud.
“Parallel computing is fundamental for attacking the really big problems in science and engineering.”

— Jay Boisseau, Director, Texas Advanced Computing Center, University of Texas at Austin

LEARN MORE ABOUT DEVELOPING FOR THE INTEL XEON PHI COPROCESSOR:
http://software.intel.com/mic-developer/

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1 Test Setup Configuration Details: OS=CentOS7, RAM=256GB DDR4@1866 GHz, Disks=Standard SATA2 disks in RAID 5 configuration, Network=1Gb Ethernet/FDR Infiniband
3 Ibid.
5 Ibid.
6 Ibid.
7 Internal and preliminary projections of theoretical double-precision performance measured by Linpack*. Based on current expectations of Knights Landing’s cores, clock frequency and floating point operations per cycle.
9 Ibid.

Intel technologies’ features and benefits depend on system configuration and may require enabled hardware, software or service activation. Performance varies depending on system configuration. Check with your system manufacturer or retailer or learn more at intel.com INTEGRATING TECHNOLOGY IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL’S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. UNLESS OTHERWISE AGREED IN WRITING BY INTEL, THE INTEL PRODUCTS ARE NOT DESIGNED NOR INTENDED FOR ANY APPLICATION IN WHICH THE FAILURE OF THE INTEL PRODUCT COULD CREATE A SITUATION WHERE PERSONAL INJURY OR DEATH MAY OCCUR. Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked “reserved” or “undefined.” Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information. The products described in this document may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are available on request. Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order. Copies of documents, which have an order number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725, or by visiting Intel’s Web site at www.intel.com. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to http://www.intel.com/performance Relative performance is calculated by assigning a baseline value of 1.0 to one benchmark result, and then dividing the actual benchmark result for the baseline platform into each of the specific benchmark results of each of the other platforms, and assigning them a relative performance number that correlates with the performance improvements reported. Intel does not control or audit the design or implementation of third party benchmarks or Web sites referenced in this document. Intel encourages all of its customers to visit the referenced Web sites or others where similar performance benchmarks are reported and confirm whether the referenced benchmarks are accurate and reflect performance of systems available for purchase. Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor series, not across different processor sequences. See http://www.intel.com/products/processor_number for details. Intel products are not intended for use in medical, life saving, critical control or safety systems, or in nuclear facility applications. All dates and products specified are for planning purposes only and are subject to change without notice Intel product plans in this presentation do not constitute Intel plan of record product roadmaps. Please contact your Intel representative to obtain Intel’s current plan of record product roadmaps. Product plans, dates, and specifications are preliminary and subject to change without notice. Any difference in system hardware or software design or configuration may affect actual performance Copyright © 2015 Intel Corporation. All rights reserved. Intel, the Intel logo, Xeon, Xeon logo, Xeon Phi, and Xeon Phi logo are trademarks of Intel Corporation in the U.S. and/or other countries. All dates and products specified are for planning purposes only and are subject to change without notice. *Other names and brands may be claimed as the property of others. Copyright © 2015 Intel Corporation. All rights reserved. Intel, the Intel logo, Intel Xeon Phi, and Xeon are trademarks of Intel Corporation in the U.S. and other countries.