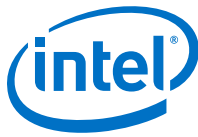


Intel® Communications Chipset 89xx Series

Thermal Mechanical Design Guide

October 2012



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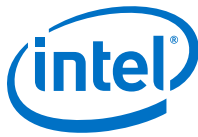
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Revision History

Date	Revision	Description
October 2012	001	Initial release

1.0 Introduction

Power dissipation requirements for electronic components have risen with the increase in complexity of computer systems. To ensure quality, reliability, and performance goals are met over a product's life cycle, the heat generated by the component must be properly dissipated. Typical methods to improve heat dissipation include selective use of airflow ducting, and/or the use of heatsinks.

The goals of this document are to:

- Describe the thermal and mechanical specifications for the Intel® Communications Chipset 89xx Series.
- Describe reference solutions that meet the thermal and mechanical specifications of the Intel® Communications Chipset 89xx Series.

A properly designed thermal solution adequately cools the device die temperature at or below the thermal specification. This is accomplished by providing a suitable local-ambient temperature, ensuring adequate local airflow, and minimizing the die to local-ambient thermal resistance. Operation outside the functional limits can degrade system performance and may cause permanent changes in the operating characteristics of the component.

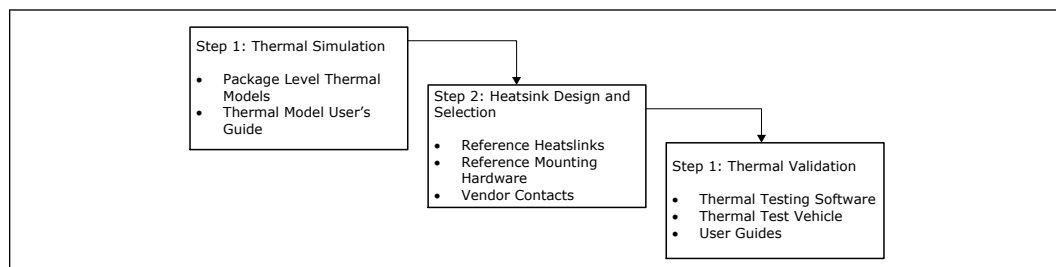
This document addresses thermal and mechanical design specifications for the Intel® Communications Chipset 89xx Series only. For thermal design information about other Intel® components, refer to the respective component's thermal design guide.

Note: Unless otherwise specified, the term PCH refers to the Intel® Communications Chipset 89xx Series.

1.1 Design Flow

Several tools are available from Intel to assist in the development of a reliable, cost-effective thermal solution. The figure below illustrates a typical thermal solution design process with available tools noted. The tools are available through your local Intel field sales representative.

Figure 1. Thermal Design Process





1.2 Definition of Terms

Table 1. Terms

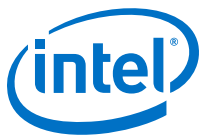
This table defines terms that are used throughout this document.

Term	Definition
FC-BGA	Flip Chip Ball Grid Array. A package type defined by a plastic substrate where a die is mounted using an underfill C4 (Controlled Collapse Chip Connection) attach style. The primary electrical interface is an array of solder balls attached to the substrate opposite the die. <i>Note:</i> The device arrives at the customer with solder balls attached.
DTS	Digital Thermal Sensor. The sensors are built into the die and monitor die temperature on the package.
PCH	Platform Controller Hub
PECI	The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices.
TDP	Thermal Design Power. Target power dissipation level for thermal solution design. TDP is based on worst-case real world applications and benchmarks at maximum component temperature. TDP is not theoretical maximum power.
TIM	Thermal Interface Material: thermally conductive material installed between two surfaces to improve heat transfer and reduce interface contact resistance.
T_{JUNCTION}	The temperature of the die. This temperature is measured using the DTS present on the die. Also referred to as T_J .
$T_{\text{JUNCTION-MAX}}$	Maximum allowed die temperature. This temperature is measured using the DTS present on the die. Also referred to as $T_{J\text{-MAX}}$.
T_{LA}	Local ambient temperature. This is the temperature measured inside the chassis, approximately 1" upstream of a component heatsink. Also referred to as T_A .
T_{SINK}	Temperature measured at the geometric center of the bottom surface of the heatsink base. Also referred to as T_S .
Ψ_{JA}	Junction-to-ambient thermal characterization parameter. A measure of the thermal solution thermal performance using the total package power. Defined as $(T_{\text{JUNCTION}} - T_{\text{LA}}) / \text{Total Package Power}$. <i>Note:</i> Heat source must be specified for Ψ measurements.
Ψ_{SA}	Sink-to-ambient thermal characterization parameter. A measure of the heat sink thermal performance using the total package power. Defined as $(T_S - T_{\text{LA}}) / \text{Total Package Power}$. <i>Note:</i> Heat source must be specified for Ψ measurements.
Ψ_{JS}	Junction-to-sink thermal characterization parameter. A measure of the thermal interface material performance using the total package power. Defined as $(T_{\text{JUNCTION}} - T_S) / \text{Total Package Power}$. <i>Note:</i> Heat source must be specified for Ψ measurements.

1.3 Reference Documents

Table 2. Reference Documents

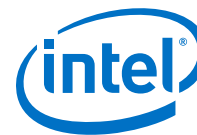
Document	Document Number / Location
Intel® Communications Chipset 89xx Series Datasheet	327879
<i>continued...</i>	



Document	Document Number / Location
<i>Intel® Communications Chipset 89xx Series Specification Update</i>	328000
<i>Intel® Xeon® and Intel® Core™ Processors For Communications Infrastructure Thermal/Mechanical Design Guide</i>	327397
<i>RS - VR12/IMVP7 SVID Protocol Design Guide</i>	
<i>RS - VR12/IMVP7 Pulse Width Modulation (PWM) Specification</i>	
<i>RS - Platform Environment Control Interface (PECI) Specification</i>	
Server Systems Infrastructure (SSI) - Thin Electronics Bay Specifications	http://ssiforum.org
PICMG Specifications (AdvancedTCA, AdvancedMC, etc.)	http://www.picmg.org
Form Factor Specifications (Motherboard, Power Supply, Riser, etc.)	http://www.formfactors.org

1.4 Package Thermal Models

Intel provides device thermal simulation models and a thermal model user's guide to aid designers in simulating, analyzing, and optimizing thermal solutions in an integrated, system-level environment. The models are for use with commercially available Computational Fluid Dynamics (CFD)-based thermal analysis tools including Flotherm* by Mentor Graphics, Inc. or Icepak* by Ansys, Inc. Contact your Intel representative to order the thermal models and associated user's guides.



2.0 Package Information

The Intel® Communications Chipset 89xx Series utilizes a 27 x 27 mm, FC-BGA package as shown in the figure below. The data in this chapter is provided for reference purposes only. Dimensions are in millimeters with inches in square brackets []. The dimensions are preliminary and are subject to change. See the *Intel® Communications Chipset 89xx Series Datasheet* for current data. In the event of a conflict, the product datasheet supersedes the data shown in this figure.



TOP VIEW

Dimensions: B_1 , B_2 , C_1 , C_2 , A_1 , A_2 , G_1 , G_2 , H , E , D , C , B , A

Callouts: SEE DETAIL B, SEE DETAIL C, SEE DETAIL D, 3X SURFACE MARK ZONE, DIE, SUBSTRATE, 0.6 MAX ALLOWABLE COMPONENT HEIGHT, 2X 2.5, 4X 2.5, 2X 3, 4X 2.5, 2X 3, 0.203, 0.254, 0.508, 0.762, 1.016, 1.27, 1.52, 1.78, 2.03, 2.29, 2.54, 2.79, 3.05, 3.3, 3.55, 3.81, 4.06, 4.32, 4.57, 4.83, 5.08, 5.33, 5.59, 5.84, 6.1, 6.35, 6.6, 6.86, 7.12, 7.37, 7.62, 7.87, 8.13, 8.38, 8.63, 8.89, 9.14, 9.39, 9.65, 9.9, 10.16, 10.41, 10.67, 10.92, 11.18, 11.43, 11.68, 11.93, 12.19, 12.44, 12.69, 12.95, 13.2, 13.45, 13.71, 13.96, 14.21, 14.47, 14.72, 14.97, 15.23, 15.48, 15.73, 15.98, 16.24, 16.49, 16.74, 17, 17.26, 17.51, 17.76, 18.02, 18.27, 18.52, 18.78, 19.03, 19.28, 19.53, 19.79, 20.04, 20.29, 20.54, 20.8, 21.05, 21.3, 21.56, 21.81, 22.07, 22.32, 22.57, 22.83, 23.08, 23.33, 23.59, 23.84, 24.09, 24.34, 24.6, 24.85, 25.1, 25.36, 25.61, 25.87, 26.12, 26.37, 26.62, 26.88, 27.13, 27.38, 27.63, 27.89, 28.14, 28.39, 28.64, 28.9, 29.15, 29.4, 29.66, 29.91, 30.16, 30.42, 30.67, 30.92, 31.17, 31.43, 31.68, 31.93, 32.18, 32.43, 32.69, 32.94, 33.19, 33.44, 33.7, 33.95, 34.2, 34.46, 34.71, 34.96, 35.22, 35.47, 35.72, 35.97, 36.23, 36.48, 36.73, 36.98, 37.24, 37.49, 37.74, 38, 38.26, 38.51, 38.76, 39.02, 39.27, 39.52, 39.77, 40.03, 40.28, 40.53, 40.78, 41.04, 41.29, 41.54, 41.8, 42.05, 42.3, 42.56, 42.81, 43.07, 43.32, 43.57, 43.82, 44.08, 44.33, 44.58, 44.84, 45.09, 45.34, 45.6, 45.85, 46.1, 46.36, 46.61, 46.86, 47.12, 47.37, 47.62, 47.87, 48.13, 48.38, 48.63, 48.88, 49.14, 49.39, 49.64, 49.9, 50.15, 50.41, 50.66, 50.91, 51.17, 51.42, 51.67, 51.92, 52.18, 52.43, 52.68, 52.93, 53.19, 53.44, 53.69, 53.94, 54.2, 54.45, 54.7, 54.96, 55.21, 55.47, 55.72, 55.97, 56.23, 56.48, 56.73, 56.98, 57.24, 57.49, 57.74, 58, 58.26, 58.51, 58.76, 59.02, 59.27, 59.52, 59.77, 60.03, 60.28, 60.53, 60.78, 61.04, 61.29, 61.54, 61.8, 62.05, 62.3, 62.56, 62.81, 63.07, 63.32, 63.57, 63.82, 64.08, 64.33, 64.58, 64.84, 65.09, 65.34, 65.6, 65.85, 66.1, 66.36, 66.61, 66.86, 67.12, 67.37, 67.62, 67.87, 68.13, 68.38, 68.63, 68.88, 69.14, 69.39, 69.64, 69.9, 70.15, 70.41, 70.66, 70.91, 71.17, 71.42, 71.67, 71.92, 72.18, 72.43, 72.68, 72.93, 73.19, 73.44, 73.69, 73.94, 74.2, 74.45, 74.7, 74.96, 75.21, 75.47, 75.72, 75.97, 76.23, 76.48, 76.73, 76.98, 77.24, 77.49, 77.74, 78, 78.26, 78.51, 78.76, 79.02, 79.27, 79.52, 79.77, 80.03, 80.28, 80.53, 80.78, 81.04, 81.29, 81.54, 81.8, 82.05, 82.3, 82.56, 82.81, 83.07, 83.32, 83.57, 83.82, 84.08, 84.33, 84.58, 84.84, 85.09, 85.34, 85.6, 85.85, 86.1, 86.36, 86.61, 86.86, 87.12, 87.37, 87.62, 87.87, 88.13, 88.38, 88.63, 88.88, 89.14, 89.39, 89.64, 89.9, 90.15, 90.41, 90.66, 90.91, 91.17, 91.42, 91.67, 91.92, 92.18, 92.43, 92.68, 92.93, 93.19, 93.44, 93.69, 93.94, 94.2, 94.45, 94.7, 94.96, 95.21, 95.47, 95.72, 95.97, 96.23, 96.48, 96.73, 96.98, 97.24, 97.49, 97.74, 98, 98.26, 98.51, 98.76, 99.02, 99.27, 99.52, 99.77, 100.03, 100.28, 100.53, 100.78, 101.04, 101.29, 101.54, 101.8, 102.05, 102.3, 102.56, 102.81, 103.07, 103.32, 103.57, 103.82, 104.08, 104.33, 104.58, 104.84, 105.09, 105.34, 105.6, 105.85, 106.1, 106.36, 106.61, 106.86, 107.12, 107.37, 107.62, 107.87, 108.13, 108.38, 108.63, 108.88, 109.14, 109.39, 109.64, 109.9, 110.15, 110.41, 110.66, 110.91, 111.17, 111.42, 111.67, 111.92, 112.18, 112.43, 112.68, 112.93, 113.19, 113.44, 113.69, 113.94, 114.2, 114.45, 114.7, 114.96, 115.21, 115.47, 115.72, 115.97, 116.23, 116.48, 116.73, 116.98, 117.24, 117.49, 117.74, 118, 118.26, 118.51, 118.76, 119.02, 119.27, 119.52, 119.77, 120.03, 120.28, 120.53, 120.78, 121.04, 121.29, 121.54, 121.8, 122.05, 122.3, 122.56, 122.81, 123.07, 123.32, 123.57, 123.82, 124.08, 124.33, 124.58, 124.84, 125.09, 125.34, 125.6, 125.85, 126.1, 126.36, 126.61, 126.86, 127.12, 127.37, 127.62, 127.87, 128.13, 128.38, 128.63, 128.88, 129.14, 129.39, 129.64, 129.9, 130.15, 130.41, 130.66, 130.91, 131.17, 131.42, 131.67, 131.92, 132.18, 132.43, 132.68, 132.93, 133.19, 133.44, 133.69, 133.94, 134.2, 134.45, 134.7, 134.96, 135.21, 135.47, 135.72, 135.97, 136.23, 136.48, 136.73, 136.98, 1

TOP VIEW

Dimensions: B_1 , A , (C_1) , B_2 , (C_2) , $2X .3$, $4X 2.5$, $4X 2.5$, $6.6 \text{ MAX ALLOWABLE COMPONENT HEIGHT}$, $2X .3$, $PIN \#1$

FRONT VIEW

Dimensions: D , C , 0.203

BOTTOM VIEW

Dimensions: H , G_1 , G_2 , G_1

DETAIL A
SUBSTRATE ALIGNMENT FIDUCIAL
SCALE 30
 $\phi 0.54 \pm 0.05$ (SOLDER RESIST OPENING)

DETAIL B
SUBSTRATE ALIGNMENT FIDUCIAL
SCALE 30
 $\phi 0.40 \pm 0.05$ (SOLDER RESIST OPENING)

DETAIL C
BGA LAND PITCH
SCALE 75
 $\phi 0.43 \pm 0.015$ (SOLDER RESIST OPENING)

DETAIL D
SUBSTRATE ALIGNMENT FIDUCIAL
SCALE 30
 $\phi 0.35 \pm 0.05$ (SOLDER RESIST OPENING)

SYMBOL	MILLIMETERS	COMMENTS
B_1	27 ± 0.04	
B_2	27 ± 0.04	
C_1	9.778	
C_2	9.423	
A	1.882 ± 0.086	
A_1	0.292 ± 0.082	PRE-SMT
A_2	0.214 ± 0.06	POST-SMT
G_1	1.063 ± 0.09	
G_2	0.485	BGA PAD CENTER TO PACKAGE EDGE
H	0.485	BGA PAD CENTER TO PACKAGE EDGE
H	0.7	MIN PITCH FOR BGA LAND PITCH PATTERN
b	0.45 ± 0.065	PRE-SMT BGA DIAMETER

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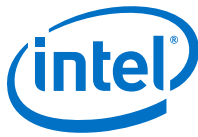
DESIGNED BY: DATE: CHECKED BY: DATE: APPROVED BY: DATE: MATERIAL: FINISH: SCALE: 5:1

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PACKAGE MECHANICAL DRAWING

SIZE: DRAWING NUMBER: 85967 KEY: A1

SHEET 1 OF 1



3.0 Thermal Specifications

The Intel® Communications Chipset 89xx Series requires a thermal solution to maintain temperatures within its operating limits. Any attempt to operate the PCH outside these operating limits may result in permanent damage to the component. Maintaining the proper thermal environment is key to reliable, long-term system operation. A complete solution includes both component and system level thermal management features.

Component level thermal solutions can include active or passive heatsinks attached to the PCH die.

3.1 Thermal Design Power

[Maximum Allowed Component Temperature](#) on page 12 lists the Thermal Design Power (TDP) specifications. TDP is the recommended design point for thermal solution power dissipation. TDP is based on running worst-case, real-world applications and benchmarks at maximum component temperature. TDP is not the absolute worst case power. It could, for example, be exceeded under a synthetic worst case condition or under short power spikes. The thermal solution design must keep the components' maximum temperature within specification while dissipating TDP.

Heat transfer through the FC-BGA package and into the baseboard is limited. The cooling capacity without a thermal solution is also limited, so Intel recommends the use of a heatsink for all usage conditions.

3.2 Maximum Allowed Component Temperature

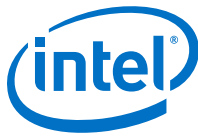
The Intel® Communications Chipset 89xx Series must maintain a maximum temperature at or below the value specified in the table below. The thermal solution is required to meet the temperatures specification while dissipating the Thermal Design Power. [Thermal Metrology](#) on page 24 includes guidelines for accurately measuring the package temperature.

Table 3. Intel® Communications Chipset 89xx Series Thermal Design Power (TDP) and Temperature Specification

Devices	SKU 1	SKU 2: Entry Level	SKU 3: Mid Performance	SKU 4: Max Performance
PCIe Endpoint	x4	x4	x8	x16
GbE	4	4	4	4
SATA	2	2	2	2
USB	6	6	6	6
Symmetric Cryptographic Functions	N	Y	Y	Y
Public Key Functions	N	Y	Y	Y
continued...				



Devices	SKU 1	SKU 2: Entry Level	SKU 3: Mid Performance	SKU 4: Max Performance
Compression/Decompression	N	Y	Y	Y
Pattern Matching	N	Y	Y	Y
Normal Mode TDP (W) ^{1, 2}	8.5	9.5	11	12
End Point Mode TDP ^{1, 2}	5.7	6.7	8.2	9.2
Non-End Point Mode TDP ^{1, 2}	2.8	2.8	2.8	2.8
T _{JUNCTION-MAX} (°C)	103	103	103	103
T _{JUNCTION-MIN} (°C)	0	0	0	0
Notes: 1. TDP values are B0 pre-silicon estimates and are subject to change. 2. See the <i>Intel® Communications Chipset 89xx Series Datasheet</i> for definition of the various modes for the chipset.				



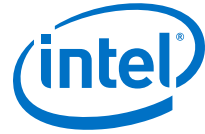
4.0 Mechanical Specifications

4.1 Package Mechanical Requirements

The FC-BGA package for the Intel® Communications Chipset 89xx Series is a bare die package and will be in direct contact with the thermal solution. The maximum allowable static force for the bare die package is 15 lbf normal to the die. Any force greater than this could damage the device.

4.2 Board Level Keep Out Zone Requirements

A general description of the keep-out zones and mounting hole pattern for the reference thermal solutions are shown in [Mechanical Drawings](#) on page 29. When using heatsinks that extend beyond the reference heatsink envelopes shown in [Mechanical Drawings](#) on page 29, motherboard components placed between the underside of the heatsink and the motherboard cannot exceed 1.75 mm [0.07 in] in height.



5.0 Thermal Solution Requirements

5.1 Heatsink Design Considerations

To dissipate the heat from the Intel® Communications Chipset 89xx Series, three basic parameters should be considered.

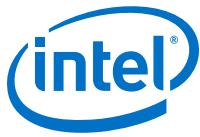
1. **The area of the surface on which the heat transfer takes place.** Without any enhancements, this is the surface of the die. One method to improve thermal performance is to attach a heatsink to the die. A heatsink increases the effective heat transfer surface area by conducting heat out of the die and into the surrounding air through fins attached to the heatsink base.

Note: The Intel® Communications Chipset 89xx Series requires a heatsink in all applications.

2. **The conduction path from the heat source to the heatsink fins.** Providing a direct conduction path from the heat source to the heatsink fins and selecting materials with higher thermal conductivity typically improves heatsink performance. The length, thickness, and conductivity of the conduction path from the heat source to the fins directly impact the thermal performance of the heatsink. In particular, the quality of the contact between the package die and the heatsink base has a higher impact on the overall thermal solution performance as PCH cooling requirements become stricter. Thermal interface material (TIM) is used to fill the gap between the die and the bottom surface of the heatsink, and thereby improve the overall performance of the stack-up (die-TIM-heatsink). With extremely poor heatsink interface flatness or roughness, TIM may not adequately fill the gap. The TIM thermal performance depends on its thermal conductivity as well as the pressure applied to it. See [Thermal Interface Material \(TIM\)](#) on page 23 for more information about TIM and about bond-line management between the die and the heatsink base.
3. **The heat transfer conditions on the surface on which heat transfer takes place.** Convective heat transfer occurs between the airflow and the surface exposed to the flow. It is characterized by the local ambient temperature of the air, T_{LA} , and the local air velocity over the surface. The higher the air velocity over the surface and the cooler the air, the more efficient is the resulting cooling. The nature of the airflow can also enhance heat transfer via convection. Turbulent flow can provide improvement over laminar flow. In the case of a heatsink, the surface exposed to the flow includes in particular the fin faces and the heatsink base.

Active heatsinks typically incorporate a fan that helps manage the airflow through the heatsink.

Passive heatsink solutions require in-depth knowledge of the airflow in the chassis. Typically, passive heatsinks see lower air speed. These heatsinks are therefore usually larger (and heavier) than active heatsinks due to the increase in the fin surface required to meet the required performance. As the heatsink fin density (the number of fins in a given cross-section) increases, the resistance to the airflow increases: it is



more likely that the air travels around the heatsink instead of through it, unless air bypass is carefully managed. Using air-ducting techniques to manage the bypass area can be an effective method for controlling airflow through the heatsink.

5.1.1 Heatsink Size

The size of the heatsink is dictated by height restrictions for installation in a system and by the space available on the motherboard and other considerations for component height and placement in the area potentially impacted by the heatsink. The height of the heatsink must comply with the requirements and recommendations published for the motherboard form factor of interest. See the form factor specifications for height restrictions. Links to some of these specifications are listed in [Reference Documents](#) on page 7. Reference thermal solutions keep-out zones for multiple form factors are shown in [Mechanical Drawings](#) on page 29.

The resulting space available above the motherboard is generally not entirely available for the heatsink. The target height of the heatsink must take into account airflow considerations (for fan performance for example) as well as other design considerations (air duct, etc.).

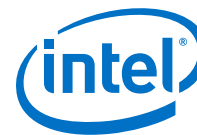
5.1.2 Heatsink Mass

With the need to increase air cooling to improve performance, heatsink solutions tend to grow larger (increase in fin surface) resulting in increased weight. The insertion of highly thermally conductive materials, like copper, to increase heatsink thermal conduction performance results in even heavier solutions. The heatsink weight must consider the package load limits, the heatsink attach mechanical capabilities, and the mechanical shock and vibration profile targets. Beyond a certain heatsink weight, the cost of developing and implementing a heatsink attach mechanism that can ensure system integrity under mechanical shock and vibration profile targets may become prohibitive.

5.1.3 System Level Thermal Solution Considerations

The heat generated by components within the chassis must be removed to provide an adequate operating environment for the processor and other components. Moving air through the chassis brings in air from the external ambient environment and removes the heat generated by the Intel® Communications Chipset 89xx Series and other components. The number, size, and relative position of fans and vents determine the chassis thermal performance, and the resulting ambient temperature around the processor. The size and type (passive or active) of the thermal solution and the amount of system airflow can be traded off against each other to meet specific system design constraints. Additional constraints are board layout, spacing, component placement, acoustic requirements, and structural considerations that limit the thermal solution size. For more information, see the appropriate form factor's thermal design suggestions.

In addition to passive heatsinks, fan heatsinks, and system fans, other solutions exist for cooling integrated circuit devices. For example, ducted blowers, heat pipes and liquid cooling are all capable of dissipating additional heat. Due to their varying attributes, each of these solutions may be appropriate for a particular system implementation.



To develop a reliable, cost-effective thermal solution, thermal characterization and simulation should be carried out at the system level, accounting for the thermal requirements of each component. In addition, acoustic noise constraints may limit the size, number, placement, and types of fans that can be used in a particular design.

5.2 Characterizing the Thermal Solution Requirement

The idea of a “thermal characterization parameter”, Ψ (Greek letter Psi), is a convenient way to characterize the performance needed for the thermal solution and to compare thermal solutions in identical situations (i.e. heating source, local ambient conditions, etc.). The thermal characterization parameter is calculated using total package power, whereas actual thermal resistance, Θ (theta), is calculated using actual power dissipated between two points. Measuring actual power dissipated into the heatsink is difficult, since some of the power is dissipated via heat transfer into the package and the board.

The junction-to-local ambient thermal characterization parameter (Ψ_{JA}) is used as a measure of the thermal performance of the overall thermal solution. Ψ_{JA} is measured in units of °C/W and defined by the following equation:

Figure 4. Junction-to-Local Ambient Thermal Characterization Parameter (Ψ_{JA})

$$\Psi_{JA} = \frac{T_{JUNCTION} - T_{LA}}{TDP}$$

The junction-to-local ambient thermal characterization parameter, Ψ_{JA} , is comprised of Ψ_{JS} , the thermal interface material thermal characterization parameter, and of Ψ_{SA} , the sink-to-local ambient thermal characterization parameter. Ψ_{JA} is defined by the following equation:

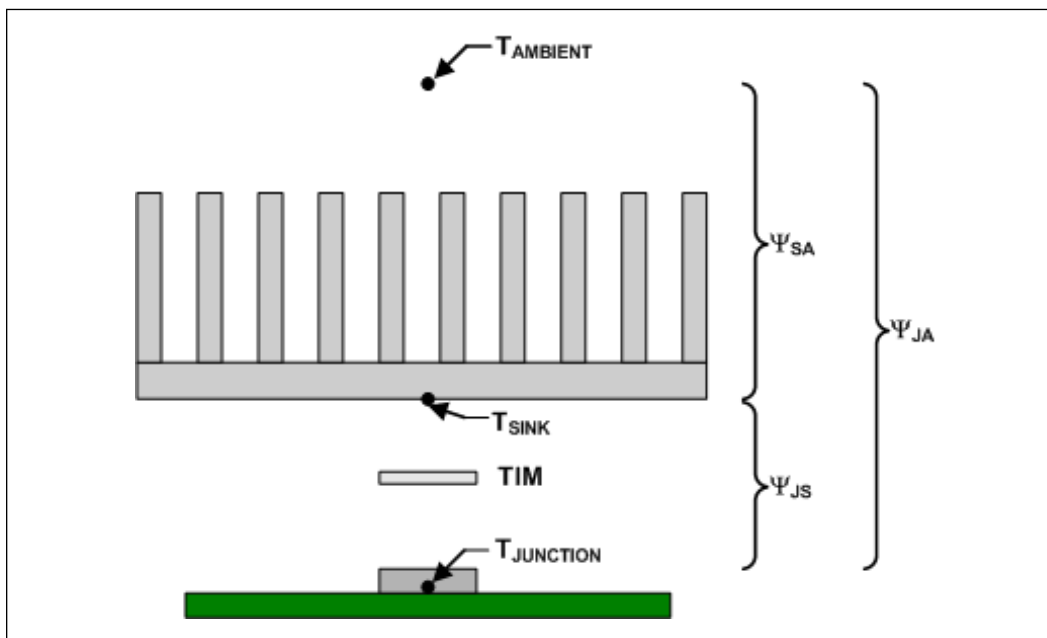
Figure 5. Junction-to-Local Ambient Thermal Characterization Parameter

$$\Psi_{JA} = \Psi_{JS} + \Psi_{SA}$$

Ψ_{JS} is strongly dependent on the thermal conductivity and thickness of the TIM between the heatsink and device package.

Ψ_{SA} is a measure of the thermal characterization parameter from the bottom of the heatsink to the local ambient air. Ψ_{SA} is dependent on the heatsink material, thermal conductivity, and geometry. Ψ_{SA} is also strongly dependent on the air velocity through the fins of the heatsink. The figure below illustrates the combination of the different thermal characterization parameters.

Figure 6. Processor Thermal Characterization Parameter Relationship



5.2.1 Example Calculating the Required Thermal Performance

The cooling performance, Ψ_{JA} , is defined using the thermal characterization parameter previously described. The process to determine the required thermal performance to cool the device includes:

Define a target component temperature $T_{JUNCTION}$ and corresponding TDP.

Define a target local ambient temperature, T_{LA} .

Use [Figure 4](#) on page 17 and [Figure 5](#) on page 17 to determine the required thermal performance needed to cool the device.

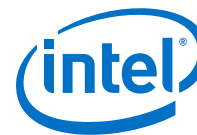
Note: The following example illustrates how to calculate the thermal resistance. The TDP and $T_{JUNCTION-MAX}$ used in the example may not be the actual specifications of the device. See the *Intel® Communications Chipset 89xx Series Datasheet* for actual power and temperature specifications.

Assume:

- TDP = 8 W and $T_{JUNCTION-MAX} = 103\text{ }^{\circ}\text{C}$
- Local processor ambient temperature, $T_{LA} = 60^{\circ}\text{C}$.

Then the following could be calculated using [Figure 4](#) on page 17 for the given processor frequency:

$$\Psi_{JA} = \frac{T_{JUNCTION-MAX} - T_{LA}}{TDP} = \frac{103 - 60}{8} = 5.375\text{ }^{\circ}\text{C/W}$$



To determine the required heatsink performance, a heatsink solution provider would need to determine Ψ_{JS} performance for the selected TIM and mechanical load configuration. If the heatsink solution were designed to work with a TIM material performing at $\Psi_{JS} \leq 0.5$ °C/W, solving for Ψ_{SA} from [Figure 5](#) on page 17, the performance needed from the heatsink is:

$$\Psi_{SA} = \Psi_{JA} - \Psi_{JS} = 5.375 - 0.5 = 4.875^{\circ}\text{C/W}$$

If the local ambient temperature is relaxed to 40°C, the same calculation can be carried out to determine the new junction-to-ambient thermal resistance:

$$\Psi_{JA} = \frac{T_{\text{JUNCTION-MAX}} - T_{LA}}{\text{TDP}} = \frac{103 - 40}{8} = 7.875^{\circ}\text{C/W}$$

It is evident from the above calculations that a reduction in the local ambient temperature has a significant effect on the junction-to-ambient thermal resistance requirement. This effect can contribute to a more reasonable thermal solution including reduced cost, heatsink size, heatsink weight, and a lower system airflow rate.

This following table summarizes the thermal budget required to adequately cool the chipset. Since the results are based on air data at sea level, a correction factor would be required to estimate the thermal performance at other altitudes.

Table 4. Required Heatsink Thermal Performance (Ψ_{JA})

SKU	Ψ_{JA} (°C/W) at $T_{LA} = 55^{\circ}\text{C}^1$	Ψ_{JA} (°C/W) at $T_{LA} = 60^{\circ}\text{C}^1$	Ψ_{JA} (°C/W) at $T_{LA} = 65^{\circ}\text{C}^1$
SKU 1 and 2	5.05	4.93	4
SKU 3	4.36	3.91	3.45
SKU 4	4	3.58	3.17
Note: 1. Local ambient temperature (T_{LA}) is measured approximately 1" directly upstream of the component thermal solution. Ψ_{JA} calculations will change if $T_{\text{JUNCTION-MAX}}$, TDP or T_{LA} is changed.			

6.0 Reference Heatsinks

Intel has developed reference heatsinks designed to meet the cooling needs of the Intel® Communications Chipset 89xx Series in embedded form factor applications. This chapter describes the overall requirements for the reference thermal solution including critical-to-function dimensions, operating environment, and verification criteria. This document details solutions that are compatible with Small Form Factor Blades . **The reference heatsink designs are not suitable for natural convection cooling and require a prescribed amount of system airflow.** The system designer must ensure that suitable airflow is provided when using the reference heatsinks. [Thermal Solution Component Suppliers](#) on page 28 contains vendor information for each component.

6.1 Small Form Factor Reference Heatsink

Two reference heatsinks are compatible with small embedded form factors. [Figure 9](#) on page 22 and [Figure 10](#) on page 22 demonstrate the heatsink thermal performance at various airflow rates. [Figure 4](#) on page 17 and [Figure 5](#) on page 17 can be used to determine the acceptable ambient temperature range at which this heatsink can be used, based on available airflow.

6.1.1 Mechanical Design

The small form factor reference thermal solutions are shown in the two figures below. The maximum heatsink height is constrained to 15 mm, which enables use in common small form factors such as CompactPCI* and other small form factor blades. One of the reference heatsinks uses spring fastener pushpins to mount to the PCB; the other heatsinks use a torsional spring clip. Detailed drawings of the heatsinks are provided in [Mechanical Drawings](#) on page 29.

Figure 7. Small Form Factor Reference Thermal Solution (Tall) Assembly



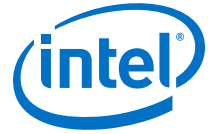
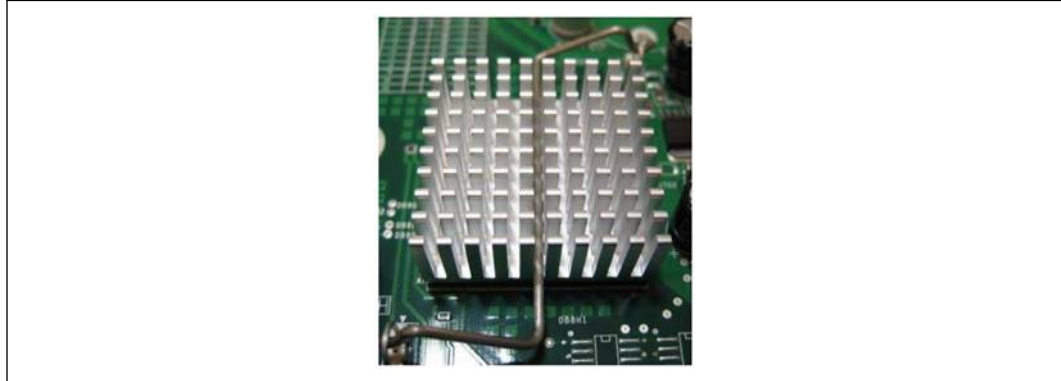


Figure 8. Small Form Factor Reference Thermal Solution (Short) Assembly



6.1.2 Additional Keep Out Zone Requirements

The PCB keep-out zones are shown in [Mechanical Drawings](#) on page 29.

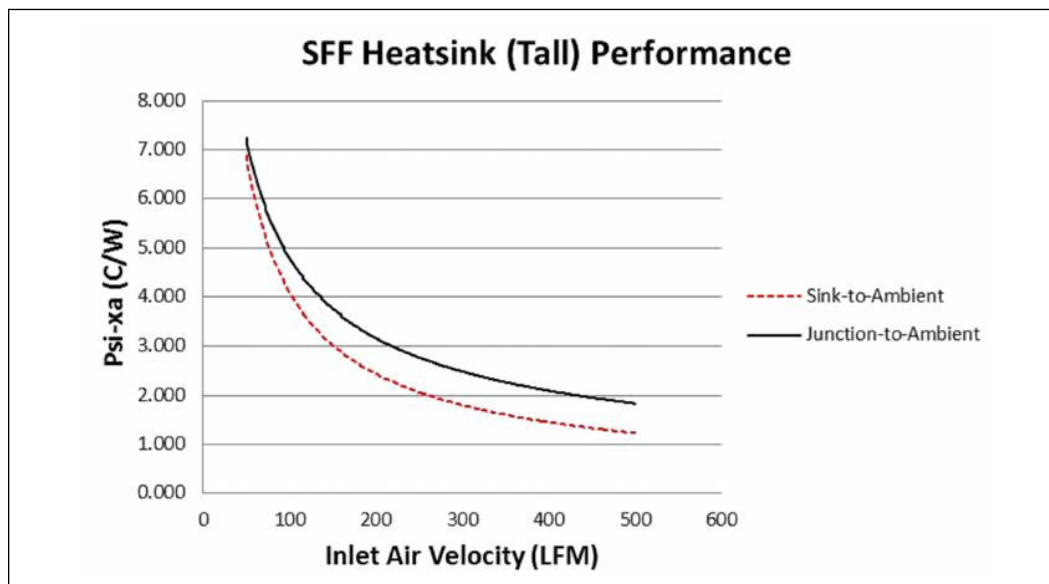
6.1.3 Thermal Performance

The material for the small form factor reference heatsinks is aluminum. These heatsinks can meet the thermal performance needed to cool the chipset in small form factor blades and meet the NEBS short term operating ambient temperature of 55° C. See the performance curves for the required amount of airflow. However, it is up to the system designer to validate the entire thermal solution (heatsink, attach method, TIM) in its final intended system. The data shown in the two figures below are based on computer modeling.

Small Form Factor Reference Thermal Solution (Tall) Performance

This reference design can be utilized for all chipset SKUs dependent on the system airflow and design. The performance curve based on computer modeling for the reference design for the required amount of airflow is shown in the following figure. However, it is up to the system designer to validate the entire thermal solution (heatsink, attach method, TIM) in its final intended system. The data shown in the two figures below are based on computer modeling.

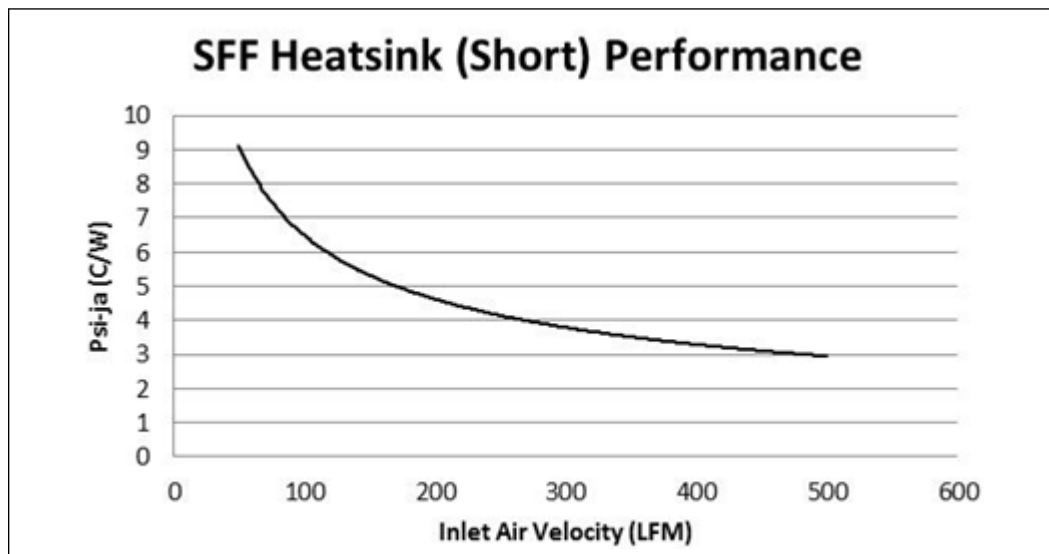
Figure 9. Small Form Factor Reference Thermal Solution (Tall) Performance



Small Form Factor Reference Thermal Solution (Short) Performance

This reference design can be utilized for the 8.5 W and 9.5 W chipset SKUs dependent on the system airflow and design. The performance curve based on computer modeling for the reference design for the required amount of airflow is shown in the following figure. However, it is up to the system designer to validate the entire thermal solution (heatsink, attach method, TIM) in its final intended system.

Figure 10. Small Form Factor Reference Thermal Solution (Short) Performance





6.2 Torsional Clip

Some of the reference solutions use wire clips with hooked ends. The hooks attach to wire anchors to fasten the clip to the board. One instance of the torsional clip is shown in [Figure 10](#) on page 22. See the detailed mechanical drawings in [Mechanical Drawings](#) on page 29.

6.3 Solder-Down Anchors

The torsional clip uses a solder-down anchor to attach to the board. It is based on a standard three-pin jumper and is soldered to the board like any common through-hole header. The anchor design includes 45° bent leads to increase the anchor attach reliability over time. See [Thermal Solution Component Suppliers](#) on page 28 for the part number and supplier information.

6.4 Heatsink Orientation

Since the thermal solutions are based on uni-directional heatsinks, airflow direction must be aligned with the direction of the heatsink fins.

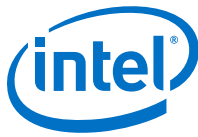
6.5 Thermal Interface Material (TIM)

The thermal interface material provides improved conductivity between the die and heatsink. It is important to understand and consider the impact of the interface between the die and heatsink base to the overall thermal solution. Specifically, the bond line thickness, interface material area, and interface material thermal conductivity must be selected to optimize the thermal solution.

It is important to minimize the thickness of the thermal interface material (TIM), commonly referred to as the bond line thickness. A large gap between the heatsink base and the die yields a greater thermal resistance. The thickness of the gap is determined by the flatness of both the heatsink base and the die, plus the thickness of the thermal interface material, and the clamping force applied by the heatsink attachment method. To ensure proper and consistent thermal performance, the TIM and application process must be properly designed.

The chipset reference thermal solutions (short) use the Chromerics T710. Alternative materials can be used at your discretion. The entire heatsink assembly, including the heatsink and TIM (including the attach method), must be validated together for specific applications.

System designers should also determine the impact of their system boundary conditions and platform usage on the performance of TIM over the lifetime of the product. TIM material performance will degrade over time and could impact ability to keep within operating temperature.



7.0 Thermal Metrology

The system designer must make measurements to accurately determine the performance of the thermal solution. The heatsink designs should be validated using a Thermal Test Vehicle. The thermal test vehicle is a device that simulates the thermal characteristics of the Intel® Communications Chipset 89xx Series. It is also recommended to perform a final verification test of the heatsink with an actual Intel® Communications Chipset 89xx Series in a real working environment.

This chapter provides information to perform thermal tests, including:

- Guidelines on how to accurately measure the component temperature.
- Details for using the thermal test vehicle.
- Information about running power simulation software that will emulate anticipated thermal design powers on the Intel® Communications Chipset 89xx Series.

7.1 T_{JUNCTION} Temperature Measurements

The component T_{JUNCTION} must be maintained at or below the maximum temperature specification as noted in [Maximum Allowed Component Temperature](#) on page 12. The die temperature in the package corresponds to T_{JUNCTION} . Measuring T_{JUNCTION} is measured using the Digital Thermal sensors on the package.

The DTS values are made available to the OS as a PCI bus device for the chipset. The details on the accessing this information can be found in thermal reporting section of the *Intel® Communications Chipset 89xx Series Datasheet*.

7.2 Local Ambient Temperature Measurement Guidelines

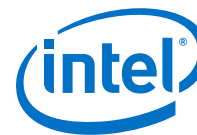
The local ambient temperature (T_{LA}) is the temperature of the ambient air surrounding the processor. For a passive heatsink, T_{LA} is defined as the heatsink approach air temperature; for an actively cooled heatsink, it is the temperature of inlet air to the active cooling fan.

It is worthwhile to determine the local ambient temperature in the chassis around the processor to understand the effect it may have on the die temperature. T_{LA} is best measured by averaging temperature measurements at multiple locations in the heatsink inlet airflow. This method helps reduce error and eliminate minor spatial variations in temperature. The following guidelines are meant to enable accurate determination of the localized air temperature around the processor during system thermal testing.

7.2.1 Active Heatsink Measurements

The following considerations apply:

- It is important to avoid taking measurements in the dead flow zone that usually develops above the fan hub and hub spokes. Measurements should be taken at four different locations uniformly placed at the center of the annulus formed by

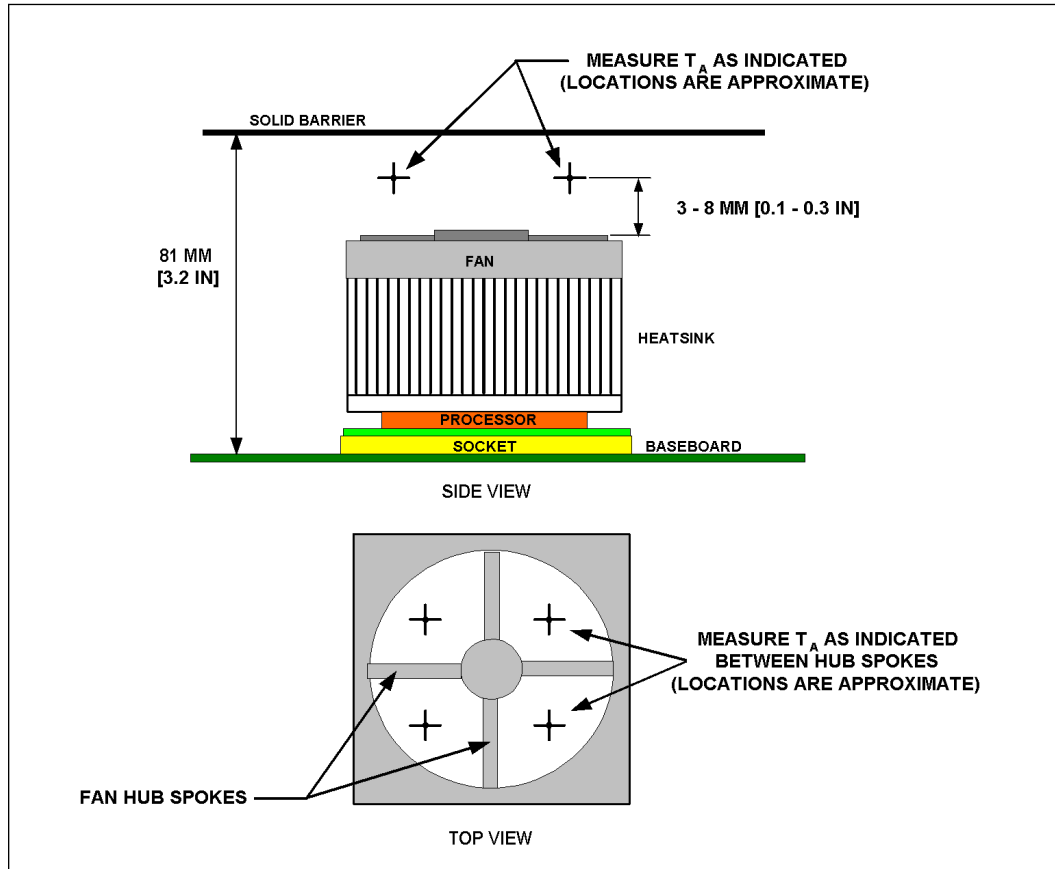


the fan hub and the fan housing to evaluate the uniformity of the air temperature at the fan inlet. The thermocouples should be placed approximately 3 mm to 8 mm [0.1 to 0.3 in] above the fan hub vertically and halfway between the fan hub and the fan housing horizontally as shown in the figure following (avoiding the hub spokes).

- Using an open bench to characterize an active heatsink can be useful, and usually ensures more uniform temperatures at the fan inlet. However, additional tests that include a solid barrier above the test motherboard surface can help evaluate the potential impact of the chassis. This barrier is typically clear Plexiglas*, extending at least 100 mm [4 in.] in all directions beyond the edge of the thermal solution. Typical distance from the motherboard to the barrier is 81 mm [3.2 in.] (this distance can be shortened for more constrained form factors). If a barrier is used, the thermocouple can be taped directly to the barrier with clear tape at the horizontal location as previously described, halfway between the fan hub and the fan housing.
- For even more realistic airflow, the motherboard should be populated with significant elements like memory cards, graphic card, and chipset heatsink. If a variable speed fan is used, it may be useful to add a thermocouple taped to the barrier above the location of the temperature sensor used by the fan to check its speed setting against air temperature. When measuring T_{LA} in a chassis with a live motherboard, add-in cards, and other system components, it is likely that the T_{LA} measurements will reveal a highly non-uniform temperature distribution across the inlet fan section.

Note: Testing an active heatsink with a variable speed fan can be done in a thermal chamber to capture the worst-case thermal environment scenarios. Otherwise, when doing a bench top test at room temperature, the fan regulation prevents the heatsink from operating at its maximum capability. To characterize the heatsink capability in the worst-case environment in these conditions, it is then necessary to disable the fan regulation and power the fan directly, based on guidance from the fan supplier.

Figure 11. Measuring T_{LA} with an Active Heatsink



Note: Drawings are not to scale.

7.2.2 Passive Heatsink Measurements

The following considerations apply:

- Thermocouples should be placed approximately 13 mm to 25 mm [0.5 to 1.0 in] away from processor and heatsink as shown in the following figure.
- The thermocouples should be placed approximately 51 mm [2.0 in] above the baseboard. This placement guideline is meant to minimize the effect of localized hot spots from baseboard components. The height above the board may vary depending on the height of the thermal solution and form factor.

Note: The location for measuring T_{LA} is also the recommended location for measuring airflow approach velocity for a passive heatsink.

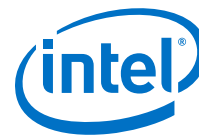
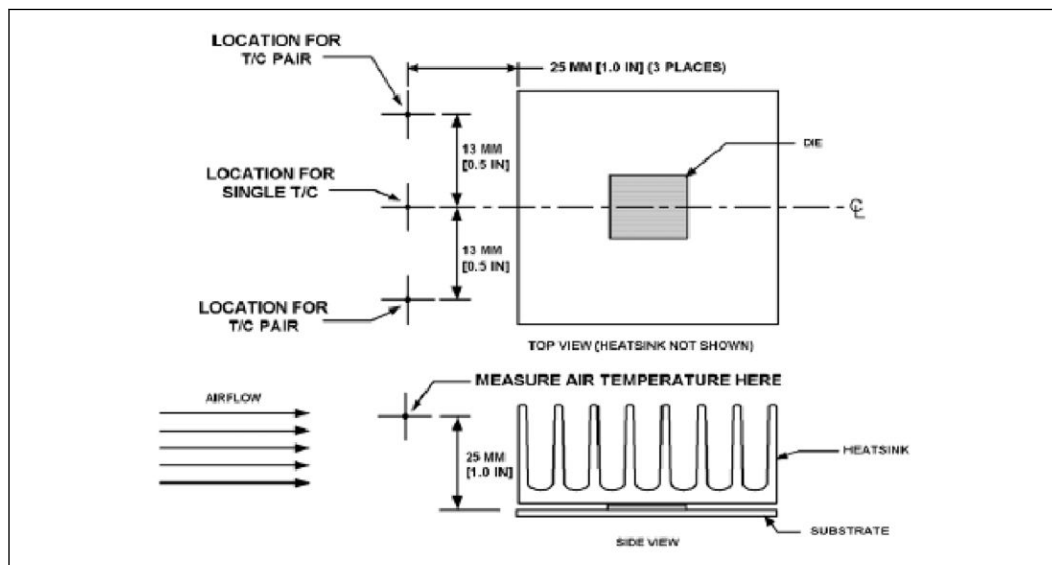


Figure 12. Measuring T_{LA} with a Passive Heatsink



Note: Drawing not to scale.

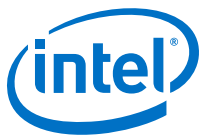
7.3 Thermal Test Vehicle

The Thermal Test Vehicle is designed to simulate the thermal characteristics of the Intel® Communications Chipset 89xx Series. However, the device is not a functional chipset. Using a custom test board provided with the TTV, the power into the device can be accurately controlled. Using the method described in [Local Ambient Temperature Measurement Guidelines](#) on page 24, the thermal performance of the heatsink can be determined. The chipset TTV may not currently be available.

Contact your Intel field representative to obtain a Thermal Test Vehicle.

7.4 Power Thermal Utility

The Power Thermal Utility (PTU) is a utility designed to dissipate the thermal design power on the chipset. To assess the thermal performance of thermal solution under “worst-case realistic application” conditions, Intel has developed a software utility that stresses the chipset at various power levels, up to and exceeding TDP. The Power Thermal Utility program may not currently be available.



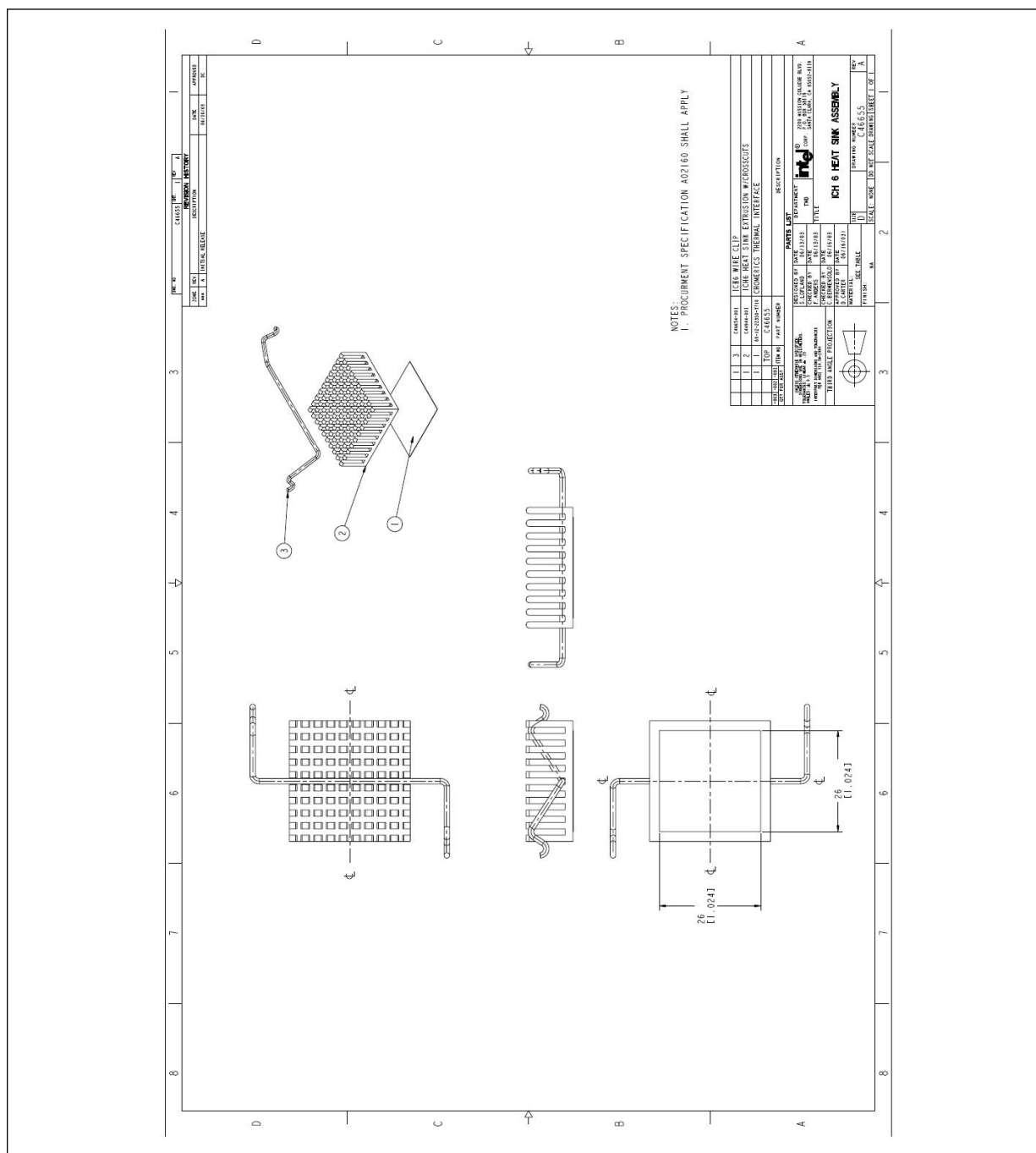
Appendix A Thermal Solution Component Suppliers

A.1 Reference Heatsink

Table 5. Suppliers

Part	Intel Part Number	Supplier / Part Number	Contact Information
Small Form Factor Heatsink (Tall)	N/A	Alpha-Novatech: UBR35-15B-0M1E68	Glenn Summerfield: glenn@alphanovatech.com
Small Form Factor Heatsink (Short) Assembly	C46655-001	AVC: S702C00001	Kai Chang: kai_chang@avc.com.tw
		CCI: 00C855802B	Monica Chih: monica_chih@ccic.com.tw Harry Lin: hlinack@aol.com
		Foxconn: 2Z802-009	Jack Chen: jack.chen@foxconn.com Wanchi Chen: wanchi.chen@Foxconn.com
Anchor	A13494-008	Foxconn: HB9703E-DW	same as above
		Wieson: G2100C888-064H	Honeywell Judy Oles Judy.Oles@Honeywell.com (509)252-8605
Note: The enabled components currently may not be available from all suppliers. Contact the supplier directly to verify component availability.			

Figure 13. Small Form Factor Heatsink (Short) Assembly



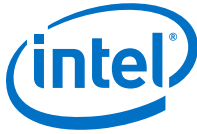


Figure 14. Small Form Factor Heatsink (Short)

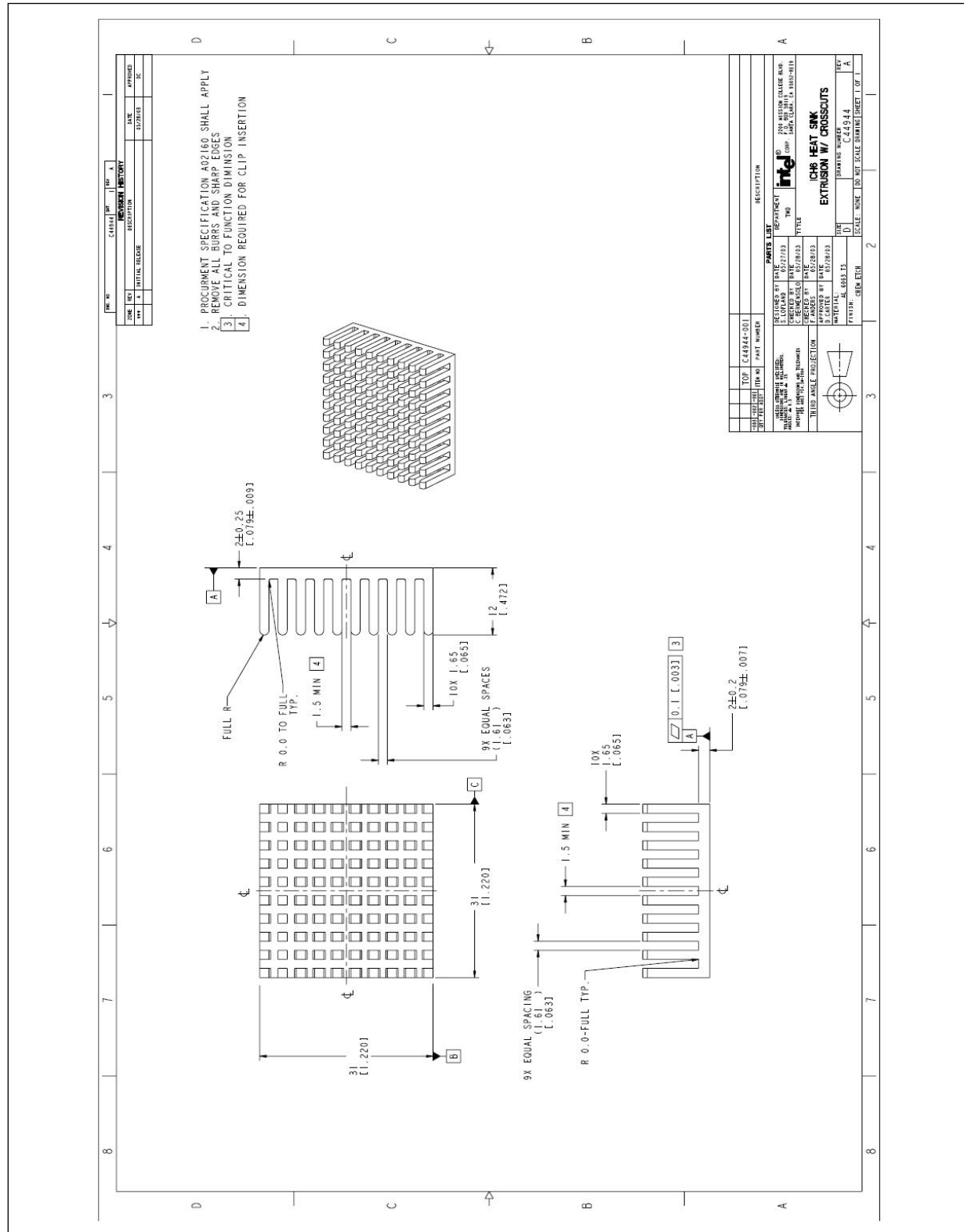


FIG. NO. C46554 REV. 07
REVISION HISTORY

DATE	BY	DESCRIPTION	APPROVED
XXX	X	INITIAL RELEASE	XX

NOTES:

- PROCUREMENT SPECIFICATION A02160 SHALL APPLY
- REMOVE ALL SHARP EDGES AND BURRS
- MATERIAL: 302 1/2H STAINLESS STEEL ($\phi \pm .4MM$)
- CRITICAL TO FUNCTION DIMENSION.

PARTS LIST

QTY	REF	ITEM NO.	PART NUMBER	DESCRIPTION
1		TOP	C46554-001	ICH8 WIRE CLIP

INSPECTION RECORD

DATE	BY	DATE	BY	DATE	BY
XXXXXX	XXXX	XXXXXX	XXXX	XXXXXX	XXXX

TESTING RECORD

DATE	BY	DATE	BY	DATE	BY
XXXXXX	XXXX	XXXXXX	XXXX	XXXXXX	XXXX

APPROVALS

DATE	BY	DATE	BY	DATE	BY
XXXXXX	XXXX	XXXXXX	XXXX	XXXXXX	XXXX

DRAWING NUMBER C46554
DO NOT SCALE DRAWING SHEET 1 OF 1



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1 4xØ0.97 [.038] PLATED THRU HOLE
4xØ0.42[.056] TRACE KEEPOUT

NO COMPONENTS THIS AREA

MAX COMPONENT HEIGHT
3.25 [.125]

COMPONENT CENTER

MAX COMPONENT HEIGHT
(NON-ICH COMPONENTS)
1.51 [.059]

2X 27.43 [1.080]

2X 18.29 [.720]

2X 5 [.197]

2X 22.39 [.882]

33 [1.299]

33 [1.299]

2X 4.19 [.165]

2X 1.85 [.073]

2X 5.08 [.200]

2X 8.76 [.345]

2X 2.11 [.083]

DETAIL A
DO NOT SCALE

NOTES:
1 HOLE PLACEMENT FABRICATION
TOLERANCE PER INTEL 454979, CLASS 1,2,3.

REVISION HISTORY		DATE		BY		APPROVED	
ZONE	REV	DESCRIPTION	DATE	BY	APPROVED	DATE	BY
1.0	1.0	CHANGED REFERENCE TO 1.0					

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ZONE	REV	DESCRIPTION	DATE	BY	APPROVED	DATE	BY
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ZONE	REV	DESCRIPTION	DATE	BY	APPROVED	DATE	BY
1.0	1.0	CHANGED REFERENCE TO 1.0					

DESIGNATION		DATE		BY		APPROVED	
ZONE	REV	DESCRIPTION	DATE	BY	APPROVED	DATE	BY
1.0	1.0	CHANGED REFERENCE TO 1.0					

DESIGNATION		DATE		BY		APPROVED	
ZONE	REV	DESCRIPTION	DATE	BY	APPROVED	DATE	BY
1.0	1.0	CHANGED REFERENCE TO 1.0					

DESIGNATION		DATE		BY		APPROVED	
ZONE	REV	DESCRIPTION	DATE	BY	APPROVED	DATE	BY
1.0	1.0	CHANGED REFERENCE TO 1.0					

DESIGNATION		DATE		BY		APPROVED	
ZONE	REV	DESCRIPTION	DATE	BY	APPROVED	DATE	BY
1.0	1.0	CHANGED REFERENCE TO 1.0					

DESIGNATION		DATE		BY		APPROVED	
ZONE	REV	DESCRIPTION	DATE	BY	APPROVED	DATE	BY
1.0	1.0	CHANGED REFERENCE TO 1.0					

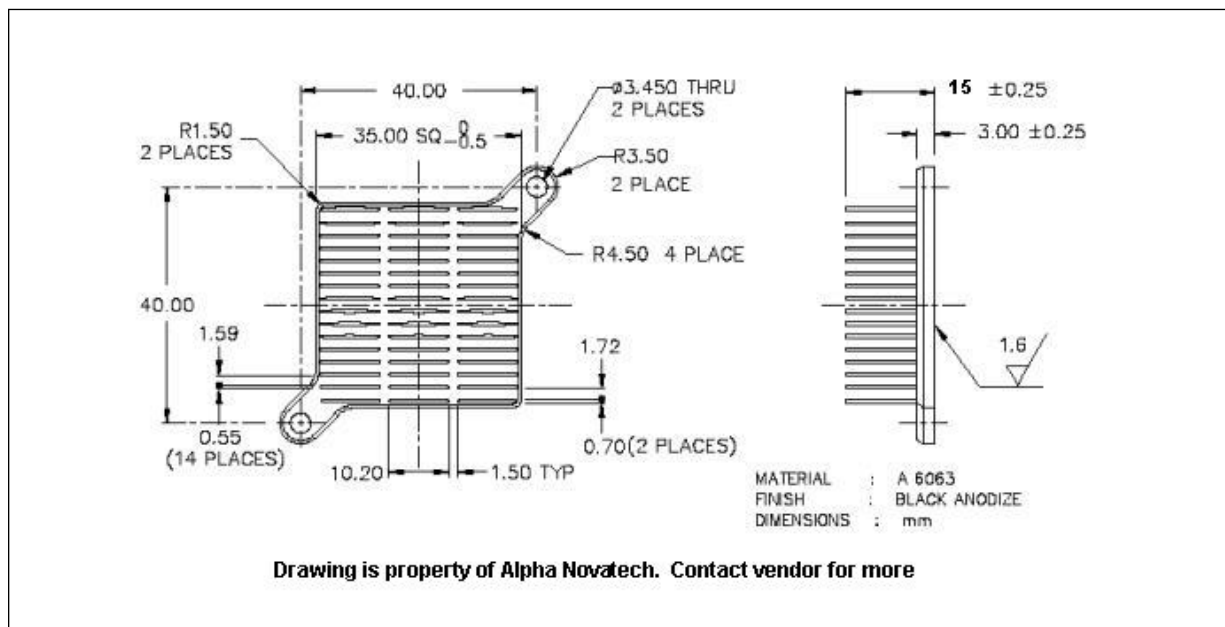
DESIGNATION		DATE		BY		APPROVED	
ZONE	REV	DESCRIPTION	DATE	BY	APPROVED	DATE	BY
1.0	1.0	CHANGED REFERENCE TO 1.0					

DESIGNATION		DATE		BY		APPROVED	
ZONE	REV	DESCRIPTION	DATE	BY	APPROVED	DATE	BY
1.0	1.0	CHANGED REFERENCE TO 1.0					

DESIGNATION		DATE		BY		APPROVED	
ZONE	REV	DESCRIPTION	DATE	BY	APPROVED	DATE	BY
1.0							



Figure 17. Small Form Factor Heatsink (Tall)



Note: Drawing is the property of Alpha Novatech. Contact vendor for more information.

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DWG. NO. CAVE_CREEK_ATCA_KOZ SHT. 1 REV. 1

4 3 1

AIRFLOW

2X $\phi 7$

20 20

35 27

2X $\phi 5$
PCB TRACE KEEP-OUT ZONE
PRIMARY AND SECONDARY SIDE

2X $\phi 3.175$
PLATED THROUGH HOLES

27 35

1.75 MM MAX COMPONENT HEIGHT

A B

SCALE 1

NOTES:
1) DIMENSIONS IN MILLIMETERS

DEPARTMENT	CAGE CODE	DRAWING NUMBER	REV
-	X	CAVE_CREEK_ATCA_KOZ	
SCALE: 1		DO NOT SCALE DRAWING SHEET 1 OF 1	

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