Intel(R) IQ80331 I/O Processor DDR-II 400 Evaluation Platform Board (IQ80331)

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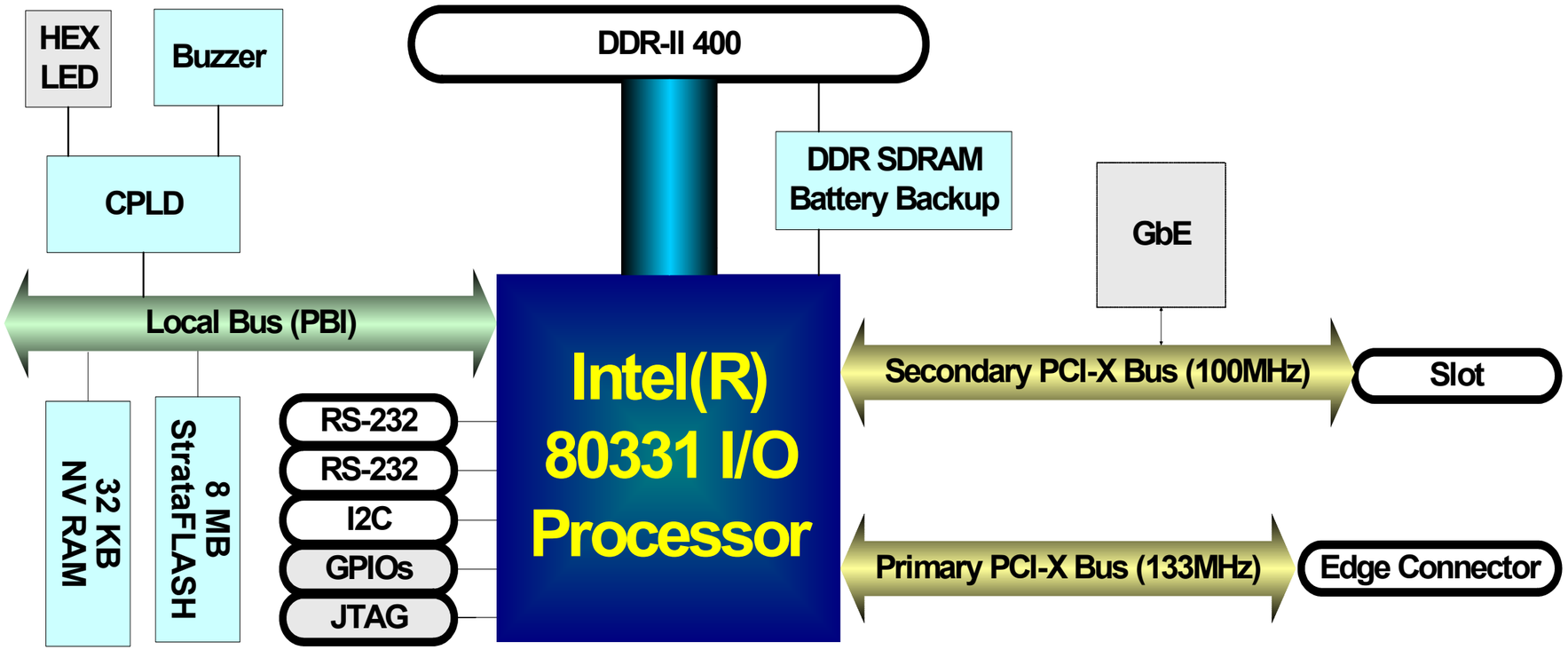
DESIGN ENGINEER:	DESIGN NAME:	SHEET TITLE:	DATE MODIFIED:	VERSION:	SHEET
SCD HARDWARE ENGINEERING	80331 DDR-II 400 CRB	INTEL(R) IQ80331 I/O PROCESSOR DDR-II 400 EVALUATION PLATFORM BOARD (IQ80331)	9-29-2004_6:59	P 1.0	1 OF 21

INTEL(R) IQ80331 DDR-II 400 BLOCK DIAGRAM



DESIGN ENGINEER:	DESIGN NAME:	SHEET TITLE:	DATE MODIFIED:	VERSION:	SHEET
SCD HARDWARE ENGINEERING	80331 DDR-II 400 CRB	IQ80331 DDR-II 400 BLOCK DIAGRAM	9-23-2004_8:59	P 1.0	2 OF 21

INTERRUPTS HEADER

J2C1

3/B7,7/D8	S_INTA_N	1
3/B7,7/D5	S_INTB_N	2
3/B7,7/D8,8/A7	S_INTC_N	3
3/B7,7/D5	S_INTD_N	4
	NC	5
	NC	6
	NC	7
	NC	8
3/B1	HPI_N	9

U3E3

Intel(R) 80331 I/O Processor

PART 1 OF 9

SECONDARY PCI-X BUS
(I/O Processor BUS)

7/A8,8/C8 S_AD[63:0]

S_AD63 L3, S_AD62 M3, S_AD61 M2, S_AD60 M1, S_AD59 N2, S_AD58 N3, S_AD57 N1, S_AD56 P3, S_AD55 P2, S_AD54 P1, S_AD53 R3, S_AD52 R2, S_AD51 R1, S_AD50 T3, S_AD49 T2, S_AD48 U3, S_AD47 J3, S_AD46 J1, S_AD45 J2, S_AD44 H3, S_AD43 K3, S_AD42 K2, S_AD41 L2, S_AD40 L1, S_AD39 L3, S_AD38 M3, S_AD37 M4, S_AD36 M2, S_AD35 N4, S_AD34 N3, S_AD33 P3, S_AD32 A5, S_AD31 B5, S_AD30 A6, S_AD29 C4, S_AD28 C3, S_AD27 D5, S_AD26 B3, S_AD25 C2, S_AD24 A3, S_AD23 D4, S_AD22 A2, S_AD21 C1, S_AD20 D3, S_AD19 A9, S_AD18 B8, S_AD17 C8, S_AD16 B7, S_AD15 C6, S_AD14 H1, S_AD13 F3, S_AD12 G1, S_AD11 H2, S_AD10 E3, S_AD9 F5, S_AD8 D2, S_AD7 G2, S_AD6 H5, S_AD5 F2, S_AD4 G3, S_AD3 H4, S_AD2 E2, S_AD1 F1, S_AD0 E1

7/A8,8/B7 S_CBE[7:0]_N

S_CBE7_N L7, S_CBE6_N L5, S_CBE5_N K6, S_CBE4_N K5, S_CBE3_N D6, S_CBE2_N G7, S_CBE1_N H7, S_CBE0_N H5

7/B5,8/B7 S_PAR F6
7/B5,8/A7 S_STOP_N D8
7/B5,8/B7 S_TRDY_N E8
7/B5,8/B7 S_FRAME_N G8
7/B8,8/B7 S_IRDY_N H8
7/B8,8/A7 S_DEVSEL_N F8
7/B8,8/A7 S_PERR_N G5
7/B8,8/A7 S_SERR_N E6
7/B8,8/A7 S_LOCK_N E7
7/B7 S_PCIXCAP R1

7/B8,8/A7 S_M66EN C9
7/C1,8/B7 S_PAR64 K8
7/A8,8/A7 S_ACK64_N J8
7/A5,8/A7 S_REQ64_N J9

9/D6 S_RST_N R5 — NC — R25 — NC

7/C8 S_REQ0_N N5
8/A7 S_REQ1_N F9
NC E5
NC K9

NC U5
NC R9

8/A7 S_GNT1_N B6
7/C5 S_GNT0_N A7

3/D8,7/D8 S_INTA_N U7
3/D8,7/D5 S_INTB_N U8
3/D8,7/D8,8/A7 S_INTC_N T9
3/C8,7/D5 S_INTD_N R9

20/D7 S_CLKO_MICTOR — R2D13 33.2 1% — S_CLKO_MICTOR_R H3 S_CLK03
8/A7 S_CLKO_GBE — R2D9 33.2 1% — S_CLKO_GBE_R F5 S_CLK02
16/C8 S_CLKO_CPLD — R2D11 33.2 1% — S_CLKO_CPLD_R G4 S_CLKO1
7/C8 S_CLKO_SLOT — R2D8 33.2 1% — S_CLKO_SLOT_R H6 S_CLKO0
R2D6 33.2 1%

S_CLKOUT_R G9 S_CLKOUT
S_CLKIN G10 S_CLKIN
S_RCOMP T5 S_RCOMP

R3C7 100 — GND

80331_BGA829

U3E3

P1_5V — 1_5V Y1

NC AA1 NC_AA1
NC U6 NC_U6
NC U5 NC_U5
NC V7 NC_V7
NC W7 NC_W7
NC U8 NC_U8
NC W8 NC_W8
NC T8 NC_T8

PART 8 OF 9

Intel(R) 80331
I/O Processor

PRIMARY PCI-X BUS

P_AD[63:0] 6/A8

P_AD63 R1, P_AD62 P4, P_AD61 P3, P_AD60 P1, P_AD59 N1, P_AD58 N2, P_AD57 N3, P_AD56 M1, P_AD55 M2, P_AD54 M4, P_AD53 L1, P_AD52 L3, P_AD51 L4, P_AD50 K1, P_AD49 J1, P_AD48 J2, P_AD47 R8, P_AD46 R7, P_AD45 R5, P_AD44 P6, P_AD43 P7, P_AD42 P8, P_AD41 N5, P_AD40 N6, P_AD39 N8, P_AD38 M5, P_AD37 M7, P_AD36 M8, P_AD35 L6, P_AD34 L7, P_AD33 L8, P_AD32 K8, P_AD31 B10, P_AD30 C10, P_AD29 A9, P_AD28 B9, P_AD27 D9, P_AD26 A8, P_AD25 C8, P_AD24 D8, P_AD23 B7, P_AD22 C7, P_AD21 A6, P_AD20 B6, P_AD19 D6, P_AD18 A5, P_AD17 C5, P_AD16 A4, P_AD15 B3, P_AD14 C3, P_AD13 C2, P_AD12 D3, P_AD11 D2, P_AD10 D1, P_AD9 E4, P_AD8 F4, P_AD7 F2, P_AD6 F1, P_AD5 G3, P_AD4 G2, P_AD3 G1, P_AD2 H4, P_AD1 H3, P_AD0 H1

P_CBE[7:0]_N 6/A8

P_CBE7_N U3, P_CBE6_N T3, P_CBE5_N U2, P_CBE4_N U1, P_CBE3_N A7, P_CBE2_N D5, P_CBE1_N B4, P_CBE0_N E1

P_PAR C4 — P_PAR 6/B5
P_STOP_N G6 — P_STOP_N 6/B5
P_TRDY_N H10 — P_TRDY_N 6/B5
P_FRAME_N E9 — P_FRAME_N 6/B5
P_IRDY_N F5 — P_IRDY_N 6/B8
P_DEVSEL_N G5 — P_DEVSEL_N 6/B8
P_PERR_N J4 — P_PERR_N 6/B8
P_SERR_N J5 — P_SERR_N 6/B8
P_LOCK_N J7 — P_LOCK_N 6/B8

P_M66EN E3 — P_M66EN 6/B8
P_PAR64 R2 — P_PAR64 6/C2
P_ACK64_N H6 — P_ACK64_N 6/A8
P_REQ64_N G11 — P_REQ64_N 6/A5
VSS W4
NC_H13 H13 — NC
NC_V8 V8 — NC
GND

HPI_N AA8
P_INTA_N W3 — P_INTA_N 6/D5
P_INTB_N V5 — P_INTB_N 6/D8
P_INTC_N V4 — P_INTC_N 6/D5
P_INTD_N V2 — P_INTD_N 6/D8

NC_R4 R4 — NC
NC_K5 K5 — NC
P_GNT_N G12 — P_GNT_N 6/C5
P_IDSEL K3 — P_IDSEL 6/C5
NC_K2 K2 — NC

NC_H12 H12 — NC
NC_F11 F11 — NC
P_REQ_N H11 — P_REQ_N 6/C8
NC_T4 T4 — NC
NC_T6 T6 — NC

NC_H7 H7 — NC
NC_H9 H9 — NC
NC_H8 H8 — NC
NC_J8 J8 — NC
NC_F7 F7 — NC
NC_E7 E7 — NC
P_CLK G9 — P_CLK 6/C8

NC_K6 K6 — NC

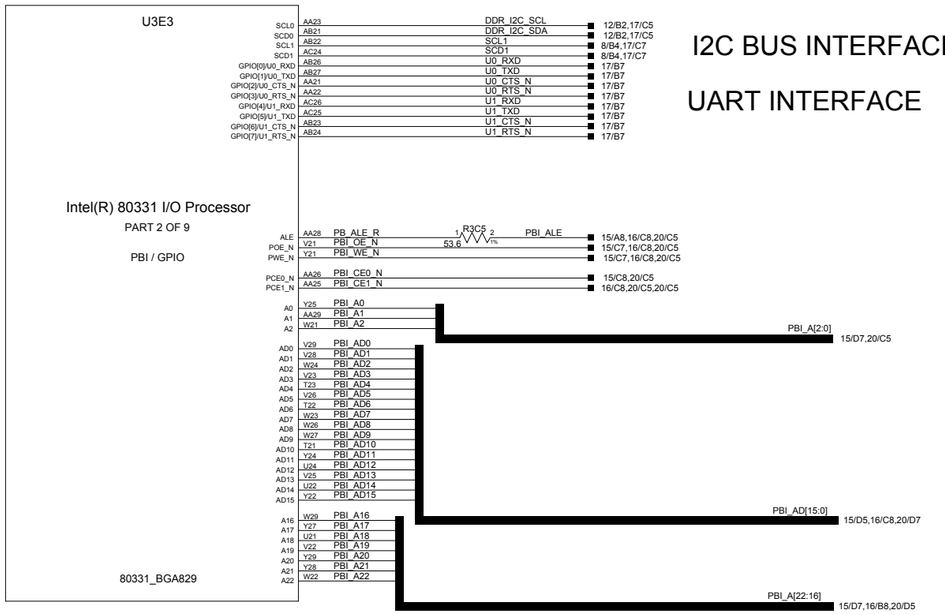
80331_BGA829 P_RCOMP V1 — P_RCOMP — R4D4 100 — GND

P3_3V
R2D16 6.2K 1%
NO_POP R7R5 0
HPI_N 3/C8

	DESIGN ENGINEER: SCD HARDWARE ENGINEERING	DESIGN NAME: 80331 DDR-II 400 CRB	SHEET TITLE: INTEL(R) IQ80331 PRIMARY AND SECONDARY PCI	DATE MODIFIED: 9-23-2004_9:20	VERSION: P 1.0	SHEET 3 OF 21

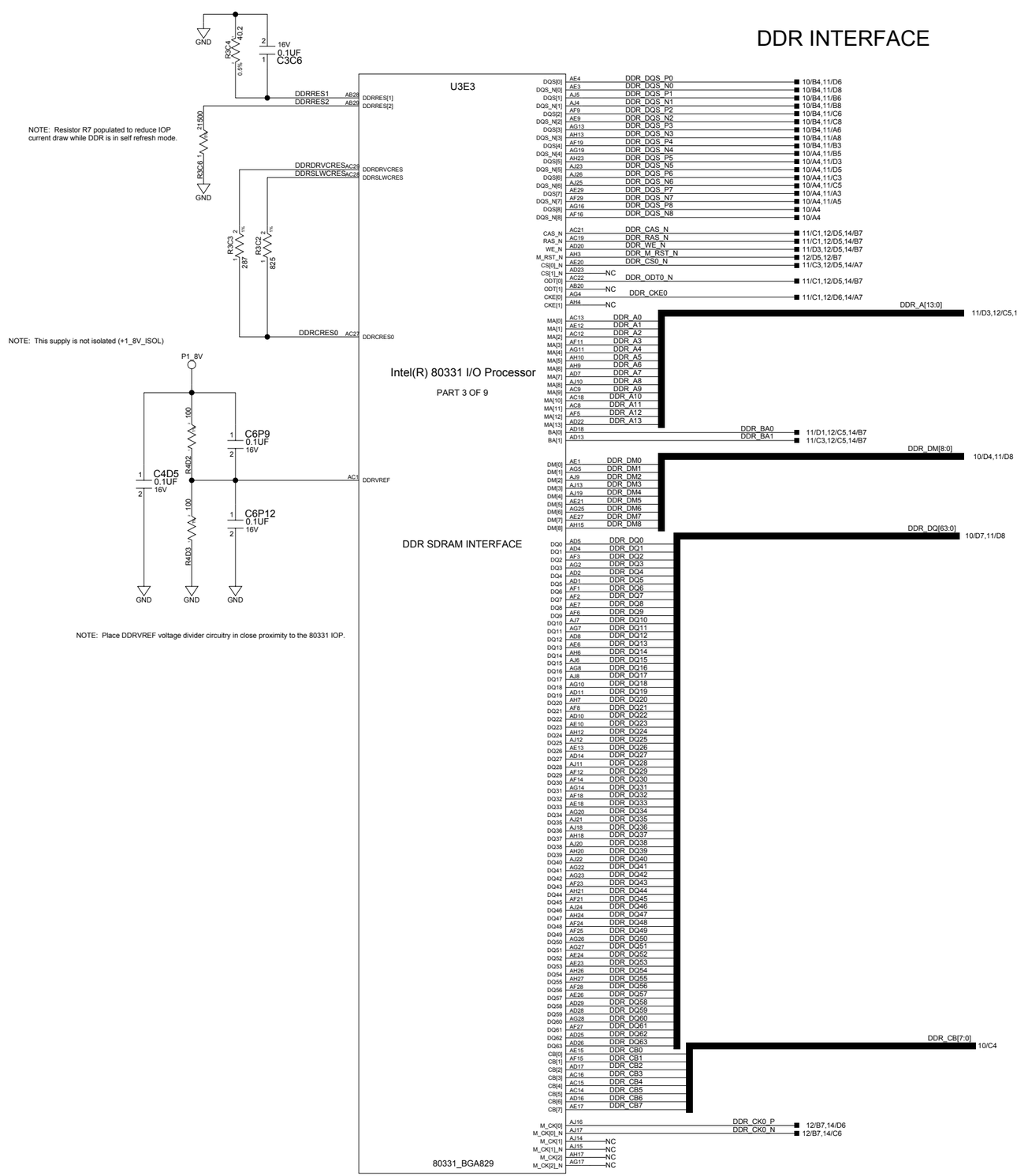
I2C BUS INTERFACE

UART INTERFACE

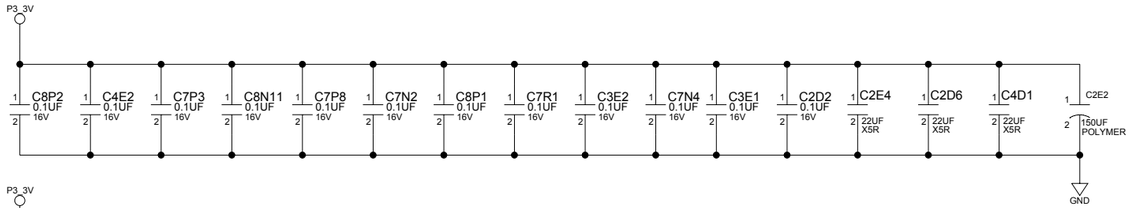


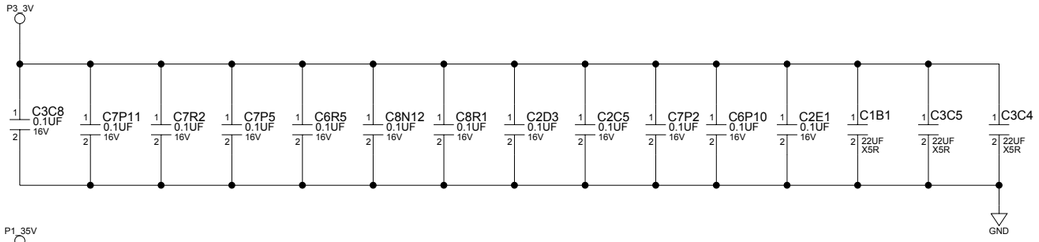
PERIPHERAL BUS INTERFACE (PBI)

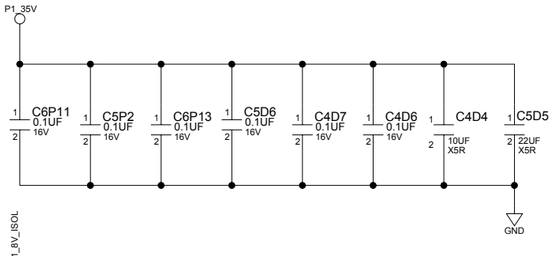
DDR INTERFACE

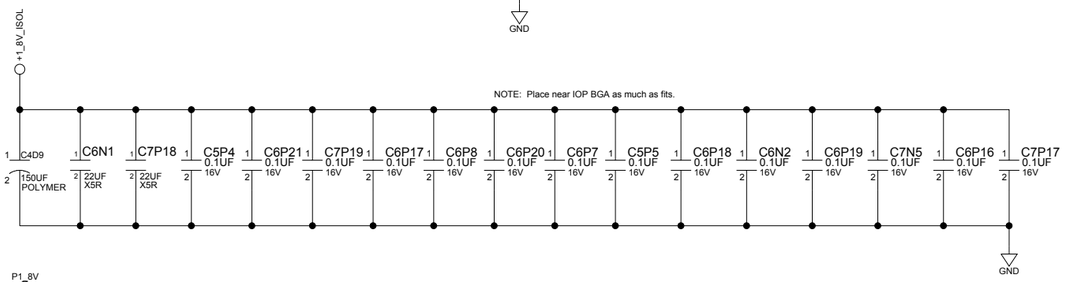


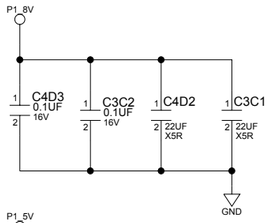
DESIGN ENGINEER:	DESIGN NAME:	SHEET TITLE:	DATE MODIFIED:	VERSION:	SHEET
SCD HARDWARE ENGINEERING	80331 DDR-II 400 CRB	INTEL(R) IQ80331 - DDR / PBI / UART / I2C	9-23-2004_8:59	P 1.0	4 OF 21

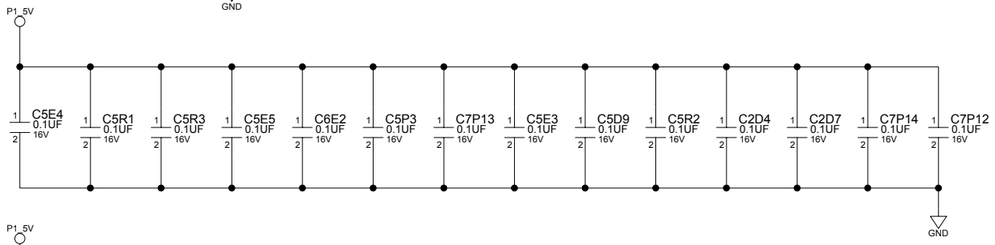


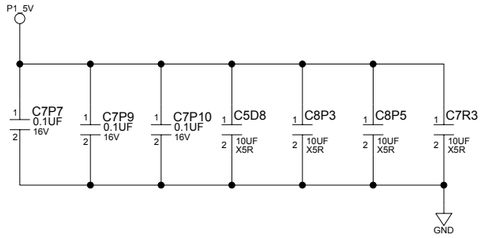




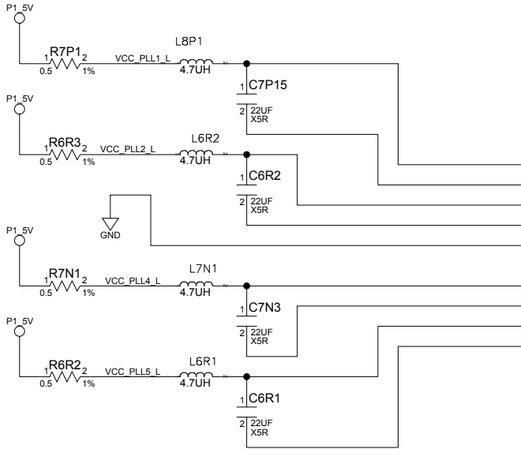






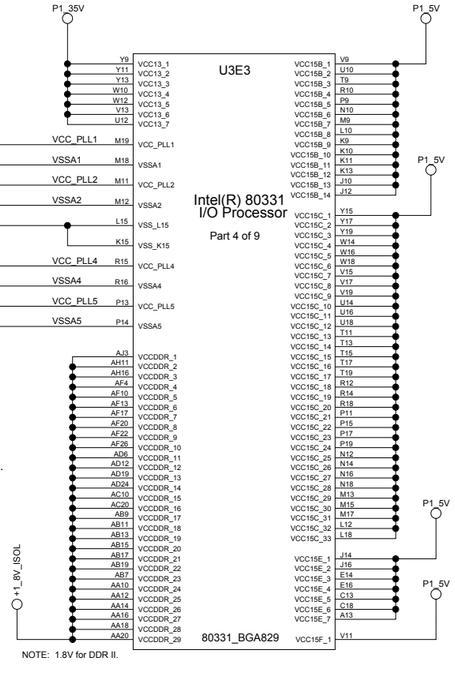


FILTERED PHASE LOCK-LOOP SUPPLY

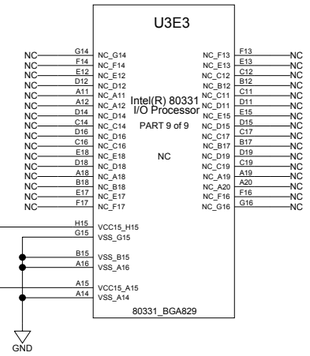


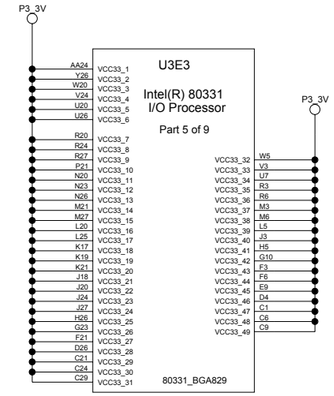
NOTE: Route these as differential Pairs.
5 on 5 in Breakout.25 on 5 to CAP.

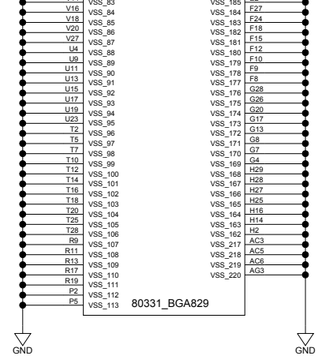
IOP PWR & GND PINS



NOTE: 1.8V for DDR II.







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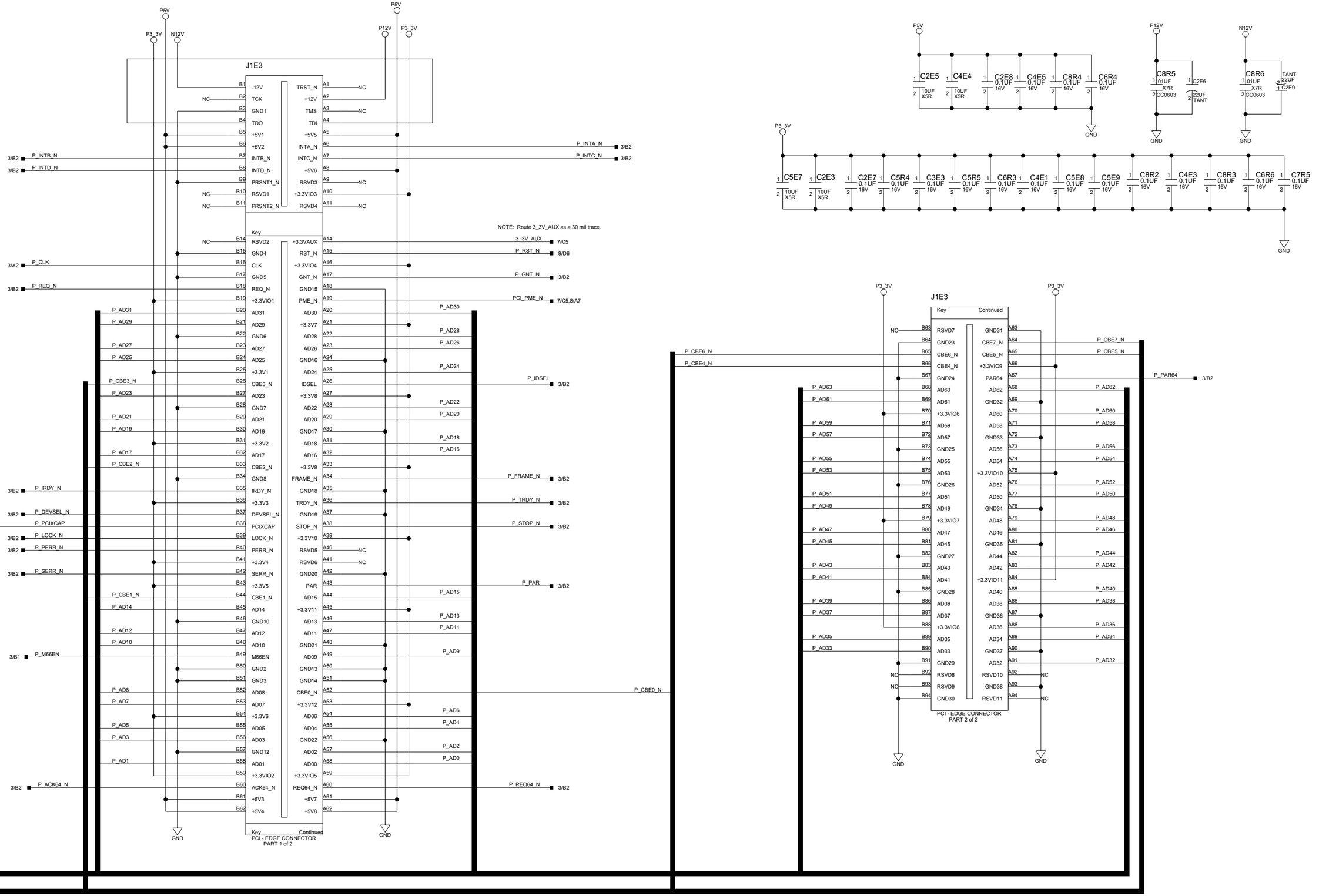

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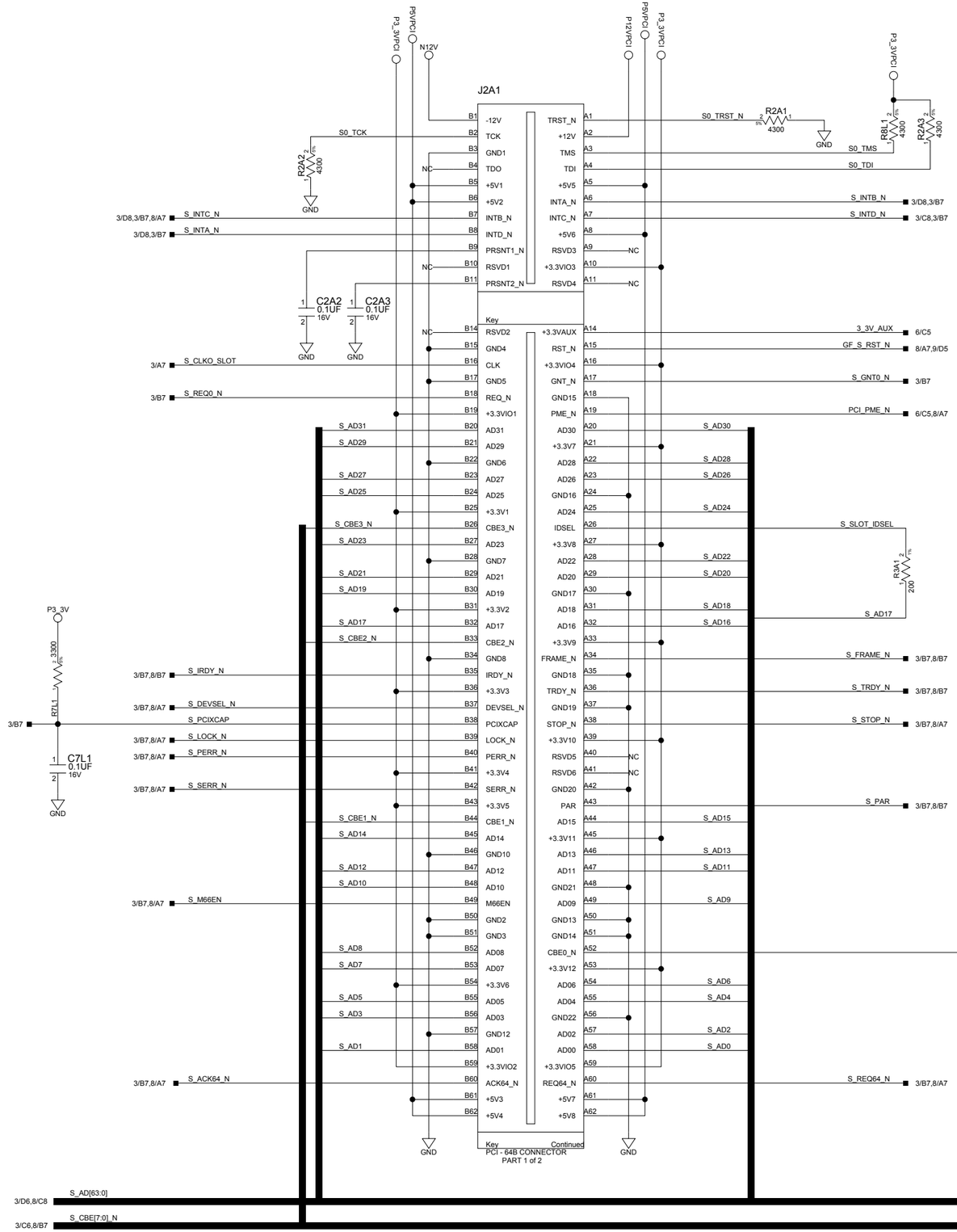
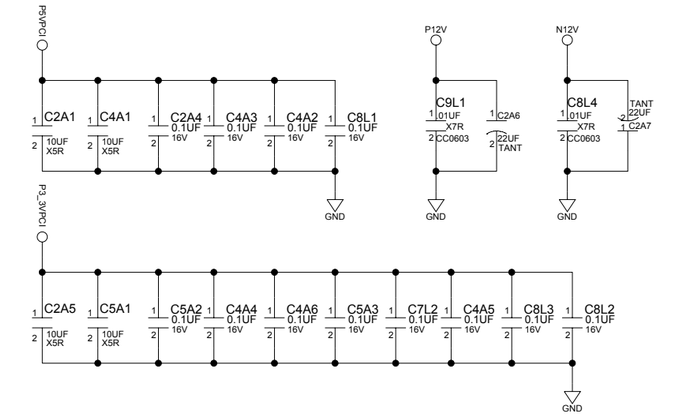
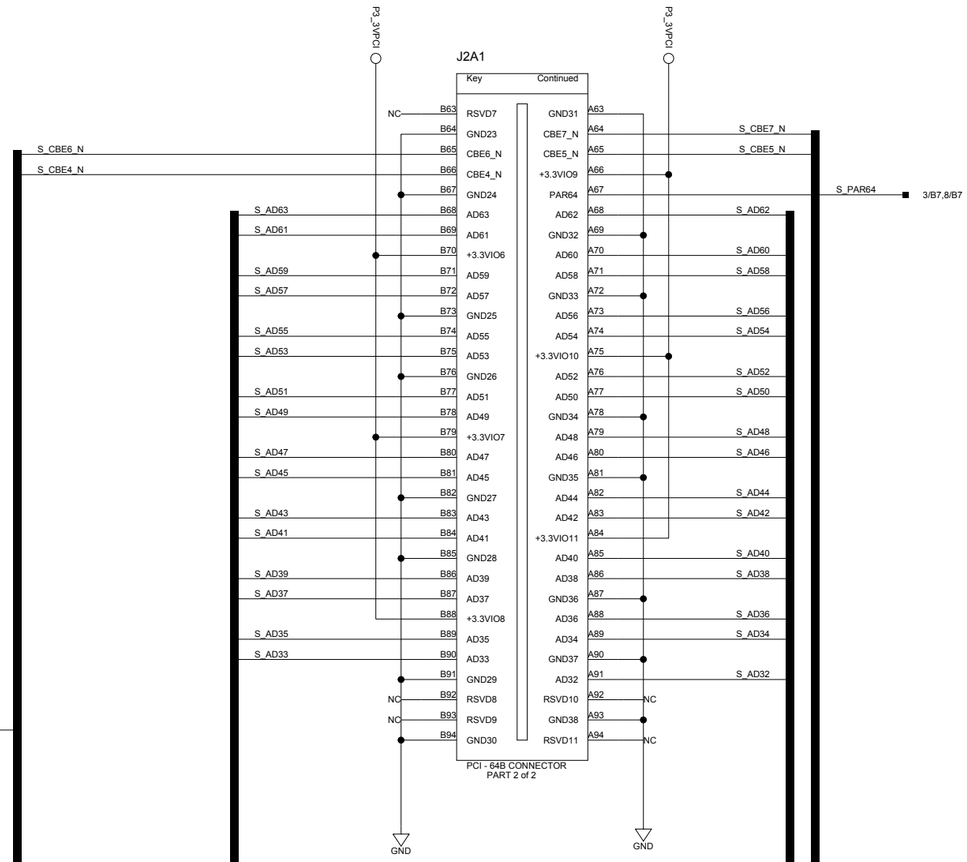
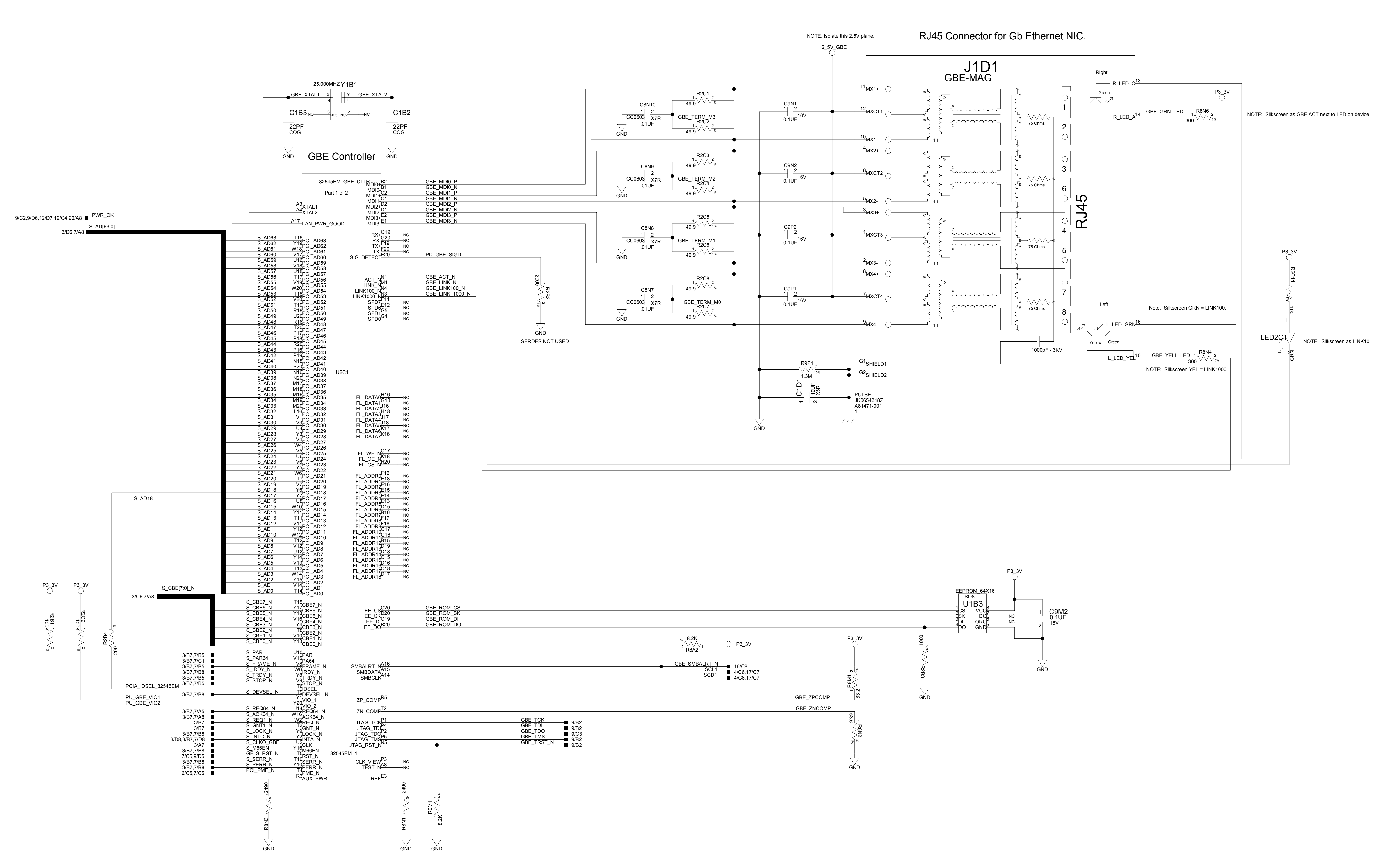






	DESIGN ENGINEER: SCD HARDWARE ENGINEERING	DESIGN NAME: 80331 DDR-II 400 CRB	SHEET TITLE: SECONDARY PCI-X BUS SLOT	DATE MODIFIED: 9-23-2004_9:04	VERSION: P 1.0	SHEET 7 OF 21



RJ45 Connector for Gb Ethernet NIC.
NOTE: Isolate this 2.5V plane.
+2_5V_GBE
J1D1
GBE-MAG
RJ45
GBE Controller
25.000MHZ Y1B1
GBE_XTAL1
GBE_XTAL2
C1B3
C1B2
22PF
COG
GND
82545EM_GBE_CTLR
Part 1 of 2
U2C1
82545EM_1
GBE_MDI0_P
GBE_MDI0_N
GBE_MDI1_P
GBE_MDI1_N
GBE_MDI2_P
GBE_MDI2_N
GBE_MDI3_P
GBE_MDI3_N
PD_GBE_SIGD
GBE_ACT_N
GBE_LINK_N
GBE_LINK100_N
GBE_LINK_1000_N
SERDES NOT USED
PWR_OK
9/C2,9/D6,12/D7,19/C4,20/A8
S_AD[63:0]
3/D6,7/A8
S_AD18
S_CBE[7:0]_N
3/C6,7/A8
PCIA_IDSEL_82545EM
PU_GBE_VIO1
PU_GBE_VIO2
P3_3V
GBE_TERM_M3
GBE_TERM_M2
GBE_TERM_M1
GBE_TERM_M0
75 Ohms
1000pF - 3KV
SHIELD1
SHIELD2
PULSE
JK0654218Z
A81471-001
Right
Left
R_LED_C
R_LED_A
L_LED_GRN
L_LED_YEL
Green
Yellow
GBE_GRN_LED
GBE_YELL_LED
NOTE: Silkscreen as GBE ACT next to LED on device.
Note: Silkscreen GRN = LINK100.
NOTE: Silkscreen YEL = LINK1000.
NOTE: Silkscreen as LINK10.
LED2C1
EEPROM_64X16
SO8
U1B3
C9M2
0.1UF
16V
GBE_ROM_CS
GBE_ROM_SK
GBE_ROM_DI
GBE_ROM_DO
GBE_SMBALRT_N
SCL1
SCD1
16/C8
4/C6,17/C7
GBE_ZPCOMP
GBE_ZNCOMP
GBE_TCK
GBE_TDI
GBE_TDO
GBE_TMS
GBE_TRST_N

DESIGN ENGINEER:	DESIGN NAME:	SHEET TITLE:	DATE MODIFIED:	VERSION:	SHEET
SCD HARDWARE ENGINEERING	80331 DDR-II 400 CRB	GIGABIT ETHERNET CONTROLLER	9-23-2004_9:04	P 1.0	8 OF 21

GBE GND PINS

U2C1
Part 2 of 2
82545EM_2

82545EM_GBE_CTLR

NOTE: 82545EB provides 2.5V regulator.

NOTE: Depopulate R2 and populate R9 when battery backup capability is not required.

JTAG INTERFACE

U3E3
Intel(R) 80331 I/O Processor
PART 7 OF 9
JTAG/MISC
80331_BGA829

NO_POP=TRUE

NOTE: The 80331 has weak internal pullups on the JTAG TDI, TMS, TRST_N signals.

JUMPER J1B2

PIN	SETTING
1 & 2	JTAG Communication to IOP only.
3 & 4	JTAG Communication to IOP and Gb-Ethernet.
5 & 6	Not Applicable, No Connection.
7 & 8	Enables 1K TRST# Pull-down.

JTAG Connector

P1C1

J1B2
HEADER2X4
Jumper Here for 80331 only.
Jumper Here for 80331 + GBE.
Jumper Here to add TRST# Pulldown.

NOTE: JTAG Control Header/Jumpers.

U6E1
MAX6306UK29D3
SOT23_5

NOTE: Reset Timeout Period = 140ms.

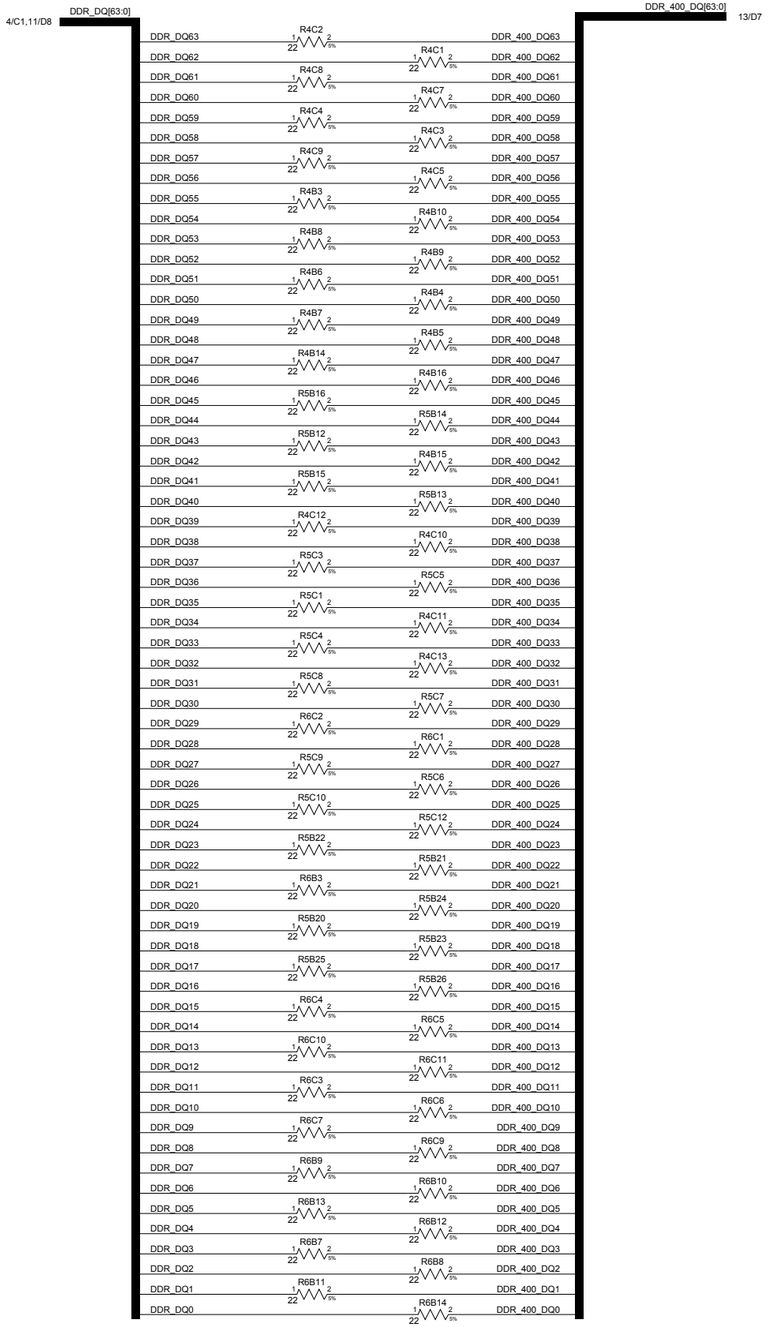
U4D1
MAX811_EUS_T
SOT143

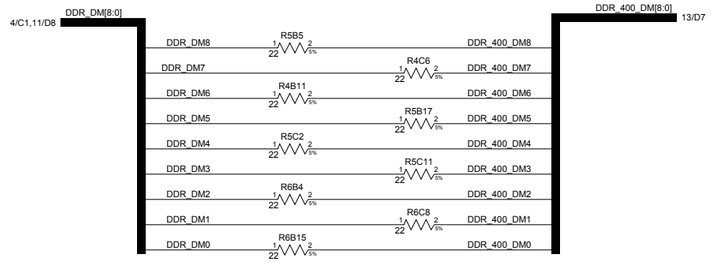
U2E2
SN74LVC2G66

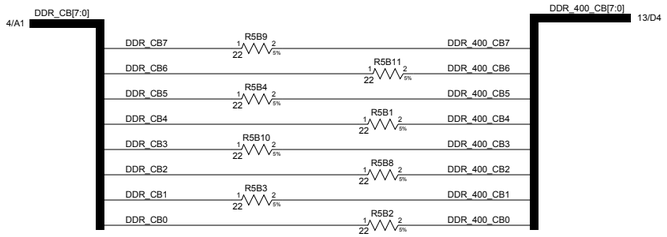
U3E1
74LVC2G08
GND;4 P3_3V;8

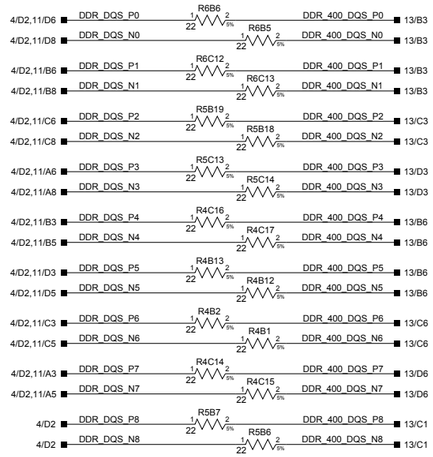
U1B1, U1B2
74LVC125AD
GND;7 P3_3V;14

C9M1, C9M3 0.1UF 16V









	DESIGN ENGINEER: SCD HARDWARE ENGINEERING	DESIGN NAME: 80331 DDR-II 400 CRB	SHEET TITLE: DDR-II 400 SERIES TERMINATION		DATE MODIFIED: 9-23-2004_9:04	VERSION: P 1.0	SHEET 10 OF 21

DDR_DM[8:0]
4/C1,10/D4
DDR_DQ[63:0]
4/C1,10/D7

J4M1

NC	A1	OD1	OD0	B1	NC
DDR_DM0	A2	OD3	OD2	B2	NC
	A3	GND0	GND9	B3	
DDR_DQ0	A4	OD5	OD4	B4	NC
DDR_DQ5	A5	OD7	OD6	B5	DDR_DQ4
	A6	GND1	GND10	B6	
DDR_DQ1	A7	OD9	OD8	B7	NC
DDR_DQ6	A8	OD11	OD10	B8	DDR_DQ7
	A9	GND2	GND11	B9	
DDR_DQ2	A10	OD13	OD12	B10	NC
DDR_DQ3	A11	OD15	OD14	B11	NC
	A12	GND3	GND12	B12	
4/D2,10/B4 DDR_DQS_N0	A13	OD16_CKN	OD16_CKP	B13	DDR_DQS_P0 4/D2,10/B4
	A14	GND4	GND13	B14	
DDR_DM2	A15	ED1	ED0	B15	NC
DDR_DQ21	A16	ED3	ED2	B16	NC
	A17	GND5	GND14	B17	
DDR_DQ16	A18	ED5	ED4	B18	NC
DDR_DQ17	A19	ED7	ED6	B19	NC
	A20	GND6	GND15	B20	
DDR_DQ18	A21	ED9	ED8	B21	DDR_DQ20
DDR_DQ23	A22	ED11	ED10	B22	NC
	A23	GND7	GND16	B23	
DDR_DQ22	A24	ED13	ED12	B24	NC
DDR_DQ19	A25	ED15	ED14	B25	NC
	A26	GND8	GND17	B26	
4/D2,10/B4 DDR_DQS_N2	A27	ED16_CKN	ED16_CKP	B27	DDR_DQS_P2 4/D2,10/B4
	n.c.	Align	Align	n.c.	
	n.c.	Align	Align	n.c.	

Logic Analyzer Conn
Soft Touch*
AGILENT*_LA_E5390A
GND NO POP GND

J4N1

NC	A1	OD1	OD0	B1	NC
DDR_DQ12	A2	OD3	OD2	B2	NC
	A3	GND0	GND9	B3	
DDR_DQ13	A4	OD5	OD4	B4	NC
DDR_DQ8	A5	OD7	OD6	B5	DDR_DM1
	A6	GND1	GND10	B6	
DDR_DQ9	A7	OD9	OD8	B7	NC
DDR_DQ10	A8	OD11	OD10	B8	NC
	A9	GND2	GND11	B9	
DDR_DQ14	A10	OD13	OD12	B10	NC
DDR_DQ15	A11	OD15	OD14	B11	DDR_DQ11
	A12	GND3	GND12	B12	
4/D2,10/B4 DDR_DQS_N1	A13	OD16_CKN	OD16_CKP	B13	DDR_DQS_P1 4/D2,10/B4
	A14	GND4	GND13	B14	
DDR_DQ29	A15	ED1	ED0	B15	NC
DDR_DQ28	A16	ED3	ED2	B16	NC
	A17	GND5	GND14	B17	
DDR_DQ24	A18	ED5	ED4	B18	NC
DDR_DM3	A19	ED7	ED6	B19	NC
	A20	GND6	GND15	B20	
DDR_DQ27	A21	ED9	ED8	B21	DDR_DQ25
DDR_DQ31	A22	ED11	ED10	B22	NC
	A23	GND7	GND16	B23	
DDR_DQ30	A24	ED13	ED12	B24	NC
DDR_DQ26	A25	ED15	ED14	B25	NC
	A26	GND8	GND17	B26	
4/D2,10/B4 DDR_DQS_N3	A27	ED16_CKN	ED16_CKP	B27	DDR_DQS_P3 4/D2,10/B4
	n.c.	Align	Align	n.c.	
	n.c.	Align	Align	n.c.	

Logic Analyzer Conn
Soft Touch*
AGILENT*_LA_E5390A
GND NO POP GND

J5M1

DDR_DM5	A1	OD1	OD0	B1	NC
DDR_DQ45	A2	OD3	OD2	B2	DDR_DQ41
	A3	GND0	GND9	B3	
DDR_DQ44	A4	OD5	OD4	B4	NC
DDR_DQ40	A5	OD7	OD6	B5	NC
	A6	GND1	GND10	B6	
DDR_DQ43	A7	OD9	OD8	B7	NC
DDR_DQ46	A8	OD11	OD10	B8	NC
	A9	GND2	GND11	B9	
DDR_DQ42	A10	OD13	OD12	B10	NC
DDR_DQ47	A11	OD15	OD14	B11	NC
	A12	GND3	GND12	B12	
4/D2,10/A4 DDR_DQS_N5	A13	OD16_CKN	OD16_CKP	B13	DDR_DQS_P5 4/D2,10/A4
	A14	GND4	GND13	B14	
DDR_DQ54	A15	ED1	ED0	B15	DDR_DM6
DDR_DQ52	A16	ED3	ED2	B16	NC
	A17	GND5	GND14	B17	
DDR_DQ53	A18	ED5	ED4	B18	NC
DDR_DQ49	A19	ED7	ED6	B19	NC
	A20	GND6	GND15	B20	
DDR_DQ51	A21	ED9	ED8	B21	NC
DDR_DQ50	A22	ED11	ED10	B22	DDR_DQ48
	A23	GND7	GND16	B23	
DDR_DQ55	A24	ED13	ED12	B24	NC
NC	A25	ED15	ED14	B25	NC
	A26	GND8	GND17	B26	
4/D2,10/A4 DDR_DQS_N6	A27	ED16_CKN	ED16_CKP	B27	DDR_DQS_P6 4/D2,10/A4
	n.c.	Align	Align	n.c.	
	n.c.	Align	Align	n.c.	

Logic Analyzer Conn
Soft Touch*
AGILENT*_LA_E5390A
GND NO POP GND

J5N1

DDR_DQ36	A1	OD1	OD0	B1	NC
DDR_DQ33	A2	OD3	OD2	B2	DDR_DQ37
	A3	GND0	GND9	B3	
DDR_DM4	A4	OD5	OD4	B4	NC
DDR_DQ35	A5	OD7	OD6	B5	NC
	A6	GND1	GND10	B6	
DDR_DQ32	A7	OD9	OD8	B7	NC
DDR_DQ39	A8	OD11	OD10	B8	NC
	A9	GND2	GND11	B9	
DDR_DQ38	A10	OD13	OD12	B10	DDR_DQ34
NC	A11	OD15	OD14	B11	NC
	A12	GND3	GND12	B12	
4/D2,10/A4 DDR_DQS_N4	A13	OD16_CKN	OD16_CKP	B13	DDR_DQS_P4 4/D2,10/B4
	A14	GND4	GND13	B14	
DDR_DQ57	A15	ED1	ED0	B15	NC
DDR_DQ61	A16	ED3	ED2	B16	DDR_DQ60
	A17	GND5	GND14	B17	
DDR_DM7	A18	ED5	ED4	B18	NC
DDR_DQ56	A19	ED7	ED6	B19	NC
	A20	GND6	GND15	B20	
DDR_DQ59	A21	ED9	ED8	B21	NC
DDR_DQ58	A22	ED11	ED10	B22	NC
	A23	GND7	GND16	B23	
DDR_DQ63	A24	ED13	ED12	B24	NC
DDR_DQ62	A25	ED15	ED14	B25	NC
	A26	GND8	GND17	B26	
4/D2,10/A4 DDR_DQS_N7	A27	ED16_CKN	ED16_CKP	B27	DDR_DQS_P7 4/D2,10/A4
	n.c.	Align	Align	n.c.	
	n.c.	Align	Align	n.c.	

Logic Analyzer Conn
Soft Touch*
AGILENT*_LA_E5390A
GND NO POP GND

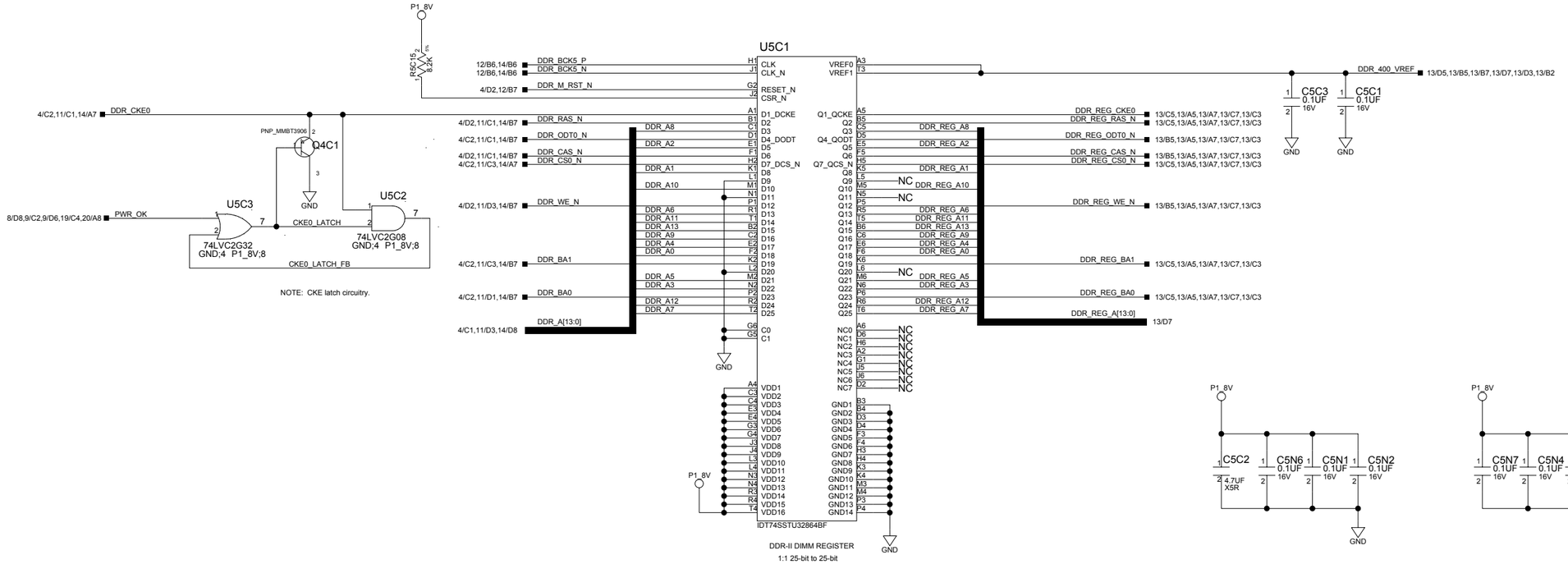
DDR_A[13:0]
4/C1,12/C5,14/D8

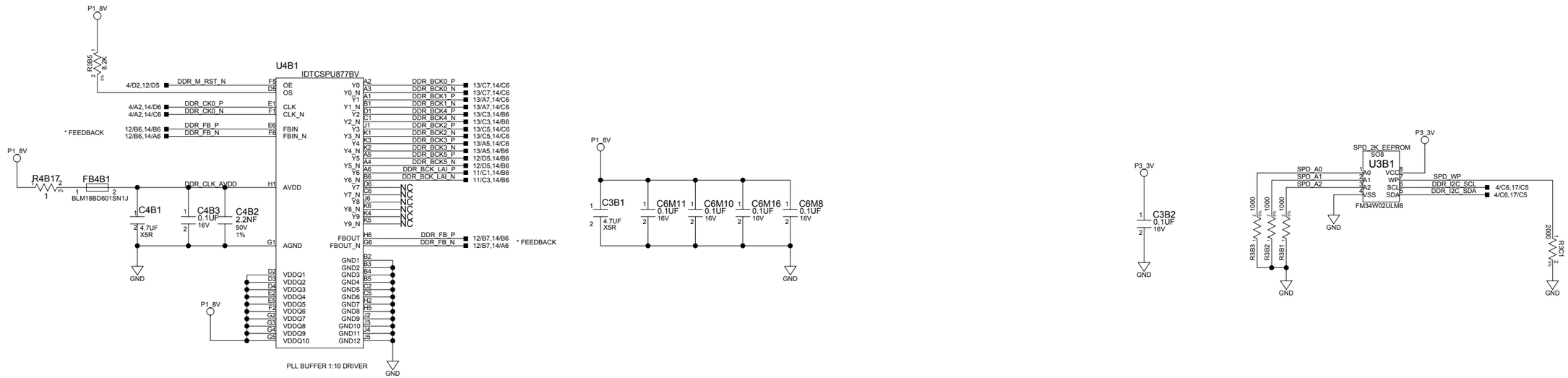
J5N2

NC	A1	OD1	OD0	B1	NC
NC	A2	OD3	OD2	B2	NC
	A3	GND0	GND9	B3	
NC	A4	OD5	OD4	B4	DDR_A7
DDR_A11	A5	OD7	OD6	B5	DDR_A12
	A6	GND1	GND10	B6	
DDR_A6	A7	OD9	OD8	B7	DDR_BA0 4/C2,12/C5,14/B7
NC	A8	OD11	OD10	B8	NC
	A9	GND2	GND11	B9	
4/D2,12/D5,14/B7 DDR_WE_N	A10	OD13	OD12	B10	DDR_A3
DDR_A5	A11	OD15	OD14	B11	DDR_A10
	A12	GND3	GND12	B12	
NC	A13	OD16_CKN	OD16_CKP	B13	NC
	A14	GND4	GND13	B14	
4/C2,12/C5,14/B7 DDR_BA1	A15	ED1	ED0	B15	DDR_A1
4/C2,12/D5,14/A7 DDR_CS0_N	A16	ED3	ED2	B16	DDR_CAS_N 4/D2,12/D5,14/B7
	A17	GND5	GND14	B17	
DDR_A0	A18	ED5	ED4	B18	DDR_A2
DDR_A4	A19	ED7	ED6	B19	DDR_ODT0_N 4/C2,12/D5,14/B7
	A20	GND6	GND15	B20	NC
NC	A21	ED9	ED8	B21	NC
DDR_A8	A22	ED11	ED10	B22	NC
	A23	GND7	GND16	B23	
DDR_A9	A24	ED13	ED12	B24	DDR_RAS_N 4/D2,12/D5,14/B7
DDR_A13	A25	ED15	ED14	B25	DDR_CKE0 4/C2,12/D6,14/A7
	A26	GND8	GND17	B26	
12/B6,14/B6 DDR_BCK_LAI_N	A27	ED16_CKN	ED16_CKP	B27	DDR_BCK_LAI_P 12/B6,14/B6
	n.c.	Align	Align	n.c.	
	n.c.	Align	Align	n.c.	

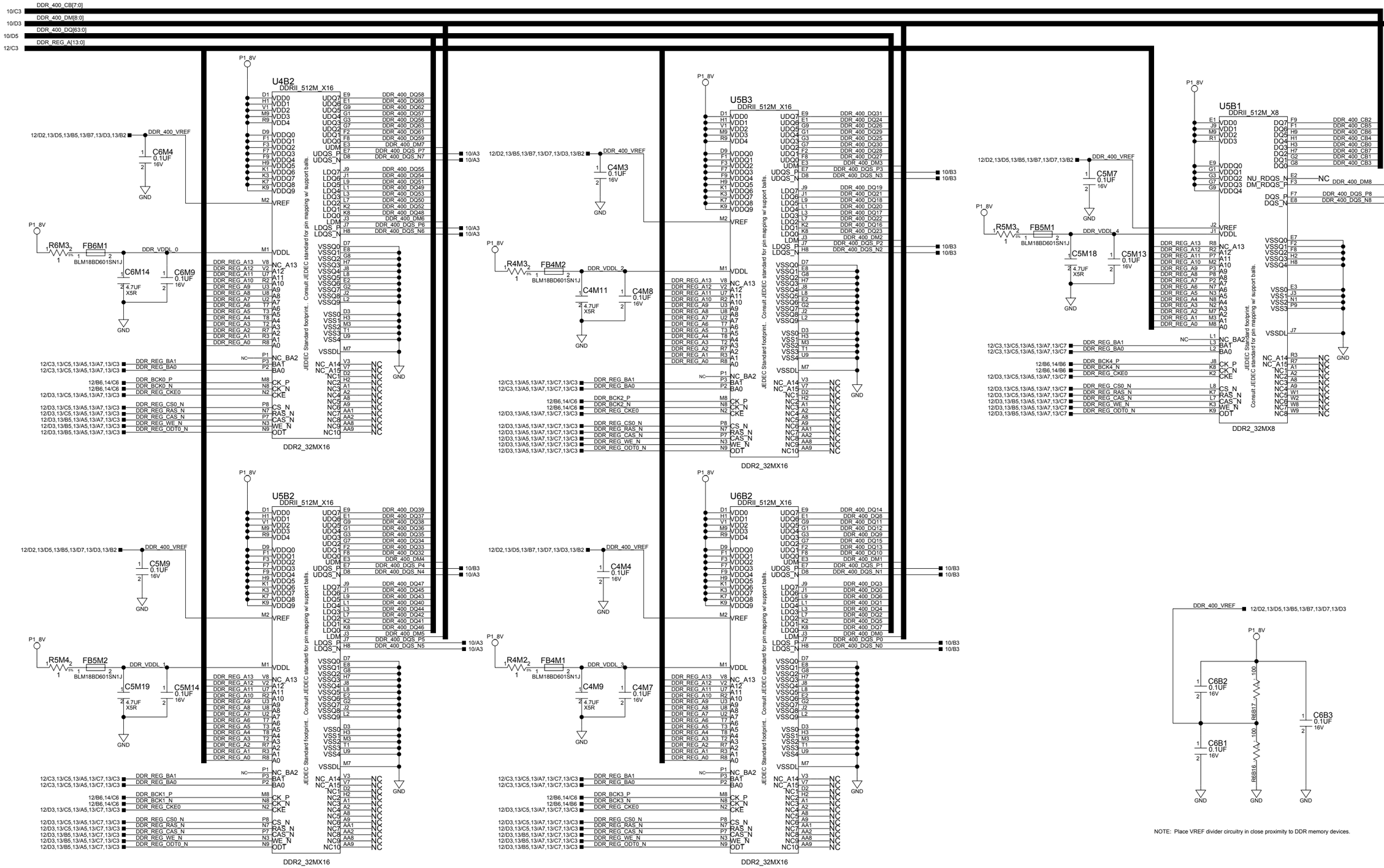
Logic Analyzer Conn
Soft Touch*
AGILENT*_LA_E5390A
GND NO POP GND

	DESIGN ENGINEER: SCD HARDWARE ENGINEERING	DESIGN NAME: 80331 DDR-II 400 CRB	SHEET TITLE: DDR-II 400 AGILENT LAI PROBES	DATE MODIFIED: 9-23-2004_9:31	VERSION: P 1.0	SHEET 11 OF 21



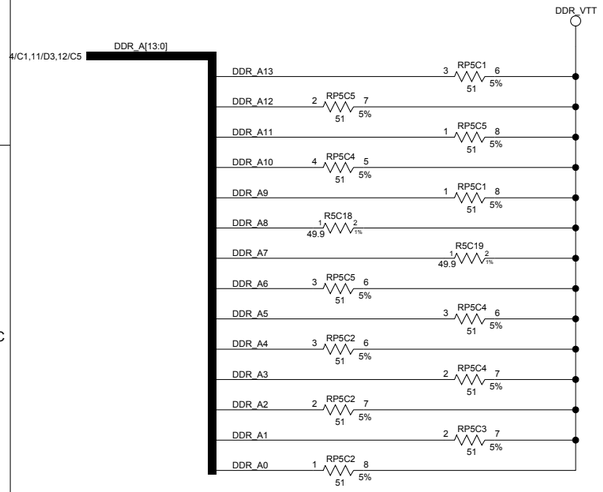


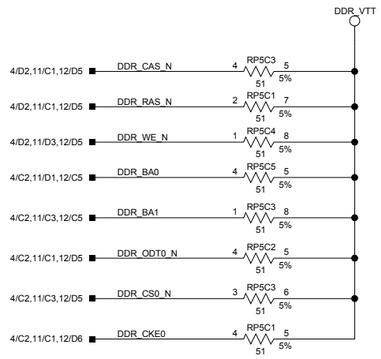
	DESIGN ENGINEER: SCD HARDWARE ENGINEERING	DESIGN NAME: 80331 DDR-II 400 CRB	SHEET TITLE: PLL BUFFER / DDR-II 400 REGISTER / SPD	DATE MODIFIED: 9-23-2004_9:04	VERSION: P 1.0	SHEET 12 OF 21



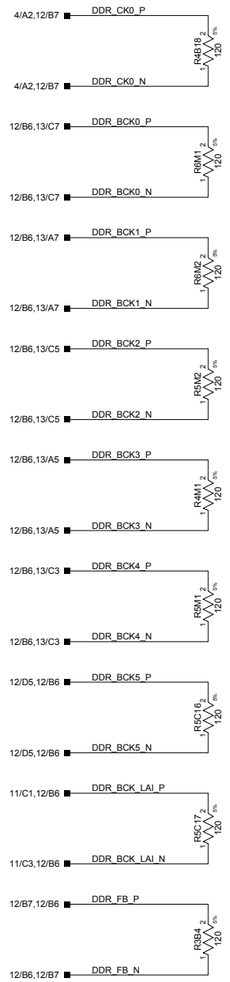
	DESIGN ENGINEER: SCD HARDWARE ENGINEERING	DESIGN NAME: 80331 DDR-II 400 CRB	SHEET TITLE: DDR-II 400 MEMORY	DATE MODIFIED: 9-23-2004_9:04	VERSION: P 1.0	SHEET 13 OF 21

DDR VTT Termination

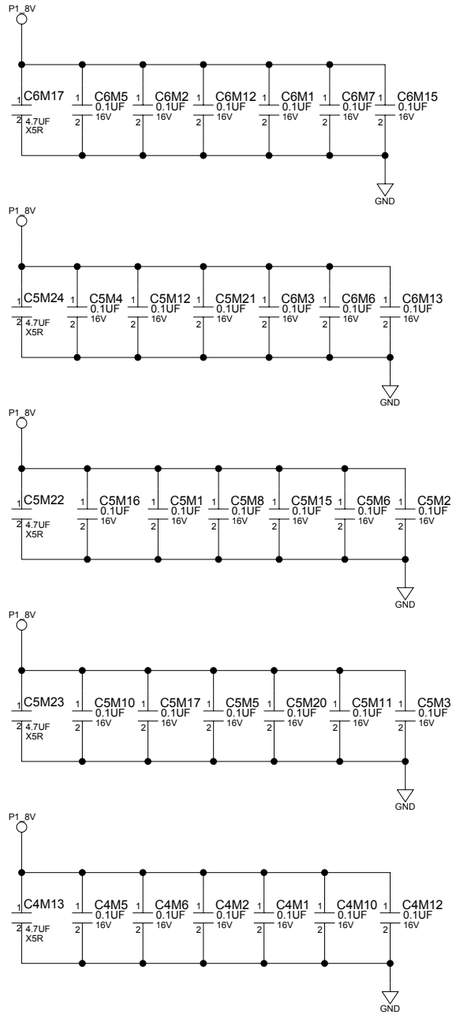




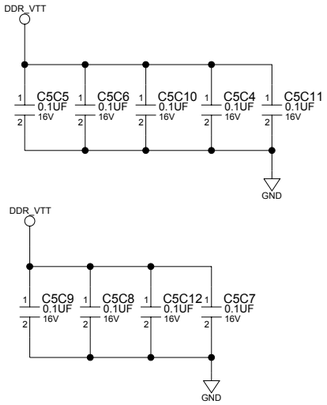
NOTE: Place termination as close to the input as possible.



DDR VDD Decoupling



DDR VTT Decoupling



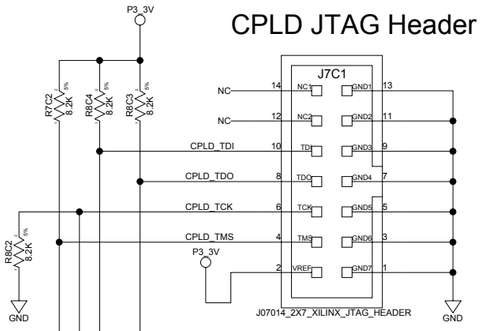
	DESIGN ENGINEER: SCD HARDWARE ENGINEERING	DESIGN NAME: 80331 DDR-II 400 CRB	SHEET TITLE: DDR-II 400 TERMINATION	DATE MODIFIED: 9-23-2004_9:04	VERSION: P 1.0	SHEET 14 OF 21

S7C1 SWITCH #	SIGNAL NAME	SWITCH SETTING	SIGNAL VALUE	STRAPPING DESCRIPTION
1	PBI_AD3	* PUSHED IN AT THE TOP	0	SECONDARY PCI BUS SET TO 100 MHz
		PUSHED IN AT THE BOTTOM	1	SECONDARY PCI BUS SET TO 133 MHz
2	PBI_AD5	PUSHED IN AT THE TOP	0	HOLD IOP CORE IN RESET
		* PUSHED IN AT THE BOTTOM	1	ALLOW IOP CORE TO EXECUTE
3	PBI_AD6	PUSHED IN AT THE TOP	0	CONFIGURATION RETRY DISABLED - USE WHEN BOOTING IN A BACKPLANE
		* PUSHED IN AT THE BOTTOM	1	CONFIGURATION RETRY ENABLE - USE WHEN BOOTING IN A HOST
4	PBI_AD0	PUSHED IN AT THE TOP	0	DISABLE THE 80331 PCI-TO-PCI BRIDGE
		* PUSHED IN AT THE BOTTOM	1	ENABLE THE 80331 PCI-TO-PCI BRIDGE
5	PBI_A0	PUSHED IN AT THE TOP	0	DISABLE PRIVATE DEVICES
		* PUSHED IN AT THE BOTTOM	1	ENABLE PRIVATE DEVICES - ALLOWS USE OF DEVICES ON SECONDARY PCI BUS
6	PBI_A1	PUSHED IN AT THE TOP	0	NORMAL MEMORY ADDRESSING MODE ON THE SECONDARY PCI BUS
		* PUSHED IN AT THE BOTTOM	1	PRIVATE MEMORY SPACE ENABLED ON THE SECONDARY PCI BUS
7	PBI_A2	PUSHED IN AT THE TOP	0	32-bit PRIMARY PCI-X BUS WIDTH
		* PUSHED IN AT THE BOTTOM	1	64-bit PRIMARY PCI-X BUS WIDTH
8	N/C	PUSHED IN AT THE TOP	0	SPARE SWITCH, NO INFLUENCE TO STRAPPING OPTIONS
		* PUSHED IN AT THE BOTTOM	1	SPARE SWITCH, NO INFLUENCE TO STRAPPING OPTIONS
9	N/C	PUSHED IN AT THE TOP	0	SPARE SWITCH, NO INFLUENCE TO STRAPPING OPTIONS
		* PUSHED IN AT THE BOTTOM	1	SPARE SWITCH, NO INFLUENCE TO STRAPPING OPTIONS
10	3_3V	PUSHED IN AT THE TOP	0	by-16 MODE BUS WIDTH FOR PBI MEMORY BOOT WINDOW
		* PUSHED IN AT THE BOTTOM	1	by-8 MODE BUS WIDTH FOR PBI MEMORY BOOT WINDOW

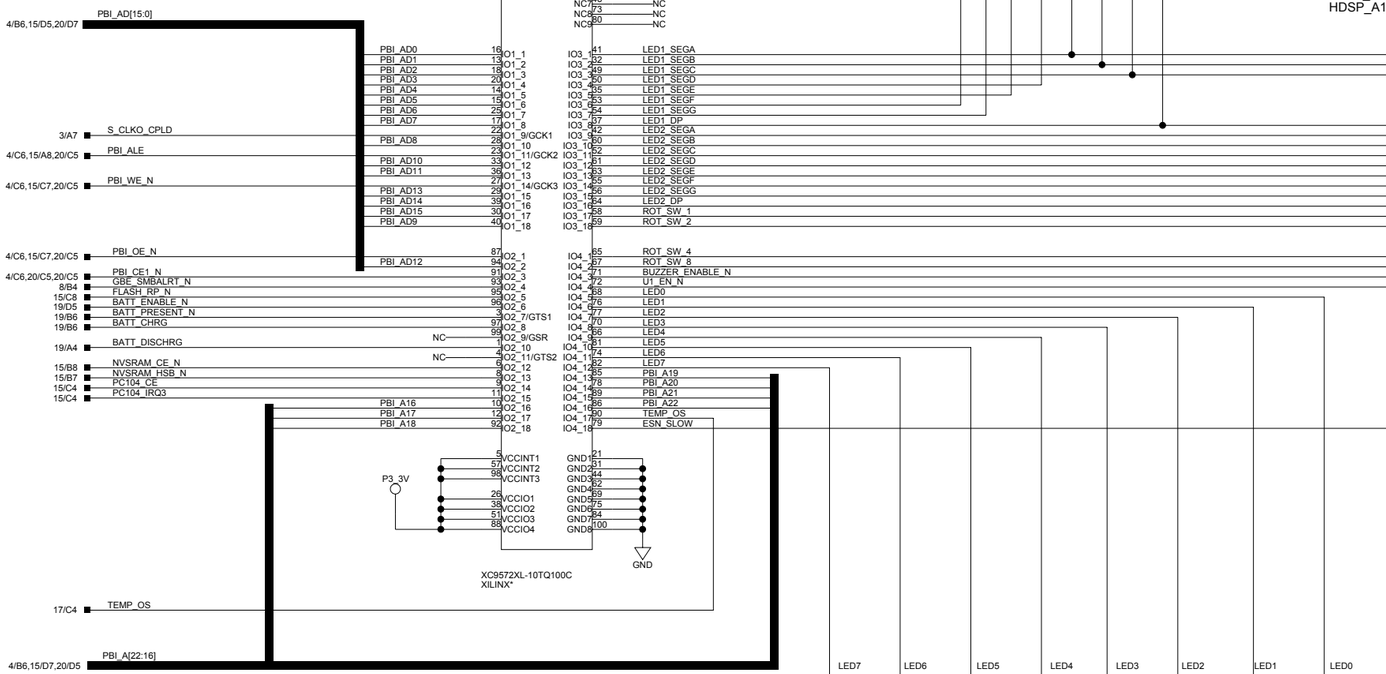
* DEFAULT SWITCH SETTINGS WHEN BOOTING WITH RedBoot FIRMWARE SOFTWARE.

DESIGN ENGINEER: SCD HARDWARE ENGINEERING	DESIGN NAME: 80331 DDR-II 400 CRB	SHEET TITLE: NV AND FLASH MEMORY / PBI / CONFIGURATION STRAPING	DATE MODIFIED: 9-23-2004_9:21	VERSION: P 1.0	SHEET 15 OF 21

CPLD JTAG Header

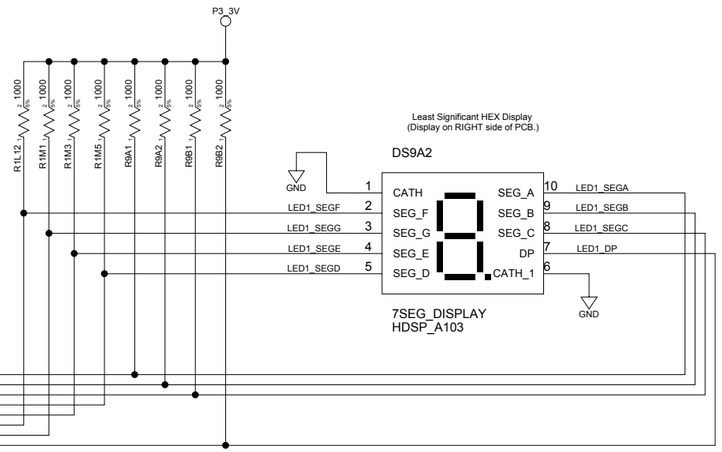


CPLD

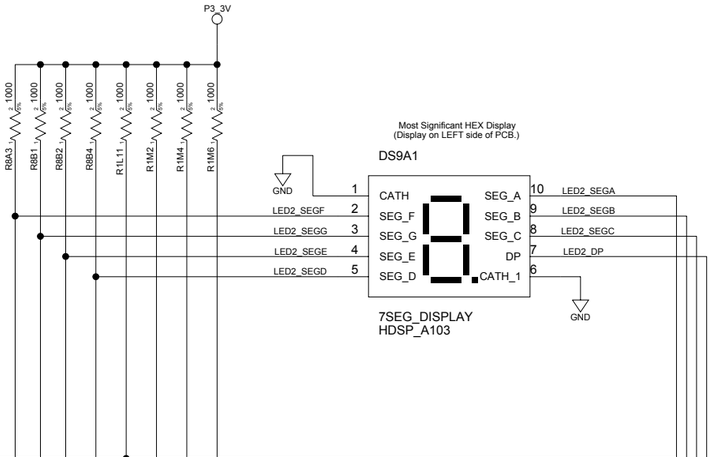


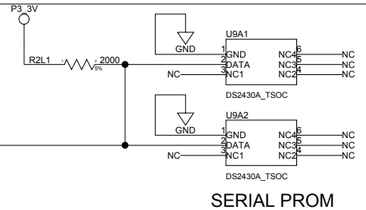
NOTE: When running RedBoot, a proper boot results with an output of A1 on hex display.
NOTE: When core is held in reset (default setting), no output results on hex display.

Least Significant HEX Display
(Display on RIGHT side of PCB.)



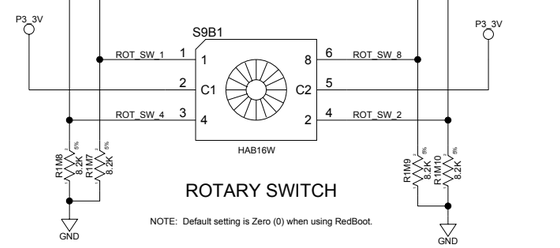
Most Significant HEX Display
(Display on LEFT side of PCB.)





SERIAL PROM

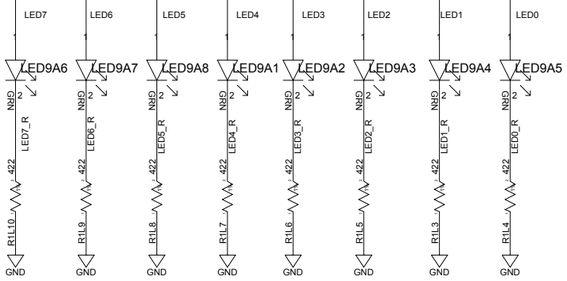
NOTE: Embedded Serial Numbers.

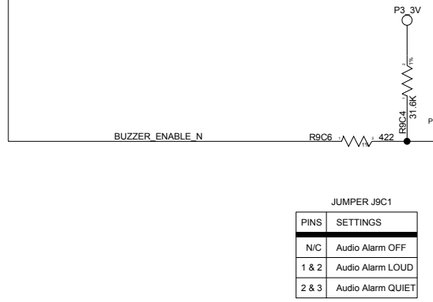


ROTARY SWITCH

NOTE: Default setting is Zero (0) when using RedBoot.

MISC. LEDS

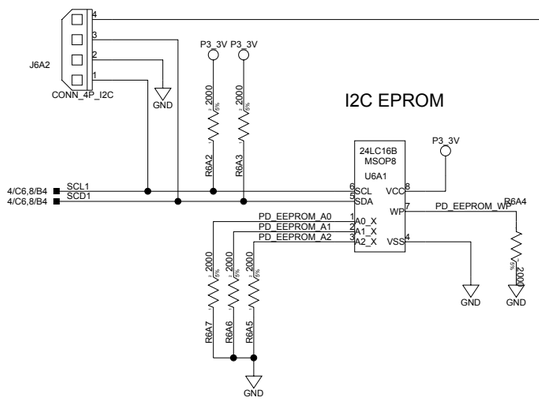




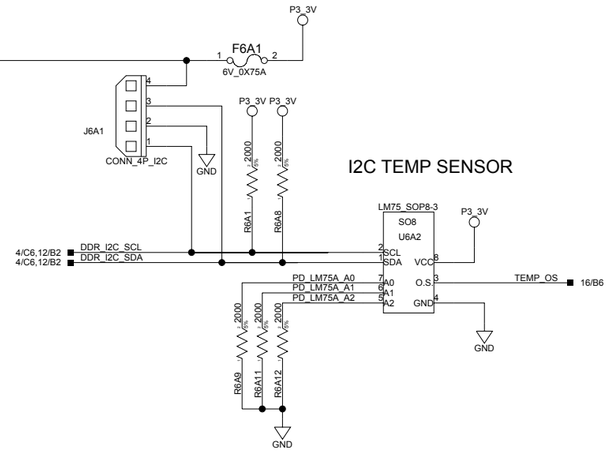
AUDIO ALARM

	DESIGN ENGINEER: SCD HARDWARE ENGINEERING	DESIGN NAME: 80331 DDR-II 400 CRB	SHEET TITLE: CPLD / HEX DISPLAYS / EPROMS / ROTARY SWITCH / BUZZER	DATE MODIFIED: 9-23-2004_8:59	VERSION: P 1.0	SHEET 16 OF 21

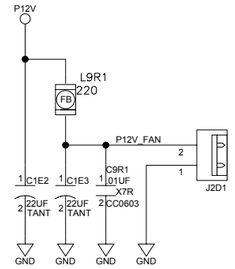
I2C EPROM HEADER



I2C TEMP SENSOR HEADER

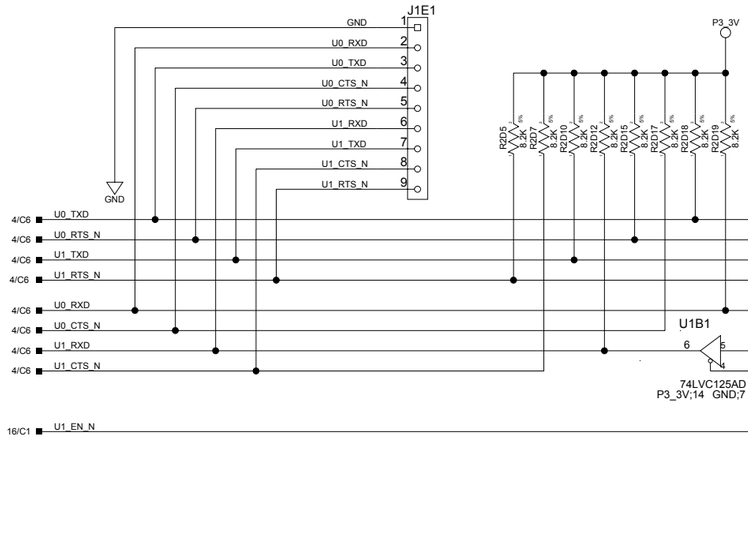


FAN POWER HEADER



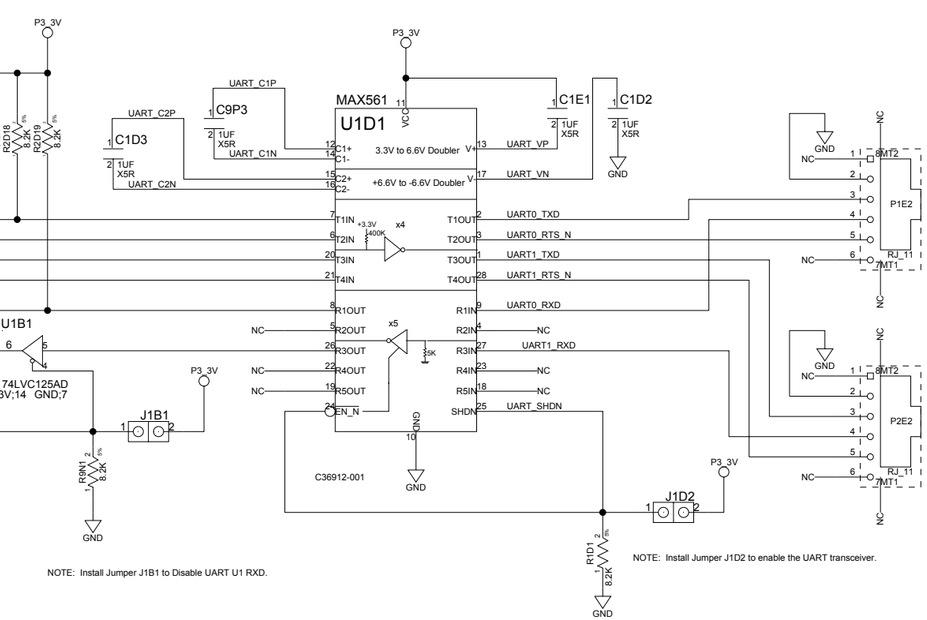
NOTE:
Header J2D1 is to be utilized for active IOP cooling.
The active heat sink part number is: C51829-001.
The passive IOP cooling solution requires at least 200 lfpm across its surface.
The passive heat sink part number is: C50161-001.

UART HEADER



NOTE: Install Jumper J1B1 to Disable UART U1 RXD.

RS-232 TRANSCEIVER



NOTE: Install Jumper J1D2 to enable the UART transceiver.

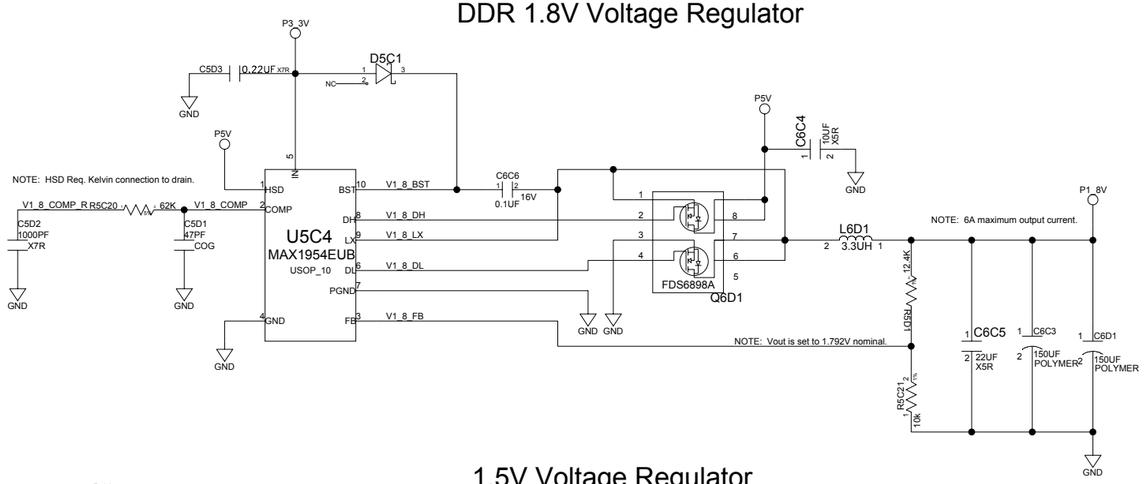
RJ11 Dual Serial Port Connector

NOTE: Lower RJ11 connector on PCB.

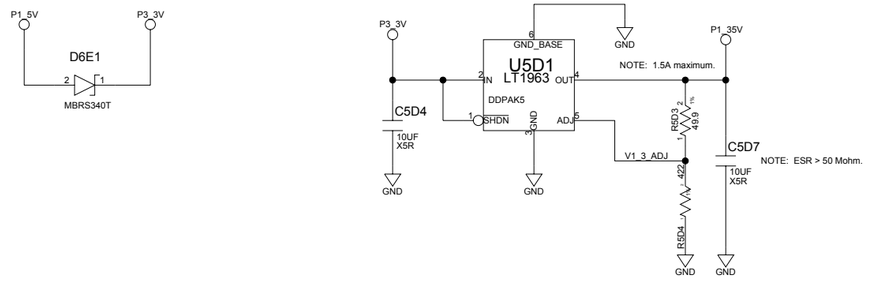
NOTE: Upper RJ11 connector on PCB.

	DESIGN ENGINEER: SCD HARDWARE ENGINEERING	DESIGN NAME: 80331 DDR-II 400 CRB	SHEET TITLE: I2C INTERFACE / UART TXRX / MISC. HEADERS	DATE MODIFIED: 9-23-2004_9:04	VERSION: P 1.0	SHEET 17 OF 21

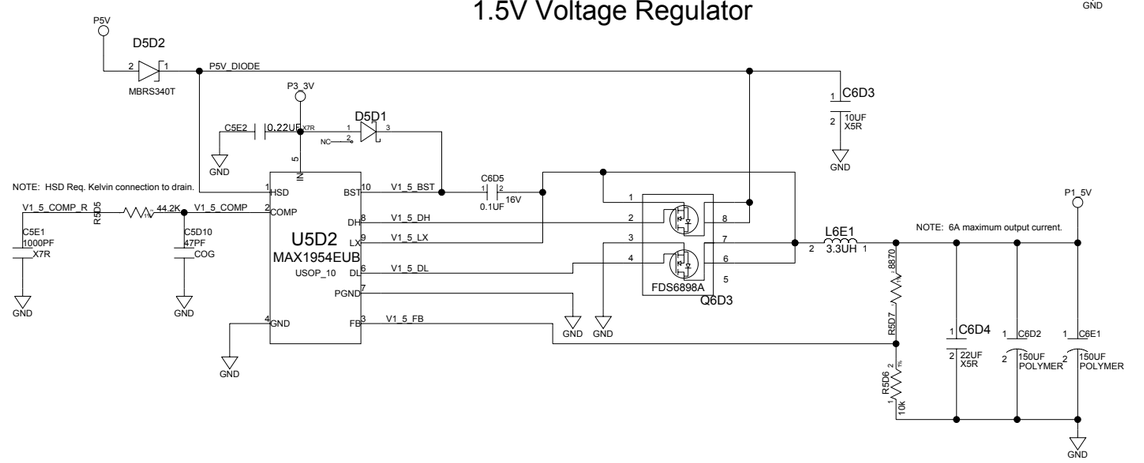
DDR 1.8V Voltage Regulator



1.35V Voltage Regulator

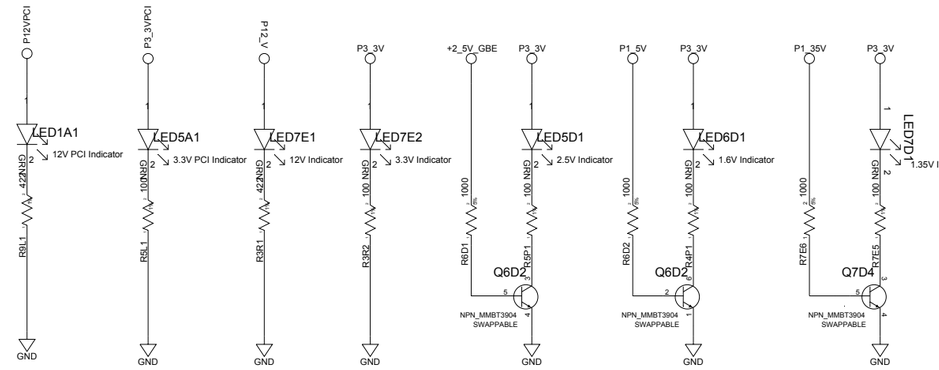


1.5V Voltage Regulator



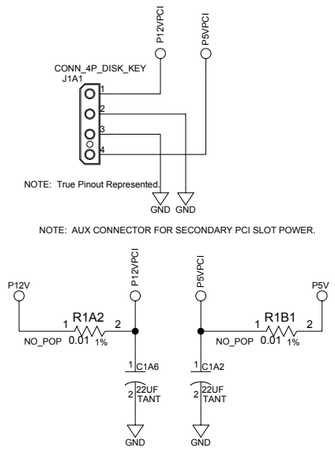
LED Indicators

NOTE: Identify indicators in silk-screen.

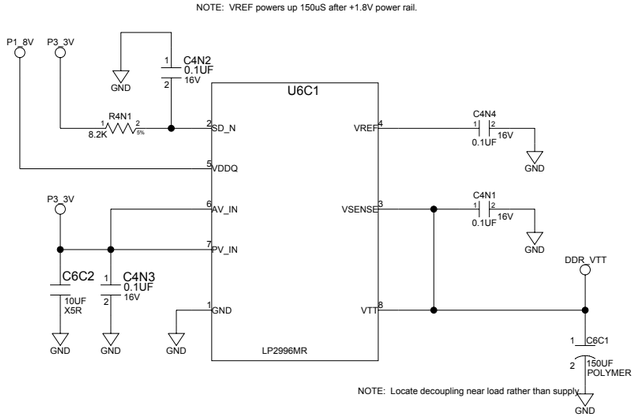


Secondary PCI-X Expansion Slot Power Connector

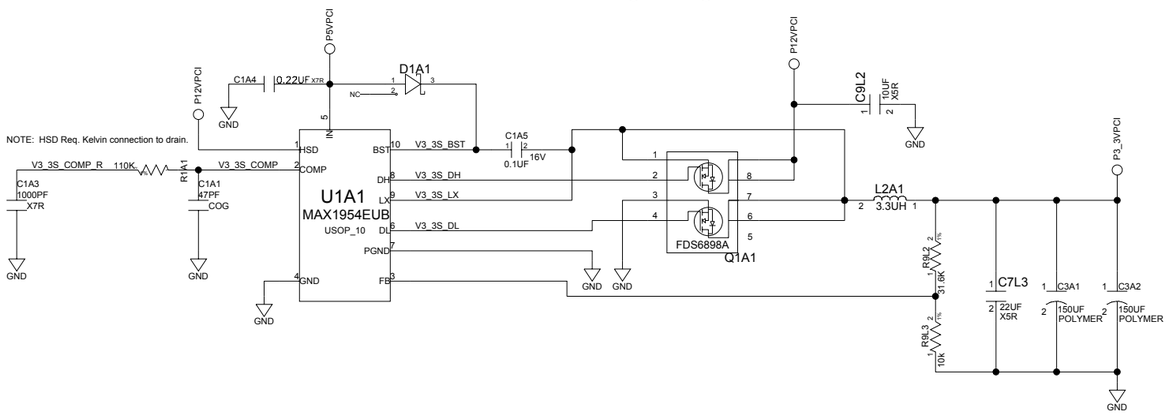
NOTE: Auxilary power MUST be connected to use secondary PCI slot.



DDR VTT Voltage Regulator



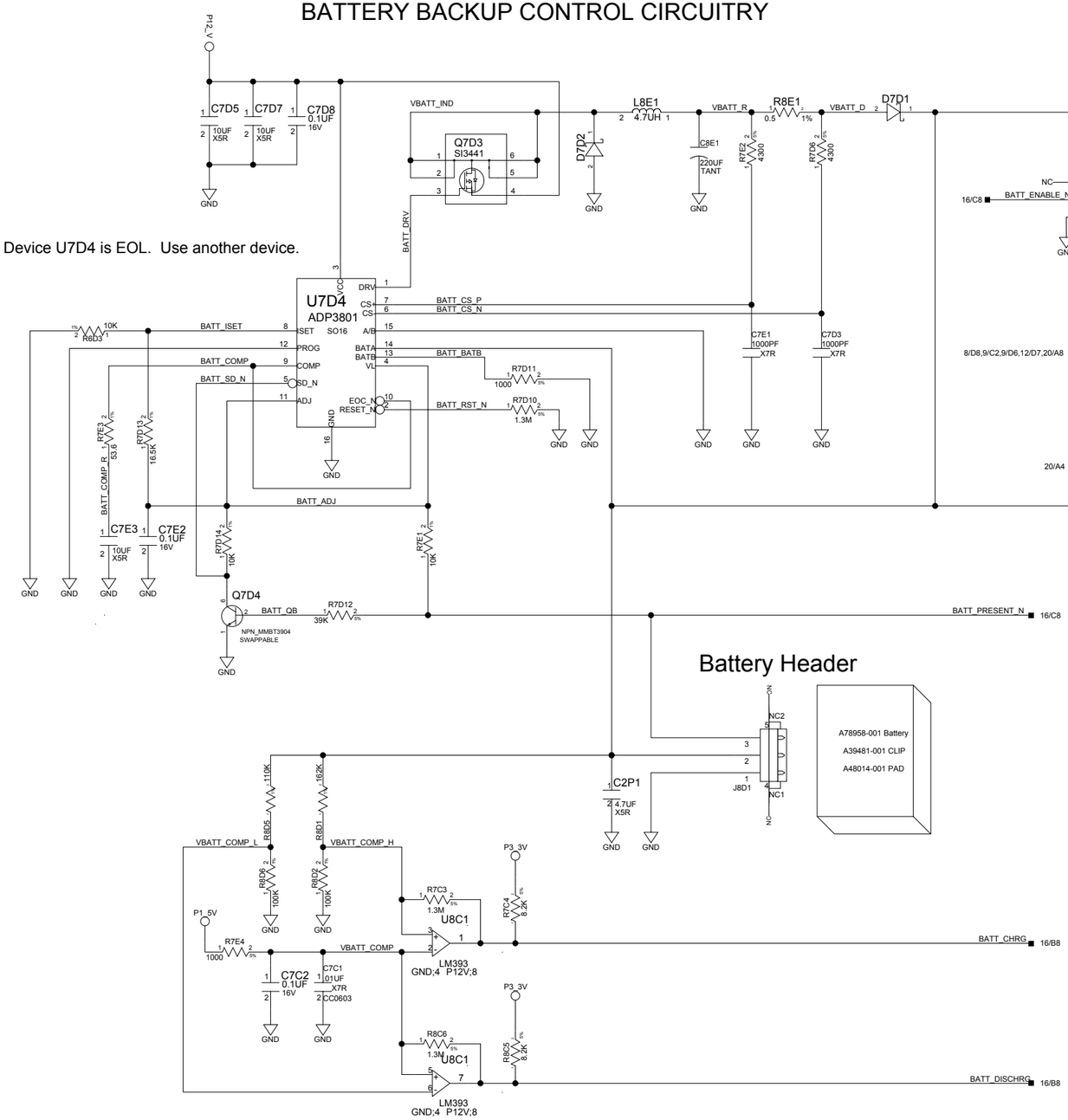
3.3V Voltage Regulator for PCI Slot



DESIGN ENGINEER:	DESIGN NAME:	SHEET TITLE:	DATE MODIFIED:	VERSION:	SHEET
SCD HARDWARE ENGINEERING	80331 DDR-II 400 CRB	VOLTAGE REGULATORS / PWR INDICATORS	9-23-2004_9:04	P 1.0	18 OF 21

BATTERY BACKUP CONTROL CIRCUITRY

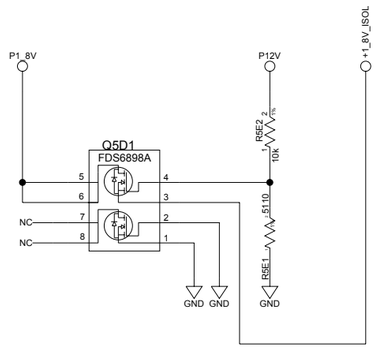
NOTE: Device U7D4 is EOL. Use another device.



Battery Header

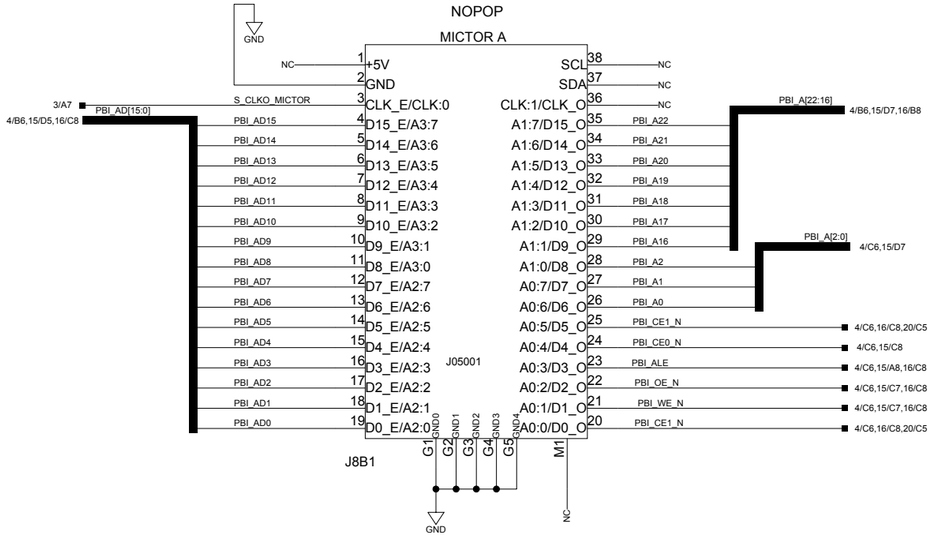
DDR SELF-REFRESH LINEAR REGULATOR

IOP 1.8V ISOLATION CIRCUITRY

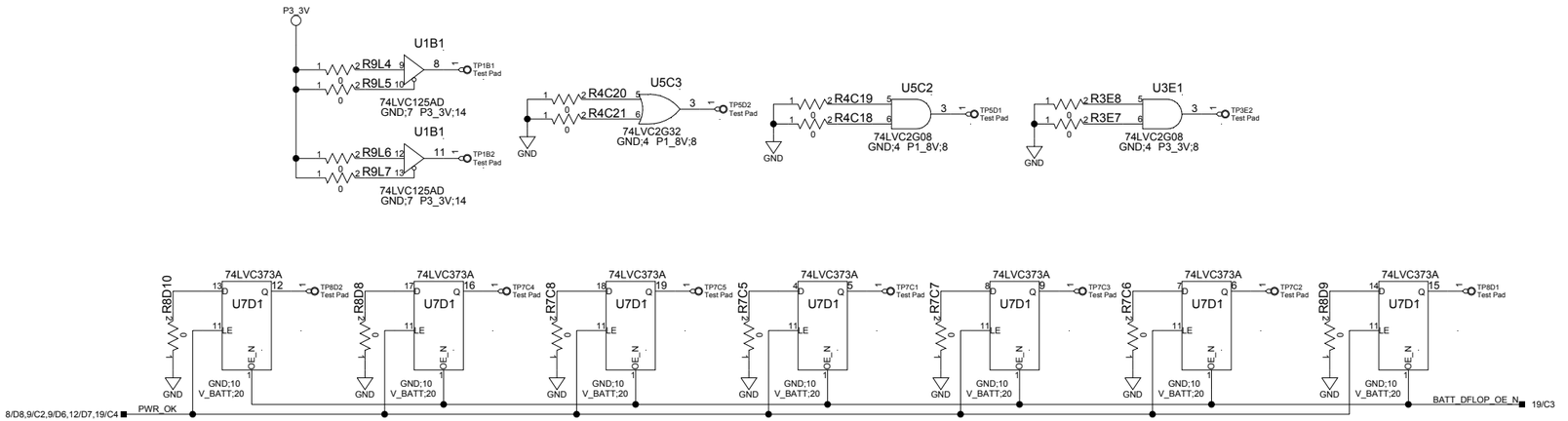


	DESIGN ENGINEER: SCD HARDWARE ENGINEERING	DESIGN NAME: 80331 DDR-II 400 CRB	SHEET TITLE: DDR-II 400 BATTERY BACKUP	DATE MODIFIED: 9-23-2004_9:04	VERSION: P 1.0	SHEET 19 OF 21

DEBUG CONNECTOR



UNUSED PARTS



	DESIGN ENGINEER: SCD HARDWARE ENGINEERING	DESIGN NAME: 80331 DDR-II 400 CRB	SHEET TITLE: UNUSED PARTS / DEBUG - MICTOR CONNECTORS	DATE MODIFIED: 9-23-2004_9:29	VERSION: P 1.0	SHEET 20 OF 21

Version History

Ver 1.0 -- Proto Build	09/29/04