

80331 DDR DIMM CUSTOMER REFERENCE BOARD

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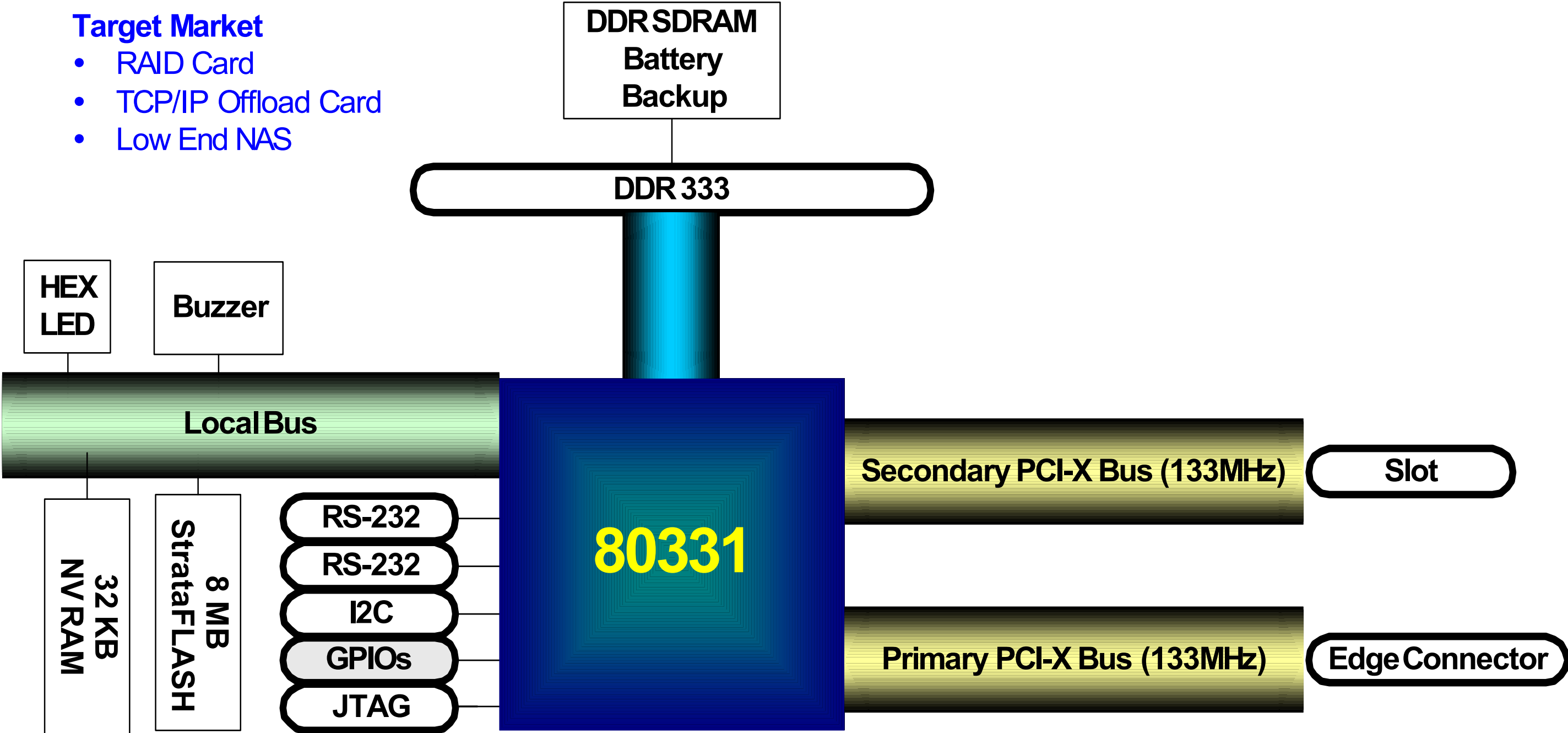
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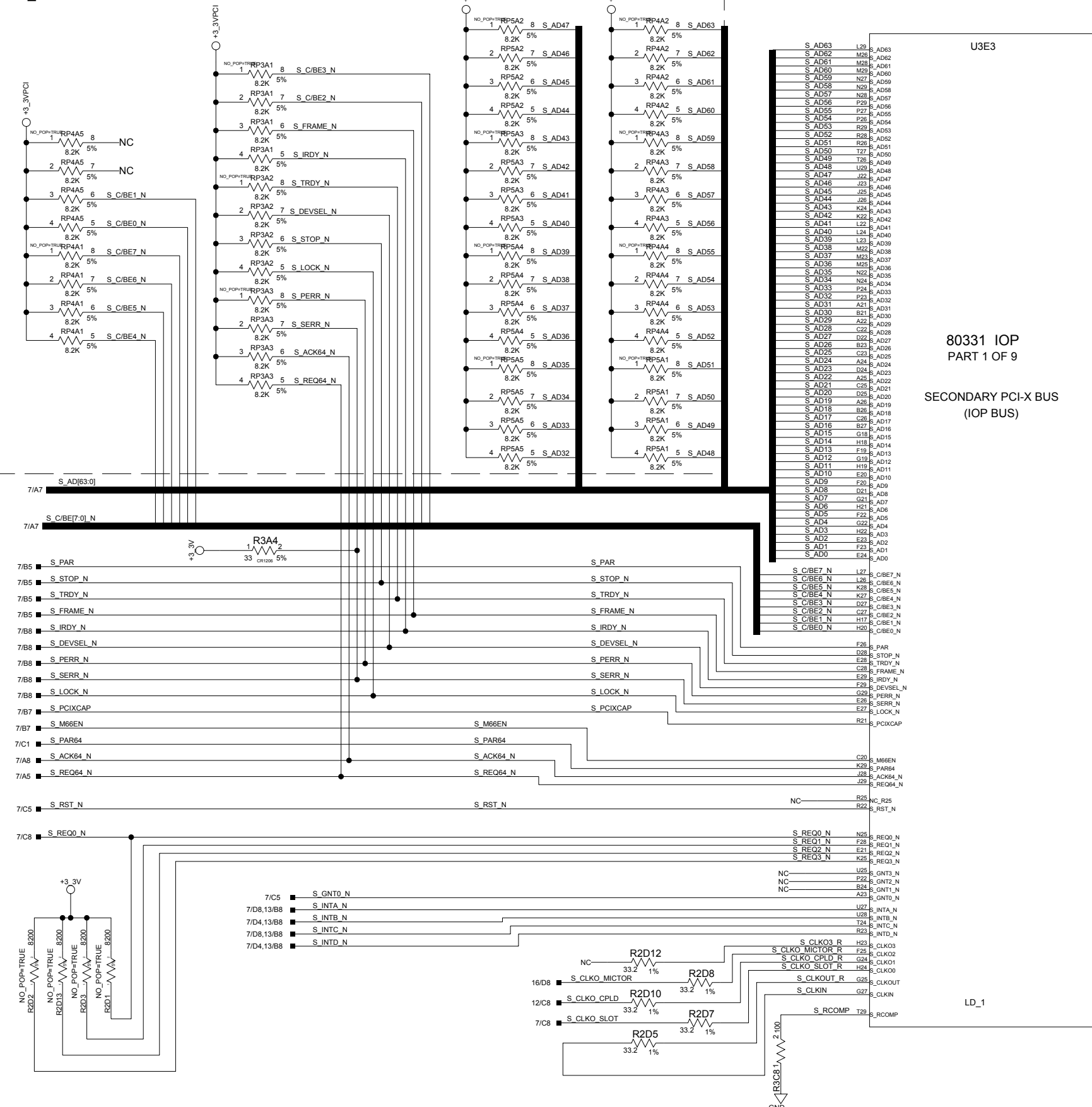
80331 DDR DIMM CUSTOMER REFERENCE BOARD

Target Market

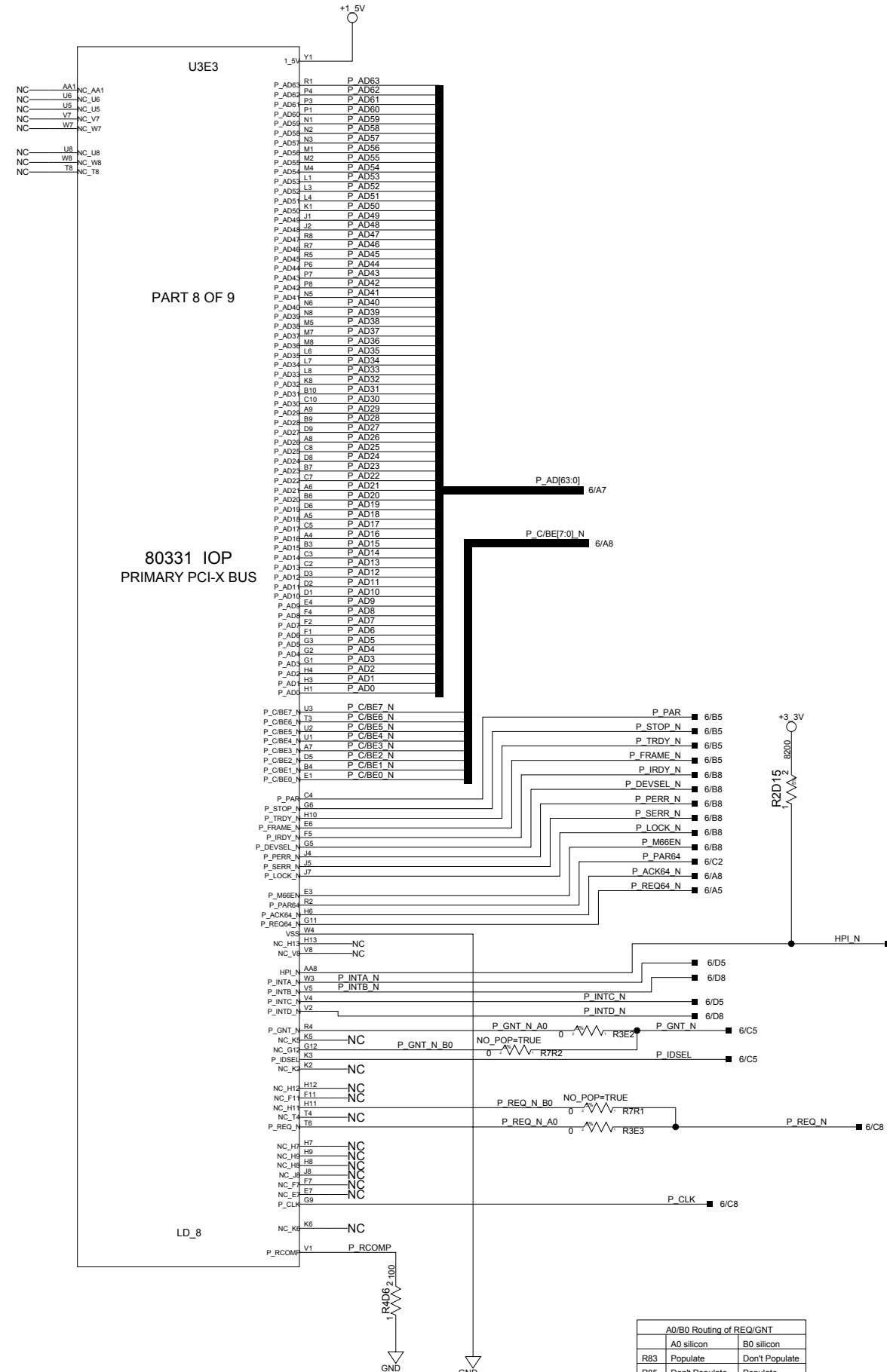
- RAID Card
- TCP/IP Offload Card
- Low End NAS



Place Resistor Packs near PCI Connector
NO_POP RPACKS



80331 IOP
PART 1 OF 9
SECONDARY PCI-X BUS
(IOP BUS)



80331 IOP
PRIMARY PCI-X BUS

A0/B0 Routing of REQ/GNT		
	A0 silicon	B0 silicon
R83	Populate	Don't Populate
R85	Don't Populate	Populate
R84	Don't Populate	Populate
R82	Populate	Don't Populate

U3E3

Pin	Signal	Notes
1	SCL_A23	9/D4, 13/D3
2	AB21	9/D4, 13/D3
3	SCD1	13/C7
4	AB22	13/C7
5	SCD1	13/C7
6	AB24	13/C7
7	GPIO[0]U0_RXD	13/B7
8	GPIO[1]U0_TXD	13/B7
9	GPIO[2]U0_CTS	13/B7
10	GPIO[3]U0_RTS	13/B7
11	GPIO[4]U1_RXD	13/B7
12	GPIO[5]U1_TXD	13/B7
13	GPIO[6]U1_CTS	13/B7
14	GPIO[7]U1_RTS	13/B7
15	U0_RXD	13/B7
16	U0_TXD	13/B7
17	U0_CTS_N	13/B7
18	U0_RTS_N	13/B7
19	U1_RXD	13/B7
20	U1_TXD	13/B7
21	U1_CTS_N	13/A7
22	U1_RTS_N	13/B7
23	PBI_ALE	11/A8, 12/C8, 16/C6
24	PBI_OE_N	11/C6, 12/C8, 16/C6
25	PBI_WE_N	11/C6, 12/C8, 16/C6
26	PBI_CE0_N	11/C6, 12/C8, 16/C6
27	PBI_CE1_N	11/C8, 16/C6
28	PBI_A0	12/C8, 16/C6, 16/C6
29	PBI_A1	12/C8, 16/C6, 16/C6
30	PBI_A2	12/C8, 16/C6, 16/C6
31	PBI_A0	11/D7, 16/D5
32	PBI_A1	11/D7, 16/D5
33	PBI_A2	11/D7, 16/D5
34	PBI_A3	11/D7, 16/D5
35	PBI_A4	11/D7, 16/D5
36	PBI_A5	11/D7, 16/D5
37	PBI_A6	11/D7, 16/D5
38	PBI_A7	11/D7, 16/D5
39	PBI_A8	11/D7, 16/D5
40	PBI_A9	11/D7, 16/D5
41	PBI_A10	11/D7, 16/D5
42	PBI_A11	11/D7, 16/D5
43	PBI_A12	11/D7, 16/D5
44	PBI_A13	11/D7, 16/D5
45	PBI_A14	11/D7, 16/D5
46	PBI_A15	11/D7, 16/D5
47	PBI_A16	11/D7, 16/D5
48	PBI_A17	11/D7, 16/D5
49	PBI_A18	11/D7, 16/D5
50	PBI_A19	11/D7, 16/D5
51	PBI_A20	11/D7, 16/D5
52	PBI_A21	11/D7, 16/D5
53	PBI_A22	11/D7, 16/D5

PART 2 OF 9

PBI / GPIO

LD_2

DDR LD DQS[8:0] 8/D6

DDR LD DQS0

DDR LD DQS1

DDR LD DQS2

DDR LD DQS3

DDR LD DQS4

DDR LD DQS5

DDR LD DQS6

DDR LD DQS7

DDR LD DQS8

8/C4

8/B4

8/B4

9/B4

8/B4

8/B4

DDR LD CAS_N

DDR LD RAS_N

DDR LD WE_N

DDR M_RST_N

DDR LD CS0_N

DDR LD CS1_N

NC

DDR LD CKE0

DDR LD CKE1

DDR LD A0

DDR LD A1

DDR LD A2

DDR LD A3

DDR LD A4

DDR LD A5

DDR LD A6

DDR LD A7

DDR LD A8

DDR LD A9

DDR LD A10

DDR LD A11

DDR LD A12

DDR LD A13

DDR LD A[13:0] 8/D5

DDR LD_BA0

8/B4

DDR LD_BA1

8/B4

DDR LD_DM[8:0] 8/C6

DDR LD_DQ[63:0] 8/D8

DDR LD DQ0

DDR LD DQ1

DDR LD DQ2

DDR LD DQ3

DDR LD DQ4

DDR LD DQ5

DDR LD DQ6

DDR LD DQ7

DDR LD DQ8

DDR LD DQ9

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DDR LD DQ263

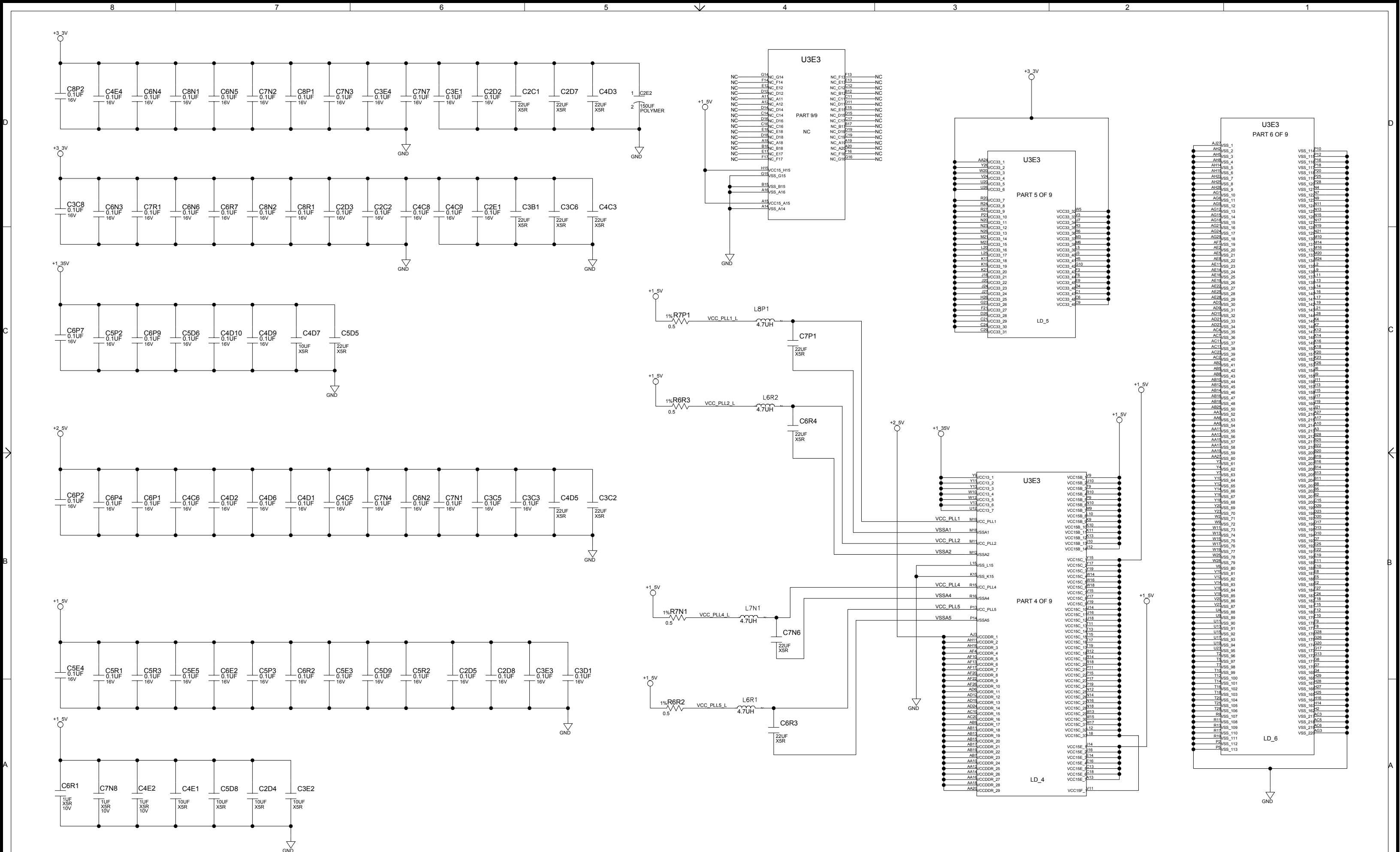
DDR LD DQ264

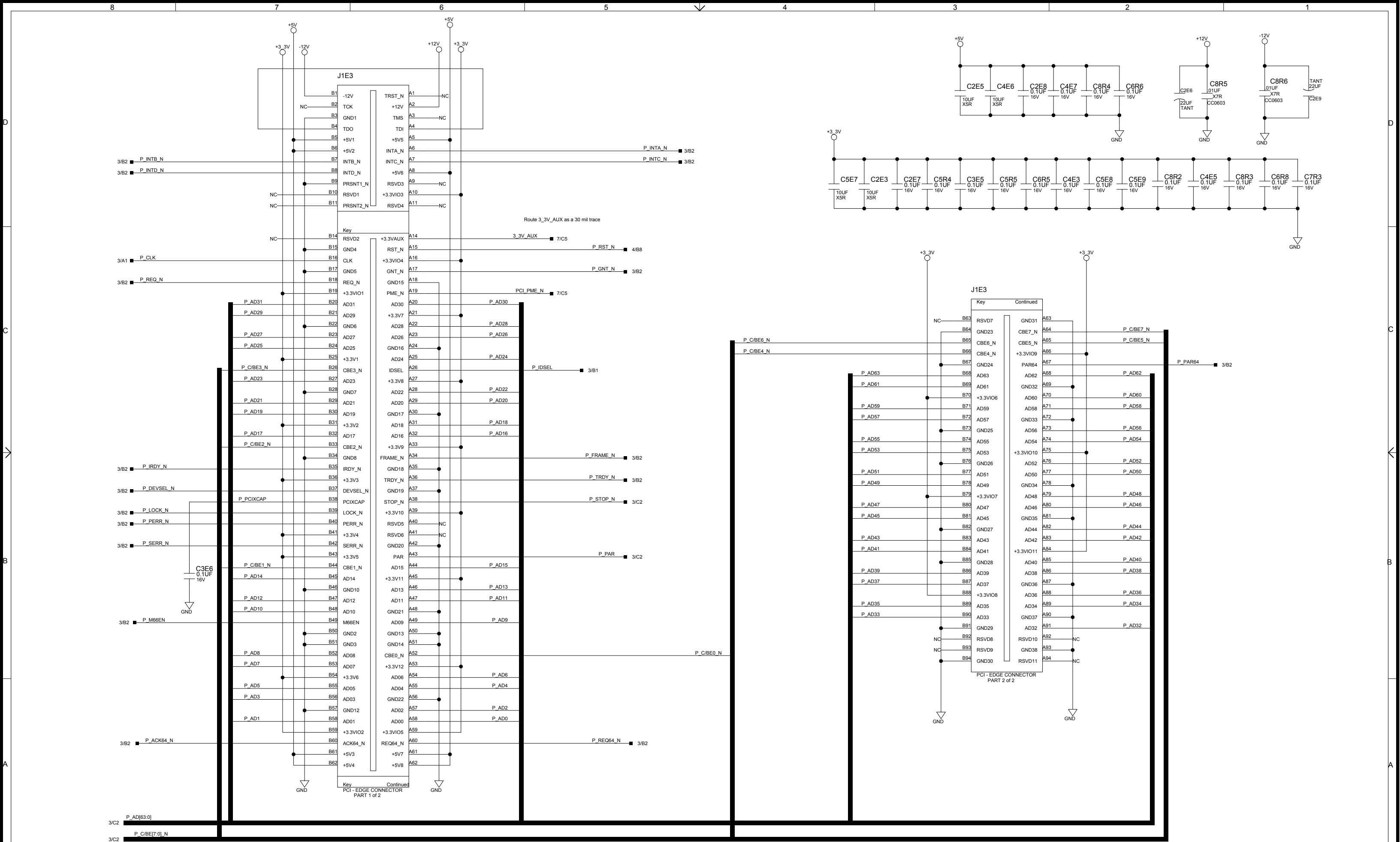
DDR LD DQ265

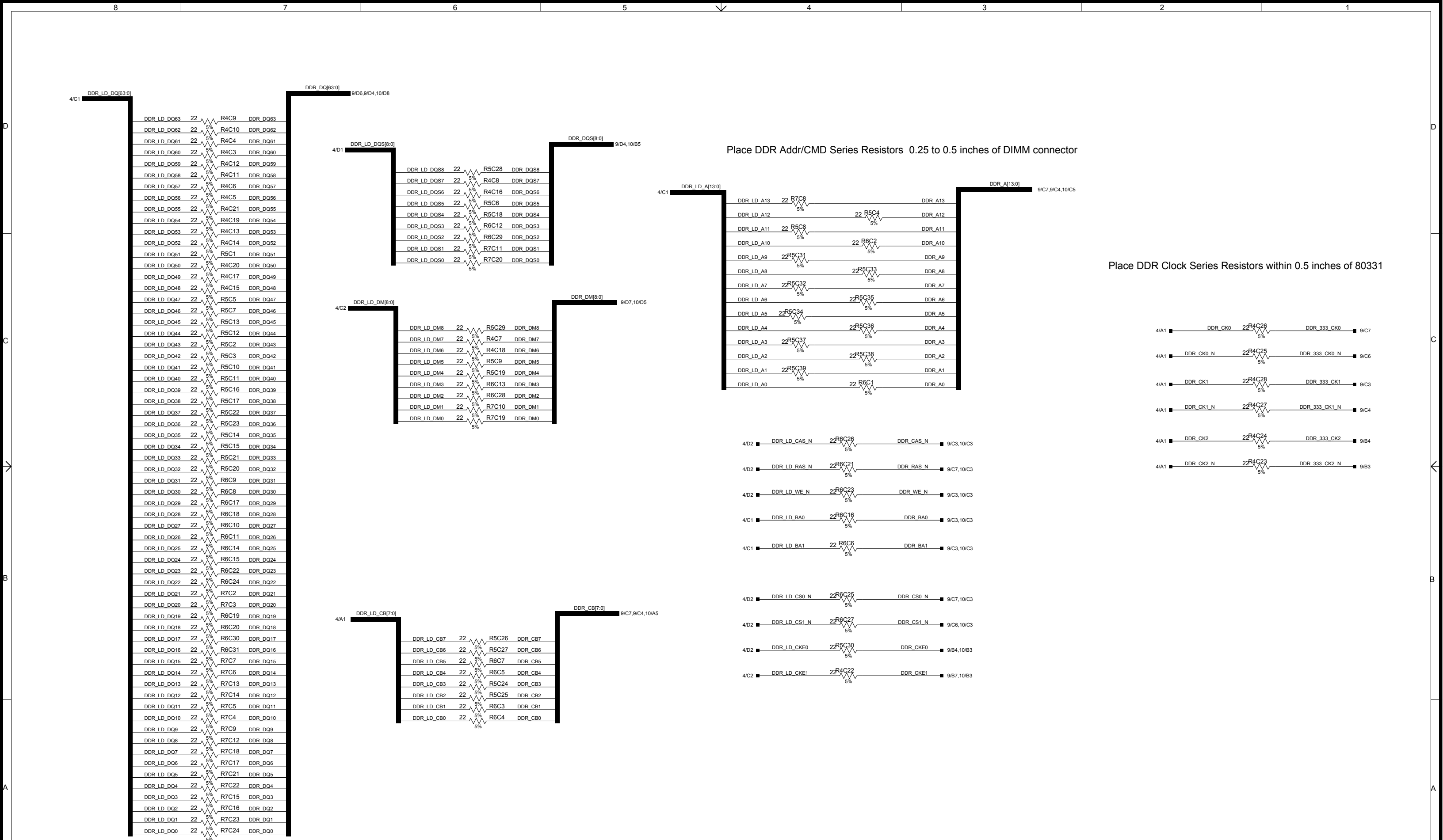
DDR LD DQ266

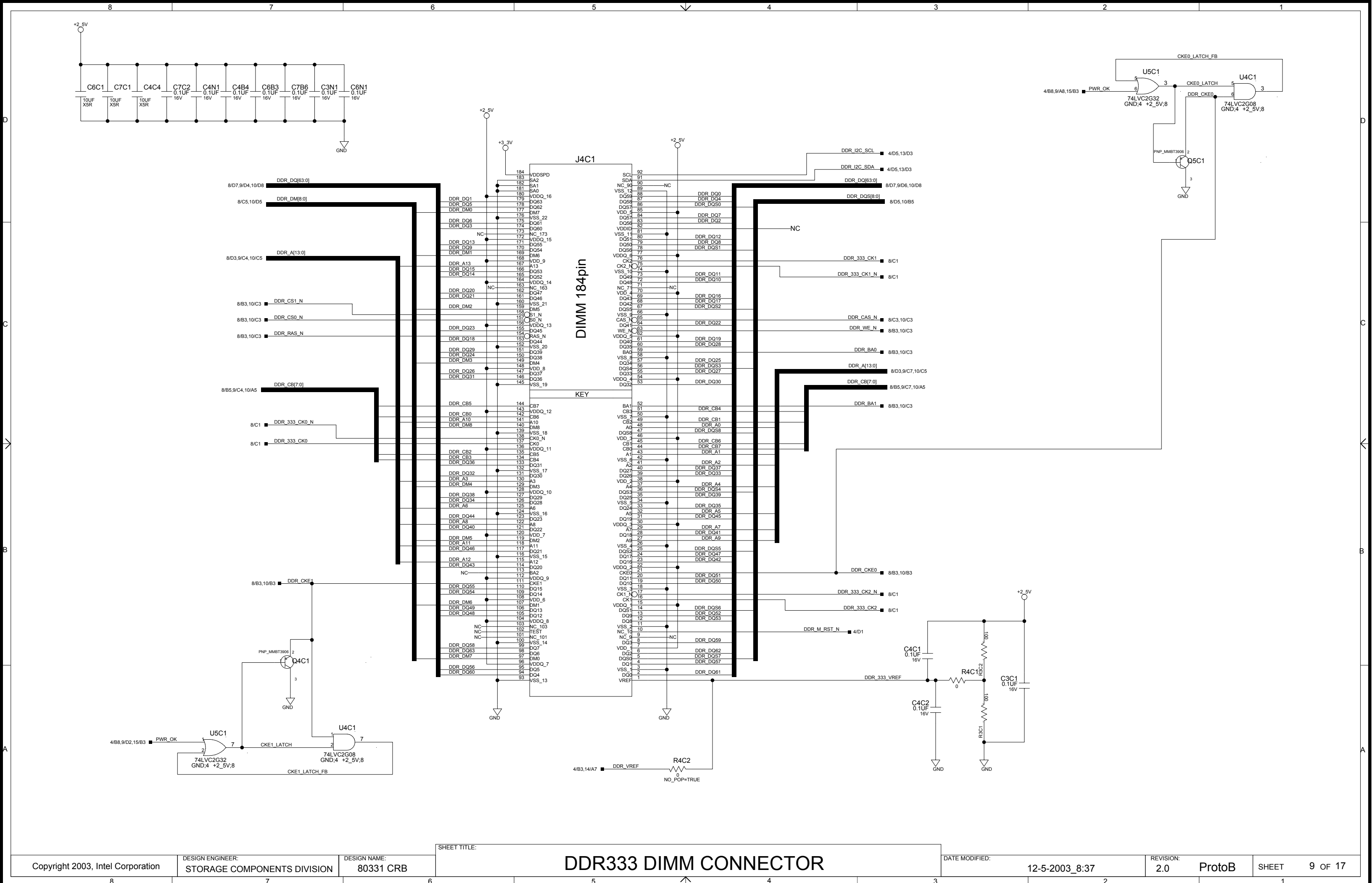
DDR LD DQ267

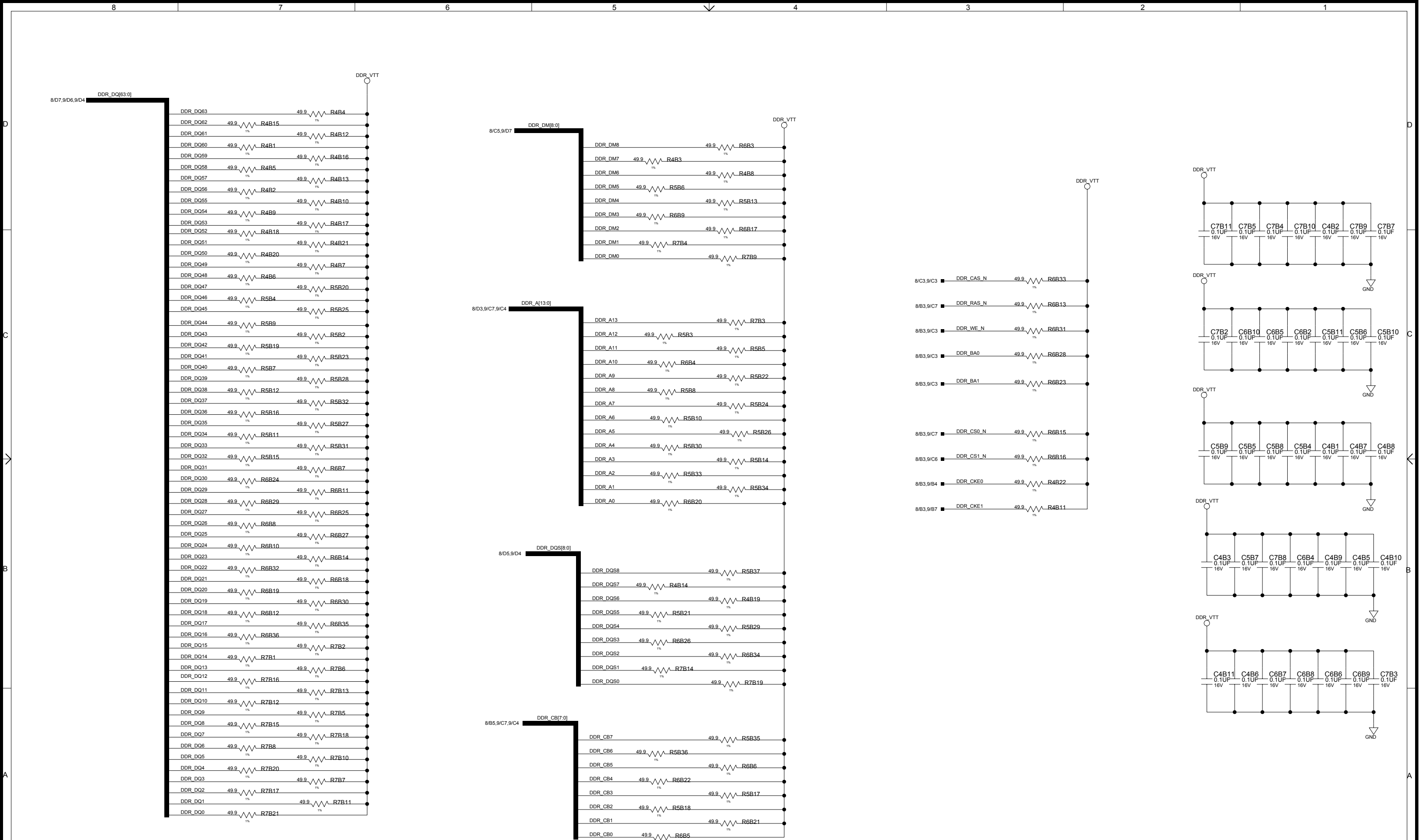
DDR LD

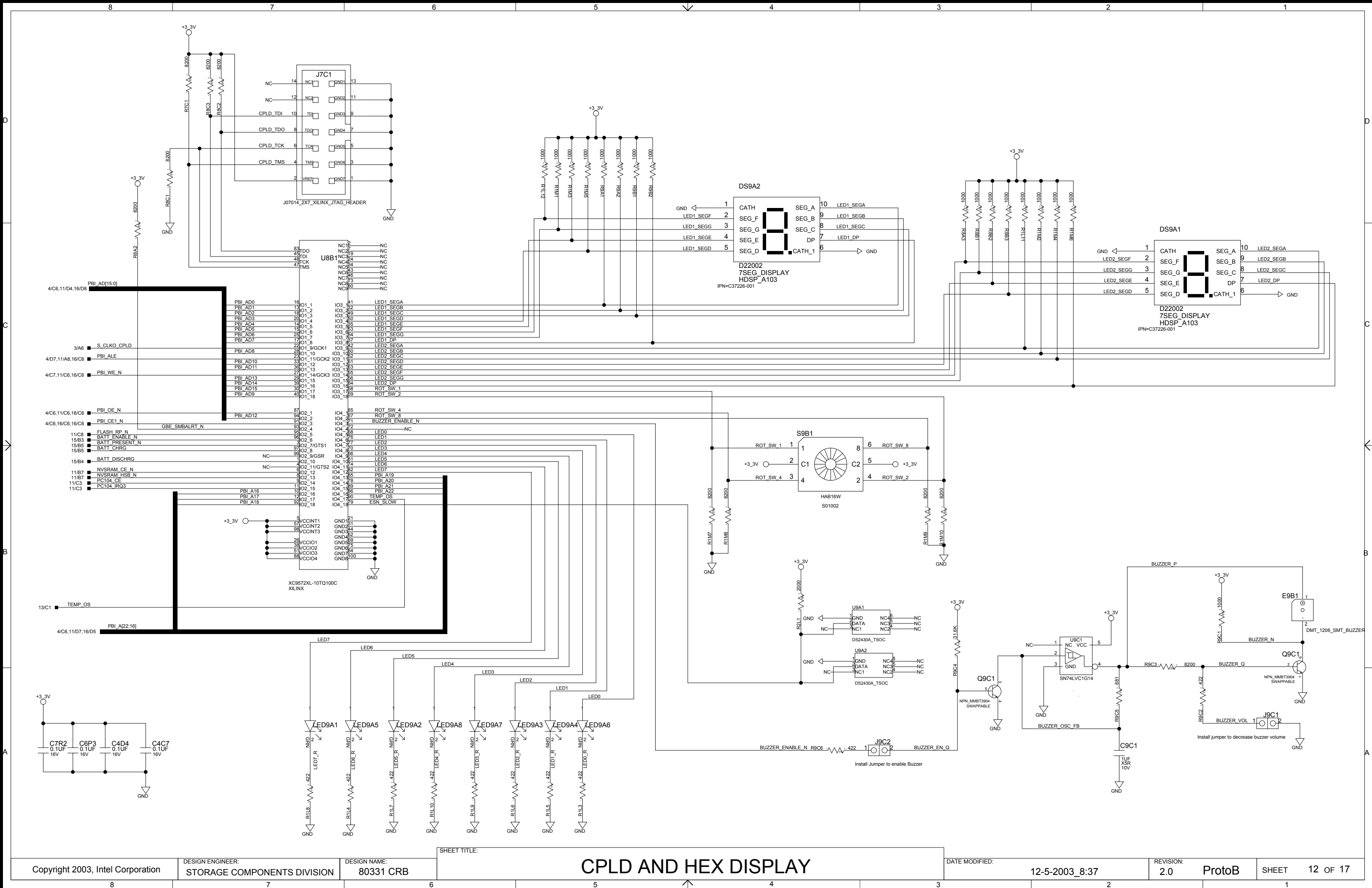


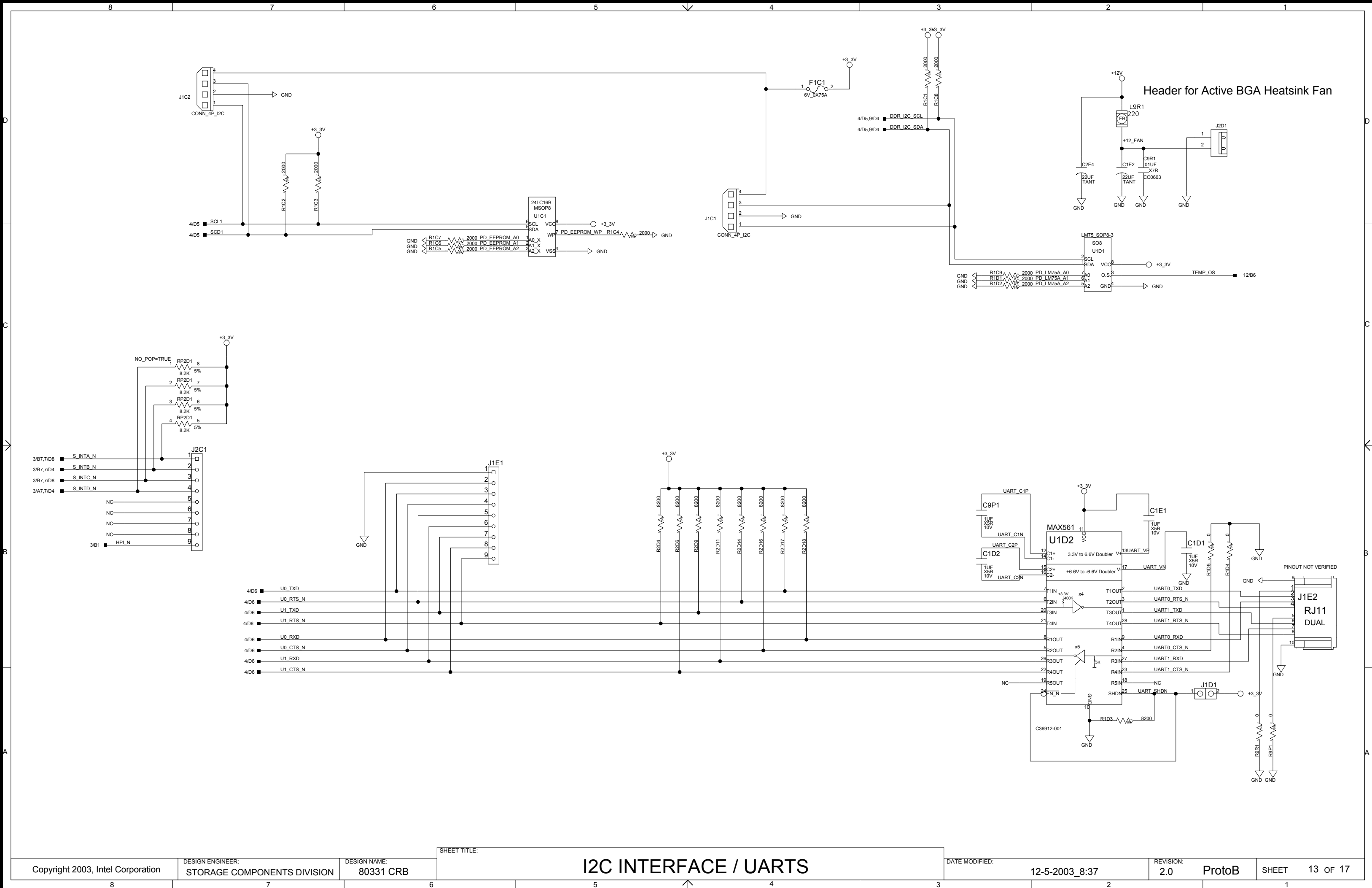




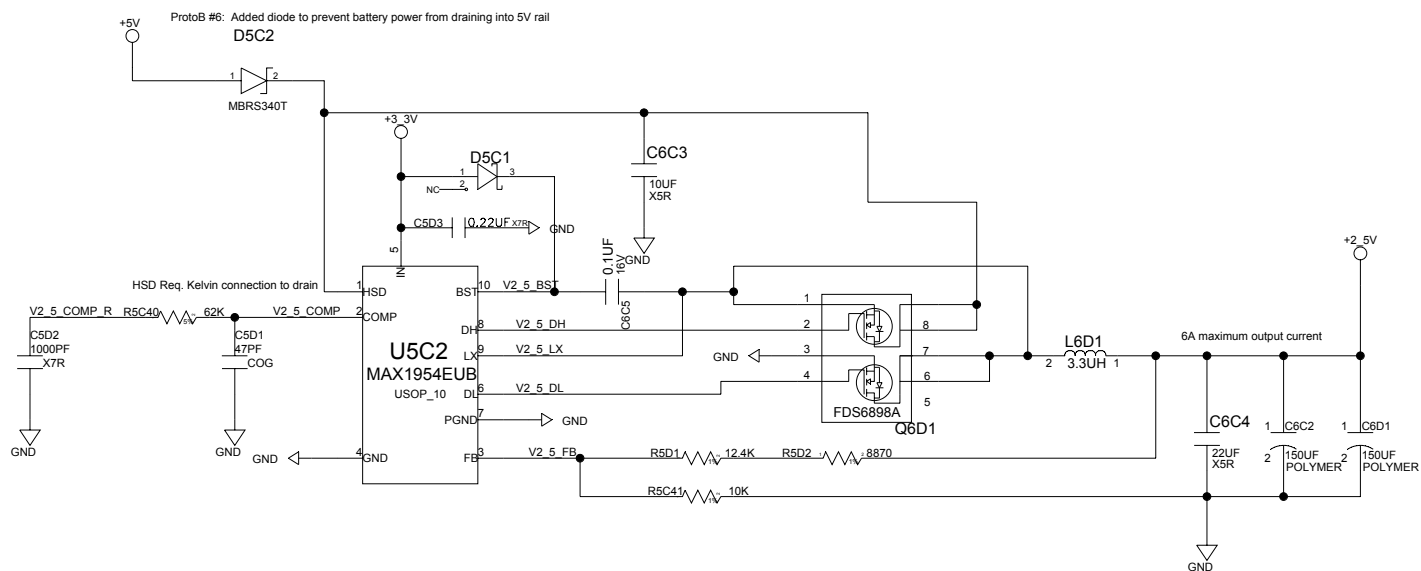




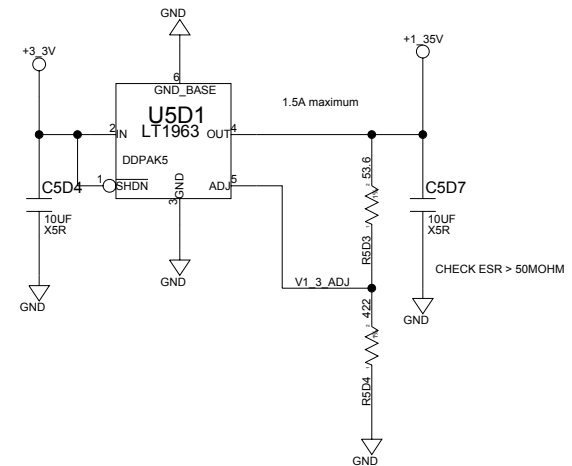




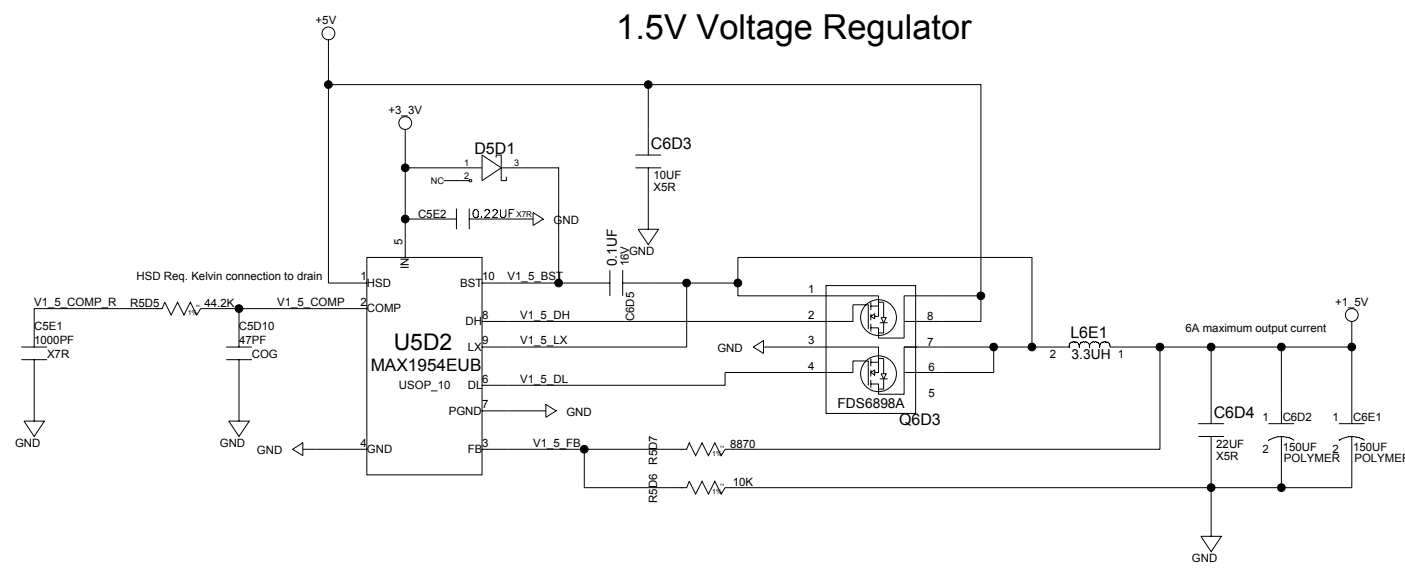
DDR Voltage Regulator



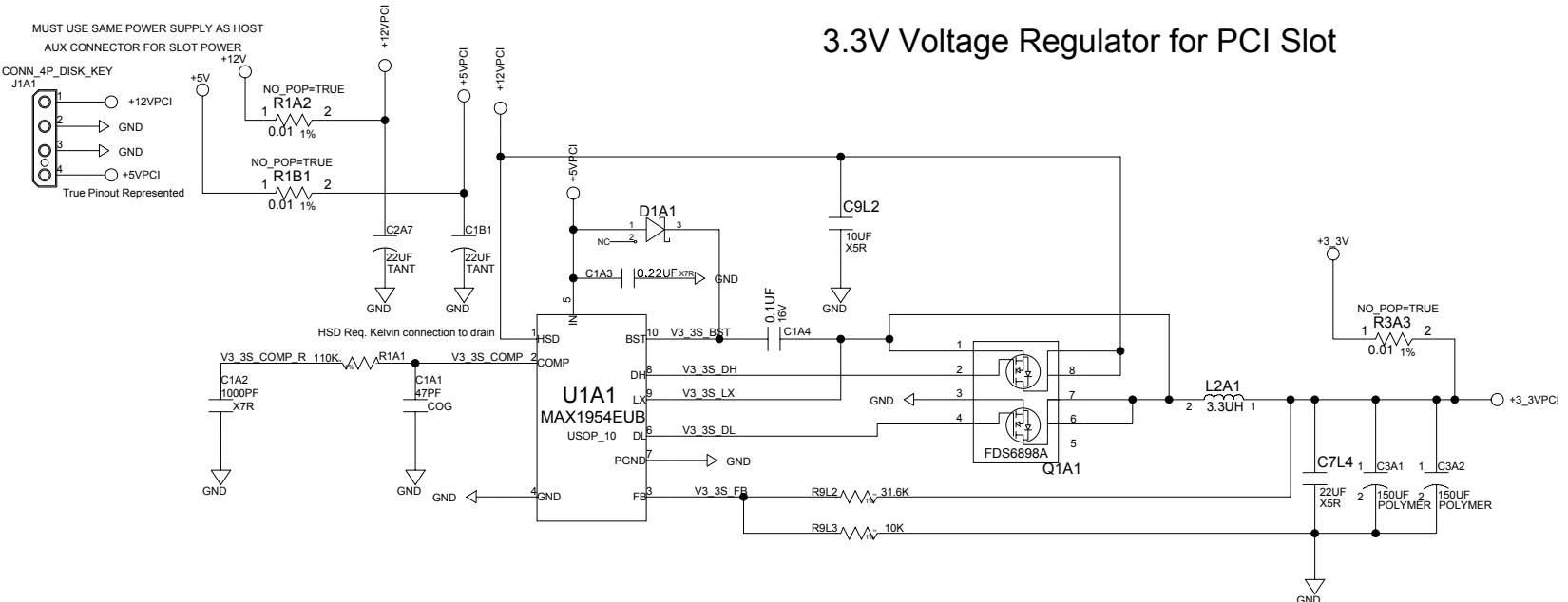
1.35V Voltage Regulator



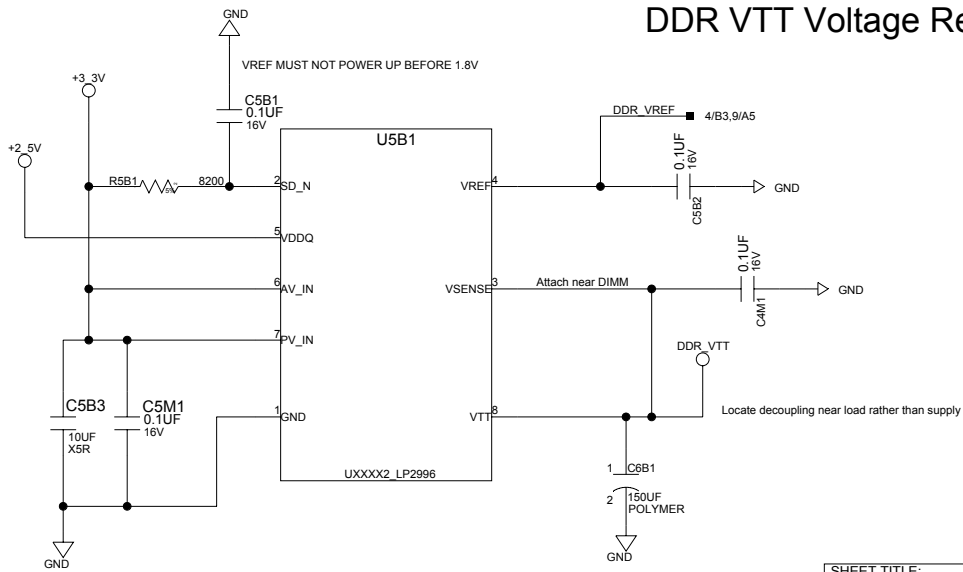
1.5V Voltage Regulator



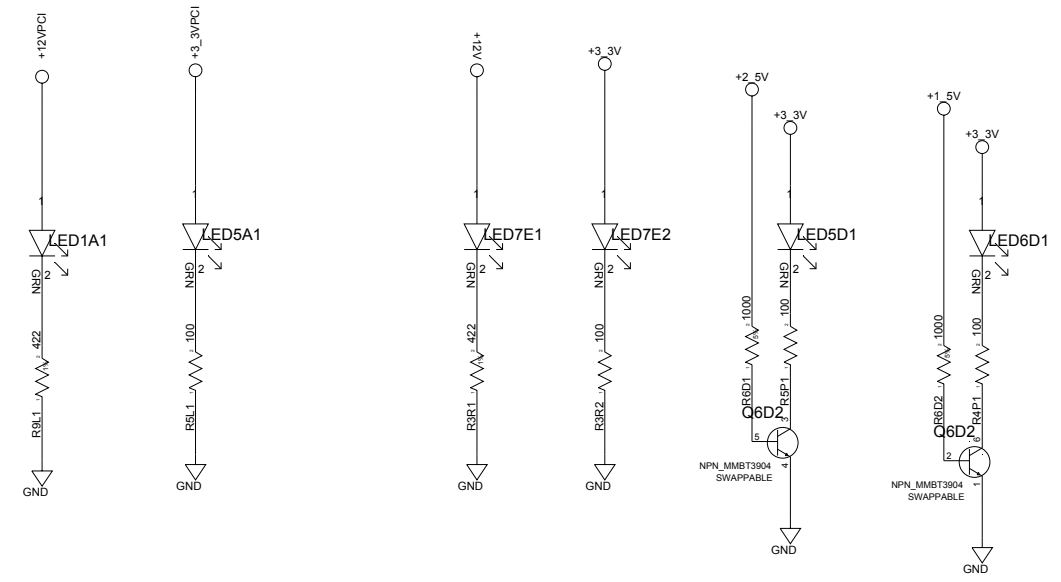
3.3V Voltage Regulator for PCI Slot

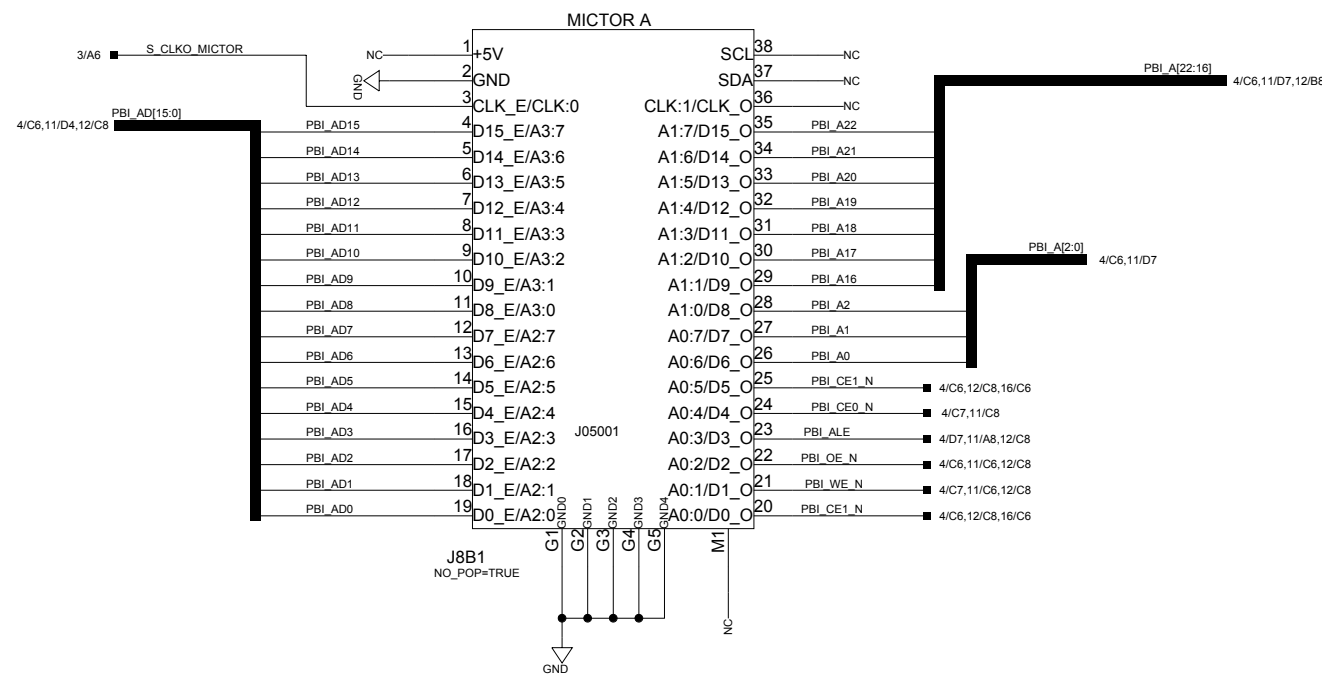


DDR VTT Voltage Regulator



LED Indicators





Mictor Connector Pin out
Agilent's vs. Tektronix

Tek	Agilent		Agilent	Tek
1 GND (1)	1 +5VDC (3)	• •	2 SCL (2)	38 GND (1)
2 GND (1)	3 GND (3)	• •	4 SDA (2)	37 GND (1)
3 CLK	5 CLKe	• •	6 CLKo	36 CLK
4 X3:7	7 D15e	• •	8 D15o	35 X1:7
5 X3:6	9 D14e	• •	10 D14o	34 X1:6
6 X3:5	11 D13e	• •	12 D13o	33 X1:5
7 X3:4	13 D12e	• •	14 D12o	32 X1:4
8 X3:3	15 D11e	• •	16 D11o	31 X1:3
9 X3:2	17 D10e	• •	18 D10o	30 X1:2
10 X3:1	19 D9e	• •	20 D9o	29 X1:1
11 X3:0	21 D8e	• •	22 D8o	28 X1:0
12 X2:7	23 D7e	• •	24 D7o	27 X0:7
13 X2:6	25 D6e	• •	26 D6o	26 X0:6
14 X2:5	27 D5e	• •	28 D5o	25 X0:5
15 X2:4	29 D4e	• •	30 D4o	24 X0:4
16 X2:3	31 D3e	• •	32 D3o	23 X0:3
17 X2:2	33 D2e	• •	34 D2o	22 X0:2
18 X2:1	35 D1e	• •	36 D1o	21 X0:1
19 X2:0	37 D0e	• •	38 D0o	20 X0:0

(1) Tektronix doesn't use pins 1,2,37,38 but recommends that they are grounded.
(2) Pins 2 & 4 are not to be used they are outputs from the logic analyzer used to program emulation or analysis probes.
(3) Pins 1 & 3 are not to be used they should be left as no connects. They are power pins for analysis/emulation probes.

8		7		6		5		4		3		2		1	
Revision History															
Rev 2.0 - ProtoB		12/5/2003													