Intel® Firmware Support Package (Intel® FSP) for Intel® Atom™ Processor C2000 Product Family for Communications Infrastructure POSTGOLD5

Release Notes

June 2016
## Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>June 15, 2016</td>
<td>002</td>
<td>Post-Gold 005 Release</td>
</tr>
<tr>
<td>September 24, 2015</td>
<td>001</td>
<td>Initial public release. Post-Gold 004 Release</td>
</tr>
<tr>
<td>April 9, 2015</td>
<td>1.3</td>
<td>Post-Gold 003 Release</td>
</tr>
<tr>
<td>April 2, 2014</td>
<td>1.2</td>
<td>Post-Gold 002 Release</td>
</tr>
<tr>
<td>December 18, 2013</td>
<td>1.1</td>
<td>Post-Gold 001 Release – first public release</td>
</tr>
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</table>
1.0 Introduction

This package contains the required binary image(s) and collateral for the Intel® Firmware Support Package (Intel® FSP) for Intel® Atom™ Processor C2000 Product Family for Communications Infrastructure POSTGOLD5.

This document provides system requirements, installation instructions, issues and limitations, and legal information.

To learn more about this product, see:

- New features listed in Section 2.0 “New in This Release”, or in the help.
- Reference documentation listed in Section 4.0 “Related Documentation, Tools, and Packages” below.
- Installation instructions listed in Section 5.1 “How to Install this Release” below.

1.1 Component Information

The software in this release has been developed and validated using the following in Table 1.

Table 1. Intel® FSP Component Information

<table>
<thead>
<tr>
<th>Component</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSP Binary Version</td>
<td>POSTGOLD4</td>
</tr>
<tr>
<td>Reference Code Version</td>
<td>49.R00</td>
</tr>
<tr>
<td>Memory Reference Code Version</td>
<td>1.0.0.49</td>
</tr>
<tr>
<td>Microcode Update C2xx0 A1</td>
<td>M01406D000E</td>
</tr>
<tr>
<td>Microcode Update C2xx0 B0</td>
<td>M01406D8129</td>
</tr>
</tbody>
</table>

1.2 Limitations

The following are the limitations for the Intel® FSP:

- The serial console base address of Intel® Atom™ Processor C2000 Product Family FSP is 0x2F8.
- The boot loader must ensure that FsplInitEntry Application Programming Interface (API) is called within one second of returning from TempRamlInitEntry API.
1.3 Acronyms and Terms

Table 2 shows the acronyms and terms used in this document (arranged in alphabetic order).

**Table 2. Acronyms and Terms**

<table>
<thead>
<tr>
<th>Acronym/Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>API</td>
<td>Application Programming Interface</td>
</tr>
<tr>
<td>BCT</td>
<td>Binary Configuration Tool</td>
</tr>
<tr>
<td>BSF</td>
<td>Binary Settings File</td>
</tr>
<tr>
<td>CRB</td>
<td>Customer Reference Board</td>
</tr>
<tr>
<td>FSP</td>
<td>Firmware Support Package</td>
</tr>
<tr>
<td>IBL</td>
<td>Intel® Business Link</td>
</tr>
<tr>
<td>RMT</td>
<td>Rank Margining Tool</td>
</tr>
<tr>
<td>SoC</td>
<td>System on a Chip</td>
</tr>
<tr>
<td>UPD</td>
<td>Updatable Product Data</td>
</tr>
<tr>
<td>VPD</td>
<td>Vital Product Data</td>
</tr>
</tbody>
</table>

1.4 Intended Audience

Platform and system developers who intend to use an Intel® Firmware Support Package-based boot loader for the firmware solution for their overall design based on the Intel® Atom™ Processor C2000 Product Family. This group includes, but is not limited to, system BIOS developers, boot loader developers, and system integrators.

1.5 Customer Support

Intel offers support for this software at the API level only, defined in the FSP Integration guide and reference manuals listed in Section 4.0 “Related Documentation, Tools, and Packages”. If your field representative has created an account for you, support requests can be submitted at https://premier.intel.com.

§ §
New in This Release

2.0 New in This Release

2.1 New Features

This release includes the following new features and product changes:

- Updated platform reference code to Reference Code Release (49.R00)
- Added VPD option to bypass disabling the TCO Watchdog Timer
- Added UPD option to enable/disable the DDR Relaxed Turnaround Timing
- Added UPD option to pass the location of the Microcode Region Base
- Added UPD option to pass the size of the Microcode Region
3.0 Known Issues

Known and resolved issues relating to Intel® Firmware Support Package are described in this section.

3.1 Known Issues for the Intel® Atom™ Processor C2000 Product Family

Table 3 lists known issues for the Intel® Atom™ Processor C2000 Product Family.

<table>
<thead>
<tr>
<th>Title</th>
<th>Problem</th>
<th>Workaround</th>
<th>Impact of Workaround</th>
</tr>
</thead>
<tbody>
<tr>
<td>Certain boards exhibit intermittent boot and MCE errors.</td>
<td>Boards with DDR trace lengths longer than the CRBs, see MCE Errors at 1333/1600 MT.</td>
<td>Set PcdEnableRelaxedTurnaroundTiming to Enabled in order to enable the relaxed DDR Turnaround timing.</td>
<td>Enabling this PCD will cause ~1% performance loss on the platform.</td>
</tr>
<tr>
<td>FSP disables the TCO Watchdog Timer after the boot loader re-enables the WDT.</td>
<td>There is a coverage gap for boot loaders that utilize the WDT to address system hangs.</td>
<td>Set the PcdTcoEnable to 1 in order for FSP to bypass disabling the WDT.</td>
<td>None.</td>
</tr>
<tr>
<td>Reboot occurring when PUNIT watchdog timer times out.</td>
<td>The PUNIT has a watchdog timer that provides a window of approximately 1 second to complete initial programming of power management related registers. Failure to feedback the status to the PUNIT within 1 second of a microcode update will result in the system requesting a reboot.</td>
<td>The boot loader must ensure that FspInitEntry API is called within one second of returning from TempRamInitEntry API. For designs that do not use an RTC battery, it is recommended that the RtcPowerFailureHandler() routine should be executed after the call to FspInitEntry API to ensure that the 1 second PUNIT timeout window is not violated.</td>
<td>None.</td>
</tr>
</tbody>
</table>

Table 3. Known Issues
3.2 Resolved Issues for the Intel® Atom™ Processor C2000 Product Family

Table 4 lists known resolved software-related issues for the Intel® Atom™ Processor C2000 Product Family.

Table 4. Resolved Software-Related Issues

<table>
<thead>
<tr>
<th>Title</th>
<th>Problem</th>
<th>Implication</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB 2.0 device may not be detected at system power-on.</td>
<td>Certain internal conditions may cause one or more USB ports to fail at system power-on.</td>
<td>When this erratum occurs, a USB device attached to the affected port will not function. In addition, the OS may report problems with the USB port.</td>
</tr>
</tbody>
</table>
## 4.0 Related Documentation, Tools, and Packages

Table 5 lists Intel® FSP for Intel® Atom™ Processor C2000 Product Family Platform documentation.

### Table 5. Intel® Firmware Support Package Documentation

<table>
<thead>
<tr>
<th>Document Name</th>
<th>Document No./Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Binary Configuration Tool (BCT) for Intel® FSP</td>
<td><a href="http://www.intel.com/fsp">www.intel.com/fsp</a></td>
</tr>
</tbody>
</table>
5.0 Where to Find the Release

This package can be found on www.intel.com/fsp.

5.1 How to Install this Release

This release can be installed on either a Windows* or a Linux* system.

For Windows:
2. Run the .exe file to perform the installation.

For Linux*:
2. Extract the contents of the .tgz file.
3. See the Readme_Extract.txt file for further instructions to complete the installation.

Note: For the guide to adding the Intel® FSP APIs into the boot loader code, refer to the Intel® Atom™ Processor C2000 Product FSP Integration Guide. (See Section 4.0, “Related Documentation, Tools, and Packages” on page 10.)

Note: For the guide to compiling the boot loader together with the Intel® FSP binary, refer to the Intel® Atom™ Processor C2000 Product Family Custom Reference Board Platform Guide. (See Section 4.0, “Related Documentation, Tools, and Packages” on page 10.)

5.2 Microcode Update

Since the introduction of the Pentium® Pro processor, IA-32 processors have had the capability to correct specific errata through the loading of an Intel-supplied data block. This data block is referred to as a microcode update or system configuration data.

Each unique processor stepping/package combination has an associated microcode update that, when applied, constitutes a supported processor (that is, Specified Processor = Processor Stepping + Microcode Update). The proper microcode update must be loaded on each processor in a system. The proper microcode update is defined as the latest microcode update available from Intel for a given family, model, and stepping of the processor. Any processor that does not have the correct microcode update loaded is considered to be operating out of specification.

The microcode update included in this release is the latest update at this particular time. Intel recommends that future microcode updates are done as soon as the latest ones are released.

Note: Intel recommends subscribing to the Intel® Atom™ Processor C2000 Product Family for Microserver and Communications Infrastructure Platforms (Edisonville/Rangeley) - Message of the Week (MoW) (see Section 4.0, “Related Documentation, Tools, and Packages” on page 10) for latest news on Processor Microcode Updates.

The steps for updating the microcode for a sample boot loader can be found under “Microcode Update” in the Intel® Atom™ Processor C2000 Product Family Custom Reference Board Platform Guide. (See Section 4.0, “Related Documentation, Tools, and Packages” on page 10.)
5.3 Debug

Debug messages are the primary way of debugging the Intel® FSP. This requires enabling the debug messages into the serial port. The steps to enable the serial debug messages can be found in How to Enable Serial Debug Messages in the Intel® Atom™ Processor C2000 Product Family Custom Reference Board Platform Guide. (See Section 4.0, “Related Documentation, Tools, and Packages” on page 10.)

5.4 Validation

The Rank Margining Tool (RMT) can flag areas of concern for platform developers. The steps to enable RMT is described in detail under “How to Enable the Rank Margining Tool” in the Intel® Atom™ Processor C2000 Product Family Custom Reference Board Platform Guide. (See Section 4.0, “Related Documentation, Tools, and Packages” on page 10.)
6.0 Release Content

This release package contains the following:

Table 6. Package Contents

<table>
<thead>
<tr>
<th>Description</th>
<th>Filename</th>
<th>Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSP Kit License File</td>
<td>FSP Kit Production RULAC click-through License.pdf</td>
<td>RANGELEY_FSP_KIT</td>
</tr>
<tr>
<td>FSP Binary File</td>
<td>RANGELEY_POSTGOLD5_FSP_005_20160406.fd</td>
<td>RANGELEY_FSP_KIT/FSP</td>
</tr>
<tr>
<td>Boot Setting File (BSF)</td>
<td>RangeleyFsp.bsf</td>
<td>RANGELEY_FSP_KIT/FSP</td>
</tr>
<tr>
<td>Text file copy of FSP kit license file (Linux* only)</td>
<td>license.txt</td>
<td>RANGELEY_FSP_KIT/DOCUMENTATION</td>
</tr>
<tr>
<td>Intel® Atom™ Processor C2000 SoC Microcode</td>
<td>microcode-m01406d000e.h</td>
<td>RANGELEY_FSP_KIT/Microcode</td>
</tr>
<tr>
<td>*h</td>
<td>FSP header files</td>
<td>RANGELEY_FSP_KIT/FSP/include</td>
</tr>
<tr>
<td>*c</td>
<td>FSP source files</td>
<td>RANGELEY_FSP_KIT/FSP/srx</td>
</tr>
</tbody>
</table>

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7.0 Hardware and Software Compatibility

7.1 Supported Hardware

The FSP included in this release is specifically targeted for the Intel® Atom™ Processor C2000 Product Family System on a Chip (SoC).

7.2 Supported Operating Systems

This release installs on either a Windows* or a Linux* system. However, the FSP binary itself can be used with any software development environment to generate a complete boot loader solution.

The software in this release has been validated against the operating systems given in the following table on the Customer Reference Boards (CRBs) for the following products:

- Intel® Atom™ Processor C2000 Product Family

Note: While the Intel® Firmware Support Package is validated on Coreboot* and Yocto* on the respective platforms, it is designed to work without change on some other boot loaders and operating systems.

<table>
<thead>
<tr>
<th>Software Type</th>
<th>Name</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boot loader</td>
<td>Coreboot</td>
<td>4.3</td>
</tr>
<tr>
<td>Payload Boot loader</td>
<td>u-boot Payload</td>
<td>u-boot-2013.01.01</td>
</tr>
<tr>
<td>Firmware Component</td>
<td>FSP</td>
<td>Gold 005</td>
</tr>
<tr>
<td>Operating System</td>
<td>Yocto</td>
<td>Poky 9.0 (Yocto Project 1.4 Reference Distro) 1.4.1</td>
</tr>
<tr>
<td>Tool</td>
<td>Binary Configuration Tool</td>
<td>3.2.0</td>
</tr>
</tbody>
</table>
8.0 Configuration

A Binary Configuration Tool (BCT) for the Intel® FSP is provided as a companion tool and is intended to be used to do the following:

- Customize the FSP binary configuration options based on the Boot Setting File (BSF).
- Rebase the FSP binary to a different base address. (The default base address of the Intel® FSP for Intel® Atom™ Processor C2000 Product Family is 0xFFF80000.)

Intel recommends to use latest BCT with this release.

Refer to the BCT User Guide for the usage instructions. See Section 4.0 “Related Documentation, Tools, and Packages” to obtain the BCT.

8.1 Intel® Firmware Support Package Information

To obtain the Intel® FSP binary information:

1. Run the Binary Configuration Tool as an Administrator.
2. Click the Show Binary Description command button.
3. Select the Intel® FSP binary. For this release, the binary included is named as RANGELEY_POSTGOLD5_FSP_005_20160406.fd.
4. Click Open. Another window, shown in Figure 1, will pop out to show the Intel® FSP binary information.
5. Click OK to close the window.
Figure 1. Intel® FSP Binary Information

![FSP Header Rev. 1.0](image1)

This FSP supports the following:
- Avoton/Rangeley A1 and Bx SOC

FSP Header:
- Signature: FSPH
- Header Length: 0x40
- Header Revision: 0x1
- Image Revision: 0x150
- Image ID: AVN-FSP0
- Image Size: 0x5f000
- Image Base: 0xffff80000
- Image Attribute: 0x0
- Configuration Region Offset: 0x59a2c
- Configuration Region Size: 0xe

Header Length: 0x40
Header Revision: 0x1
Image Revision: 0x150
Image ID: AVN-FSP0
Image Size: 0x5f000
Image Base: 0xffff80000
Image Attribute: 0x0
Configuration Region Offset: 0x59a2c
Configuration Region Size: 0xe

API Entry Num: 0x3
Temp RAM Init Entry: 0x5e40b
FSP Init Entry: 0x5e589
Notify Phase Entry: 0x5e615

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9.0 Legal Information

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