



Puma 5 Family of DOCSIS* 3.0 Cable Chipsets



The Puma 5 family of cable modem, Embedded Multimedia Terminal Adapter (EMTA), set-top box (STB), and gateway chipsets provides a flexible and scalable platform on which equipment manufacturers can build systems for compelling next-generation video, voice, and data service offerings. Puma 5 delivers the much anticipated higher data rates supported by both the U.S. and European versions of DOCSIS* 3.0 (Data Over Cable Service Interface Specification).

With DOCSIS 3.0 line speeds starting at 160 Mbps, the Puma 5 family has the flexibility and agility to support a wide range of current and next-generation applications. Starting with basic data-centric cable modem applications like high-speed Internet access, Puma 5 chipsets have the resources for higher end applications such as voice-oriented embedded multimedia terminal adapter (EMTA) services and market-leading digital Internet Protocol-based television (IPTV). The platform's simple reconfigurability allows operators to deploy the DOCSIS 3.0

capabilities of the Puma 5 family today and be assured that they will be able to cost-effectively upgrade their service offerings to meet the market for compelling multimedia services like IPTV.

Flexible Architecture Optimized for Triple Play

As the first DOCSIS 3.0-compliant solution, the Puma 5 family of chipsets provides a proven and accelerated path to the marketplace for equipment manufacturers. The variety of configurations supported by the chipsets that make up the Puma 5 family gives manufacturers the ability to quickly implement cost-effective, scalable products with targeted capabilities for a wide range of applications. From entry-level high-speed Internet access services to high-end triple-play video, voice, and data service offerings, the Puma 5 family has a ready-to-implement chipset with a configuration adapted to the requirements of the narrow segments that make up the cable marketplace.

Key Features

- Flexible and scalable platform for compelling video, data, and voice applications
- Full U.S. and European DOCSIS* 3.0 data rates starting at a minimum of 160 Mbps
- Multimedia processing architecture
- DOCSIS 3.0 subsystem complete with channel bonding on both upstream and downstream
- Multichannel DOCSIS physical interface configurations:
 - Dedicated VoIP DSP-based subsystem
 - Packet accelerator reduces latencies, increases QoS
 - General-purpose processor
 - Four upstream and four downstream channels (4 x 4)
 - Expandable to four upstream and eight downstream channels (8 x 4)
- High-quality VoIP
 - Versatile home networking
 - Battery-backup control logic

For example, you can implement cost-sensitive residential services with a Puma 5 chipset supporting the minimum-yet still very high speed-DOCSIS 3.0 downstream data rates that start at 160 Mbps. Then, by capitalizing on the channel-bonding capabilities of DOCSIS 3.0 and the Puma 5 family's flexibility, you can quickly scale upward to higher speed offerings of 320 Mbps or more for business-oriented services. Plus, this sort of rapid redeployment of bandwidth requires no new capital investment in cable operators' infrastructures.

Multimedia Processing Architecture

Central to the Puma 5 chipsets is a multimedia processing architecture that includes a DOCSIS 3.0 subsystem. This subsystem is extremely flexible and supports a wide

range of channel configurations, depending on the requirements of the targeted service offering. Puma 5 chipsets have the necessary resources for supporting voice over Internet Protocol (VoIP) with excellent voice quality, even when the platform is performing extensive data or video processing.

Multichannel DOCSIS 3.0 Scalability

The DOCSIS 3.0 subsystem maximizes flexibility by supporting a range of channels and channel types, as well as expansion capabilities to accommodate future growth.

The Puma 5 family includes a DOCSIS 3.0 physical layer (PHY) interface that is adaptable to a range of U.S. and European configurations and can scale upward to a 4 x 4 configuration. Channel expansion is supported up to eight downstream channels (8 x 4).

Next-Generation Applications

The Puma 5 chipsets feature a number of capabilities for easy and cost-effective migration to next-generation applications like IPTV and others. These resources will support a rapid rollout of IPTV service as marketplace demand grows. And no capital investment is necessary in the cable operator's infrastructure.

Set-top gateway applications involving home networking and multiple STBs throughout the residence are possible with the extensive high-speed networking interfaces of the Puma 5.

The Puma 5 Family

The chipsets making up the Puma 5 family have been optimized to meet the cost and performance requirements of the most prevalent market segments in the cable industry.

- TNETC4800 supports full-functionality EMTA applications, including a battery-backup subsystem.
- TNETC4810 is optimized for EMTA applications without a battery-backup subsystem.
- TNETC4830 is an optimized data cable modem platform.

For more information on Intel® Puma 5 Family, visit www.intel.com/go/cablemodem

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. UNLESS OTHERWISE AGREED IN WRITING BY INTEL, THE INTEL PRODUCTS ARE NOT DESIGNED NOR INTENDED FOR ANY APPLICATION IN WHICH THE FAILURE OF THE INTEL PRODUCT COULD CREATE A SITUATION WHERE PERSONAL INJURY OR DEATH MAY OCCUR.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request. Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order. Copies of documents which have an order number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725, or by visiting Intel's Web site at www.intel.com.

Copyright © 2010 Intel Corporation. All rights reserved. Intel and the Intel logo are trademarks of Intel Corporation in the U.S. and other countries.

*Other names and brands may be claimed as the property of others.

Printed in USA

1110/GRB/HBD/PDF

♻️ Please Recycle

324684-001US

