Performance Optimization of Deep Learning Frameworks on Modern Intel Architectures

ElMoustapha Ould-Ahmed-Vall, AG Ramesh, Vamsi Sripathi and Karthik Raman

Representing the work of many at Intel
Agenda

• Optimization matters on modern architectures

• Intel’s recent Xeon and Xeon Phi products

• Introduction to Deep Learning

• Optimizing DL frameworks on IA
  • Key challenges
  • Optimization techniques
  • Performance data
  • DL scaling
Moore’s Law Goes on!

Increasing clock speeds -> more cores + wider SIMD (Hierarchical parallelism)
Combined Amdahl’s Law for Vector Multicores*

\[
\text{Speedup} = \left( \frac{1}{\text{Serial}\downarrow \text{frac}} + 1 - \frac{\text{Serial}\downarrow \text{frac}}{\text{NumCores}} \right) \times \left( \frac{1}{\text{Scalar}\downarrow \text{frac}} + 1 - \frac{\text{Scalar}\downarrow \text{frac}}{\text{VectorLength}} \right)
\]

Goal: Reduce Serial Fraction and Reduce Scalar Fraction of Code

Ideal Speedup: NumCores*VectorLength (requires zero scalar, zero serial work)

**Compute Bound Performance**
Most kernels of ML codes are compute bound
i.e. raw FLOPS matter

**Roofline Model**
Gflops/s = min (Peak Gflops/s, Stream BW * flops/byte)
Overview of Current Generation of Intel Xeon and Xeon Phi Products
Current Intel® Xeon Platforms

- 45nm Process Technology
  - Nehalem
  - NEW Intel® Microarchitecture (Nehalem)
  - Tock
- 32nm Process Technology
  - Westmere
  - Intel Microarchitecture (Nehalem)
  - Tick
  - Sandy Bridge
  - NEW Intel Microarchitecture (Sandy Bridge)
  - Tock
- 22nm Process Technology
  - Ivy Bridge
  - Intel Microarchitecture (Sandy Bridge)
  - Tick
  - Haswell
  - NEW Intel Microarchitecture (Haswell)
  - Tock
- 14nm Process Technology
  - Broadwell
  - Intel Microarchitecture (Haswell)
  - Tick

Latest released – Broadwell (14nm process)

- Intel’s foundation of HPC and ML performance
- Suited for full scope of workloads
- Industry leading performance/watt for serial & highly parallel workloads.
- Upto 22 cores / socket (Broadwell-EP) (w/ Hyper-Threading technology)

Software optimization helps maximize benefit and adoption of new features
2nd Generation Intel® Xeon Phi™ Platform

Knights Landing
Holistic Approach to Real Application Breakthroughs

- **Platform Memory**
  - Up to 384 GB DDR4 (6 ch)

- **Compute**
  - Intel® Xeon® Processor Binary-Compatible
  - 3+ TFLOPS¹, 3X ST² (single-thread) perf. vs KNC
  - 2D Mesh Architecture
  - Out-of-Order Cores

- **On-Package Memory**
  - Over 5x STREAM vs. DDR4³
  - Up to 16 GB at launch

- **Omni-Path**
  - 1st Intel processor to integrate

- **Integrated Intel® Omni-Path**

- **Processor Package**

- **I/O**
  - Up to 36 PCIe 3.0 lanes
## Intel® AVX Technology

### SNB/IVB
- 256b AVX1
  - Flops/Cycle: 16 SP / 8 DP

### HSW/BDW
- 256b AVX2
  - Flops/Cycle: 32SP / 16 DP (FMA)

### SKX & KNL
- 512b AVX512
  - Flops/Cycle: 64SP / 32 DP (FMA)

### AVX vs AVX2
<table>
<thead>
<tr>
<th>AVX</th>
<th>AVX2</th>
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</thead>
<tbody>
<tr>
<td>256-bit basic FP</td>
<td>Float16 (IVB 2012)</td>
</tr>
<tr>
<td>16 registers</td>
<td>256-bit FP FMA</td>
</tr>
<tr>
<td>NDS (and AVX128)</td>
<td>256-bit integer</td>
</tr>
<tr>
<td>Improved blend</td>
<td>PERMD</td>
</tr>
<tr>
<td>MASKMOV</td>
<td>Gather</td>
</tr>
<tr>
<td>Implicit unaligned</td>
<td></td>
</tr>
</tbody>
</table>

### AVX512
- 512-bit FP/Integer
- 32 registers
- 8 mask registers
- Embedded rounding
- Embedded broadcast
- Scalar/SSE/AVX “promotions”
- Native media additions
- HPC additions
- Transcendental support
- Gather/Scatter
Overview of Deep Learning and DL Frameworks
Deep Learning – Convolutional Neural Network

Convolution Parameters:
Number of outputs/feature-maps: < 4 >
Filter size: < 3 x 3 >
Stride: < 2 >
Pad_size (for corner case): <1>

Filter = 3 x 3
Stride = 2
Pad_size = 1

Convolutional parameters include:
- Number of outputs/feature-maps: less than 4
- Filter size: 3 x 3
- Stride: 2
- Pad_size (for corner case): 1

Image

Feature maps

Convolved Feature

Diagram showing the input layer, convolutional layers, max-pooling layers, and the output layer. The feature maps and convolved feature are illustrated with grid representations.
Deep Learning: Train Once Use Many Times

Step 1: Training
(Over Hours/Days/Weeks)

- Input data
- Create Deep network
- Output Classification

- 90% person
- 8% traffic light

Step 2: Inference
(Real Time)

- New input from camera and sensors
- Trained neural network model
- Output Classification

- 97% person
Deep Learning: Why Now?

**Bigger Data**
- Image: 1000 KB / picture
- Audio: 5000 KB / song
- Video: 5,000,000 KB / movie

**Better Hardware**
- Transistor density doubles every 18 months
- Cost / GB in 1995: $1000.00
- Cost / GB in 2015: $0.03

**Smarter Algorithms**
- Advances in algorithm innovation, including neural networks, leading to better accuracy in training models
Intel Caffe – ML Framework
Optimized for Xeon and Xeon Phi Products

- Fork of BVLC Caffe by Intel to optimize for IA
- Leverages Intel MKL Deep Neural Network (DNN) API’s
- Optimized for BDW (AVX2) and KNL (MIC_AVX512)
- [https://github.com/intel/caffe](https://github.com/intel/caffe)
Tensorflow™: Open Source ML Framework (Google)

- **Computation is a Dataflow Graph with Tensors**
- General computing mathematical framework – widely used for
  - Deep Neural Networks
  - Other machine learning algorithms
  - HPC applications
- Key computational kernels, extendable user operations
- Core in C++, front end wrapper in python
- Multi node support using GRPC
  - Google Remote Procedural Calls

Example from Jeff Dean’s presentation
Optimizing Deep Learning Frameworks
## Performance Optimization on Modern Platforms

### Hierarchical Parallelism

<table>
<thead>
<tr>
<th>Coarse-Grained / multi-node</th>
</tr>
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<tbody>
<tr>
<td>Domain decomposition</td>
</tr>
</tbody>
</table>

### Fine-Grained Parallelism / within node

- **Sub-domain:** 1) Multi-level domain decomposition (ex. across layers)
- 2) Data decomposition (layer parallelism)

### Scaling

- Improve load balancing
- Reduce synchronization events, all-to-all comms

### Utilize all the cores

- OpenMP, MPI, TBB...
- Reduce synchronization events, serial code
- Improve load balancing

### Vectorize/SIMD

- Unit strided access per SIMD lane
- High vector efficiency
- Data alignment

### Efficient memory/cache use

- Blocking
- Data reuse
- Prefetching
- Memory allocation

---

**Performance Optimization**

- **Utilize**
  - OpenMP, MPI, TBB...
  - Reduce synchronization events, serial code
  - Improve load balancing
- **Vectorize/SIMD**
  - Unit strided access per SIMD lane
  - High vector efficiency
  - Data alignment
- **Efficient memory/cache use**
  - Blocking
  - Data reuse
  - Prefetching
  - Memory allocation
# Intel Strategy: Optimized Deep Learning Environment

<table>
<thead>
<tr>
<th>Fuel the development of vertical solutions</th>
<th>Intel® Deep Learning SDK</th>
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</thead>
<tbody>
<tr>
<td>Accelerate design, training, and deployment</td>
<td>Caffe, theano, TensorFlow, torch, mxnet</td>
</tr>
<tr>
<td>Drive optimizations across open source deep learning frameworks</td>
<td>Intel® Math Kernel Library (Intel® MKL), Intel® MKL-DNN</td>
</tr>
<tr>
<td>Maximum performance on Intel architecture</td>
<td>Intel® Omni-Path Architecture (Intel® OPA) + Intel® XEON inside</td>
</tr>
<tr>
<td>Deliver best single node and multi-node performance</td>
<td>Intel® XEON inside + Altera 10</td>
</tr>
</tbody>
</table>

**Training** | **Inference**
Example Challenge 1: Data Layout Has Big Impact on Performance

- Data Layouts impacts performance
  - Sequential access to avoid gather/scatter
  - Have iterations in inner most loop to ensure high vector utilization
  - Maximize data reuse; e.g. weights in a convolution layer
- Converting to/from optimized Layout is some times less expensive than operating on unoptimized Layout

Better optimized for some operations

VS
Example Challenge 2: Minimize Conversions Overhead

- End to end optimization can reduce conversions
- Staying in optimized layout as long as possible becomes one of the tuning goals
- Minimize the number of back and forth conversions
  - Use of graph optimization techniques

```
Native to MKL layout ⮚ Convolution ⮚ MKL layout to Native ⮚ Max Pool ⮚ Native to MKL layout ⮚ Convolution ⮚ MKL layout to Native
```
Example Challenge 3: Ensuring Enough Parallelism to Leverage all Cores

- Maximize parallelism to use all cores efficiently

- Intra operation/layer parallelism within operators (OpenMP)

<table>
<thead>
<tr>
<th>8</th>
<th>92</th>
<th>37</th>
<th>29</th>
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<td>11</td>
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<tr>
<td>15</td>
<td>16</td>
<td>22</td>
<td>46</td>
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</table>

Convolution of tiles in parallel

<table>
<thead>
<tr>
<th>10</th>
<th>20</th>
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</thead>
<tbody>
<tr>
<td>15</td>
<td>18</td>
</tr>
</tbody>
</table>

Inter operation parallelism across operators

Parallel execution

- 1x1 Conv
- 3x3 Conv
- 5x5 Conv
- concat
Example Challenge 4: Optimizing the Data Layer

- Data Layer comprises 3 major ops
  - Read data
  - Decode data: e.g. JPEG decode, decompression
  - Transform data
- Result of read, decode & transform is input to DNN layers
- Reduce number of cores dedicated to feed DNN
  - IO optimization: consider compression
  - Decode: consider LMDB instead of JPEG
  - Resizing/data processing: consider pre-processing
  - Then vectorize, parallelize
Optimizing Deep Learning Frameworks for Intel® Architecture

- Leverage high performant compute libraries and tools
  - e.g. Intel® Math Kernel Library, Intel® Python, Intel® Compiler etc.
- Data Format/Shape:
  - Right format/shape for max performance: blocking, gather/scatter
- Data Layout:
  - Minimize cost of data layout conversions
- Parallelism:
  - Use all cores, eliminate serial sections, load imbalance
- Other Functions/Primitives (un-optimized in libraries):
  - Optimize via compiler knobs, improve existing implementations
- Memory allocation
  - unique characteristics and ability to reuse buffers
- Data layer optimizations:
  - parallelization, vectorization, IO
- Optimize hyper parameters:
  - e.g. batch size for more parallelism
  - learning rate and optimizer to ensure accuracy/convergence
AlexNet Optimization Progression

Cumulative speedup

- Baseline
- MKL Integration
- Thread Optimization
- Compiler Knobs Tuning
- Matrix Transpose/Data
- Memory Allocations
- Conversions Optimization
- Memory Allocation

Broadwell vs. Knights Landing

- 1.00x
- 2.20x
- 2.16x
- 4.18x
- 6.96x
- 7.72x
- 9.27x
- 13.36x
- 13.72x
- 40.71x
- 49.07x
VGG Optimization Progression

Cumulative Speedup

- Baseline
- MKL Integration
- Thread Optimization
- Compiler Knobs Tuning
- Matrix Transpose/Data Transformations
- Memory Allocations
- Conversions Optimization

Broadwell
Knights Landing
Configuration details

Intel® Xeon™ processor E5-2699v4 (22 Cores, 2.2 GHz), 128GB DDR memory, Centos 7.2 based on Red Hat* Enterprise Linux 7.2

Intel® Xeon Phi™ processor 7250 (68 Cores, 1.4 GHz, 16GB MCDRAM: Flat mode), 96GB DDR memory, Centos 7.2 based on Red Hat* Enterprise Linux 7.2

AlexNet and VGG benchmarks:

https://github.com/soumith/convnet-benchmarks
Multi-Node Distributed Training

• Model Parallelism
  • Break the model into $N$ nodes
  • The same data is in all the nodes

• Data Parallelism
  • Break the dataset into $N$ nodes
  • The same model is in all the nodes
  • Good for networks with few weights, e.g. GoogLeNet

• You can use either model or data parallelism or a hybrid of both
Data Parallelism

Training Data 0

Training Data 31

Worker 0

Worker 31

update model weights
Scaling Efficiency: Intel® Xeon Phi™ Processor

Deep Learning Image Classification Training Performance: MULTI-NODE Scaling

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Configurations:

* Intel® Xeon Phi™ Processor 7250 (68 Cores, 1.4 GHz, 16GB MCDRAM), 128 GB memory, Red Hat® Enterprise Linux 6.7, Intel® Optimized Framework
Multi-node Challenges

- Need to optimize both compute (iteration) and communication (weight updates)
- More nodes mean higher batch per iteration
  - Enough work for each node
- Optimized hyper parameters (e.g. Batch Size)
  - Time to Train: increases with batch size
  - Accuracy: batch size impacts convergence and accuracy
- Communication overheads if small per node batch
  - e.g. Total batch size = 1024
    - 1024 nodes: Batch size = 1 per node – **communication** dominates
    - 64 nodes each: Batch size = 16 per node – **computation** dominates

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*Time To Train (TTT)*

**batch size**

*sweet spot*
Summary

• Don’t be fooled by performance of DL workloads when using unoptimized frameworks

• Significant performance headroom from optimization on Xeon and Xeon Phi
  • Close to 300x speedup in certain topologies

• Traditional vectorization and parallelization strategies apply

• Other unique performance challenges: hyper parameters, data layer, inter/intra layer parallelization, etc.

• Call to action:
  • Try Intel optimized frameworks available today, more to come soon
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