INTEL® Fully Buffered DIMM

SPECIFICATION ADDENDUM

Rev. 0.9
March 21, 2006

TABLE OF CONTENTS

1 Document Organization

1.1 Revision History

Revision Info	Page of Revision	Description of Change
0.85		First revision of this document
0.90	9	Update latency definitions to reflect that they are DIMM specifications.
	10	Update "AMB Latency Range Table" with DIMM flight times that need to be deducted from the DIMM measurement numbers.
	11	Add CMD2DATANXT requirements
	19	Change from "Utilize service condition A" to "Utilize service condition B"
	21	Remove original section 7.4, 7.5, and 7.6
	24	Update 7.6 Appendix A "Thermal Resistance" Table values Update note 2 and 3 of the table
	30	Update Byte 17 and 18 SPD available values per JEDEC update
	33	Update Byte 99 suggested program value table
	34	Add Section 13 "OVERTEMP Function of the AMB"

1.2 Related Documents

Document	Revision	Description
FB-DIMM Architecture & Protocol Specification		Architecture and protocol specification for FB-DIMM channel.
FB-DIMM Link Signaling Specification		FB-DIMM Electrical Specification. PTP Link parameters: signaling, I/O, and AC and DC Parameters.
FB-DIMM AMB Specification		AMB Characteristics: pinout, package type, mechanical outline, footprint, AC/DC specs, power/thermal requirements, buffer TPT, special feature requirements, and basics DFT.
FB-DIMM Design Specification		FB-DIMM MIMM module parameters, multiple raw card designs, block diagrams, net topologies, routing details, timing budget, pinout, mechanical outline, stack up and SPD requirements.
DDR2 JEDEC Component Spec		JEDEC DDR2 SDRAM Data Sheet ####
FB-DIMM SPD Specification		Serial Presence Detect (SPD) values for FB-DIMMs.

1.3 Objective

This Specification addendum includes additional FBD and AMB specification information beyond the JEDEC standard. The intent of this document is to clarify and detail specifications so as to create a more robust, cost effective, compatible, and interoperable solution for Fully Buffered DIMMs (FBD).

The spec addendum represents Intel desired one voice data that is required for Intel products, which will be driven in the industry for acceptance.

2 AMB Air Flow Resistance

2.1 Introduction

Due to the variety of AMB thermal solutions currently in development, the system designers need to account for varying airflow requirements while developing systems to support Fully Buffered DIMMs (FBD). Of concern is the varying airflow impedance of the thermal solutions, which drive significantly different airflow delivery requirements of the system. There are 3-Type categorizations of DIMM Impedance which can help system designers more discretely identify the airflow requirements of a particular DIMM. The impedance values will be based on measurements conducted with a memory fixed approach velocity of 600lfm as given below:

• Type 1: 0.08 – 0.13 in H2O
• Type 2: 0.13 – 0.20 in H2O
• Type 3: 0.20 – 0.28 in H2O

See Figure 1 for impedance curves of the 3 DIMM types.

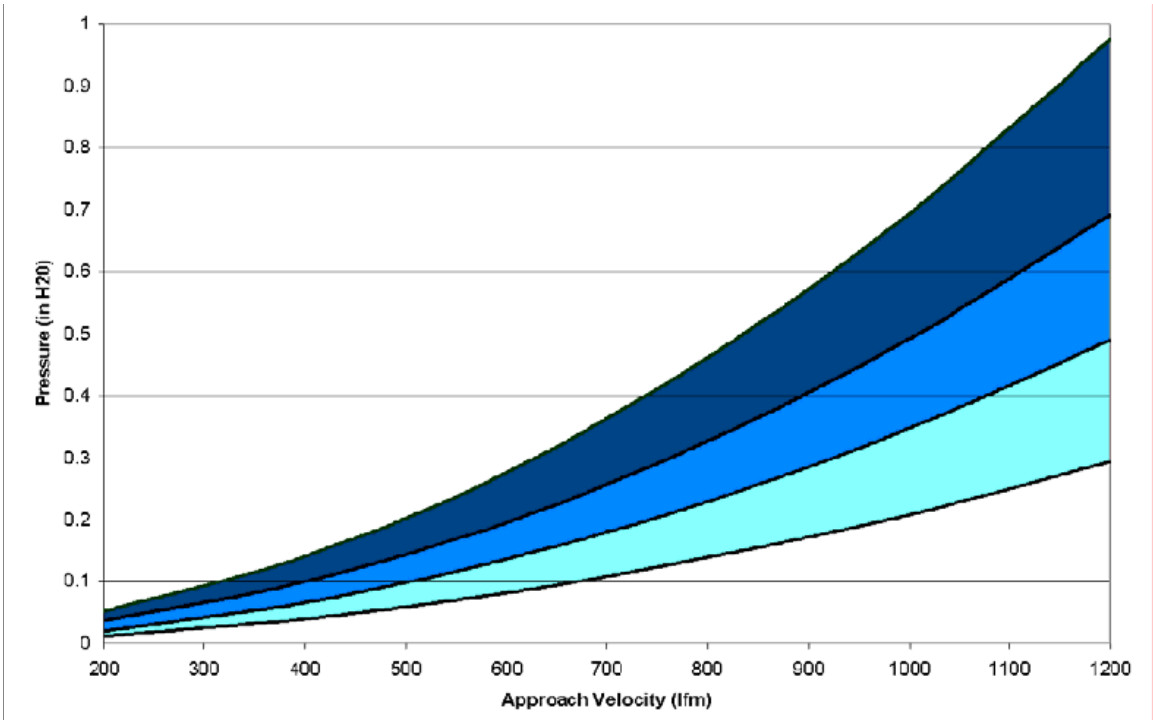


Figure 1: FBD 3-Type Impedance Characterization

Implementation of this strategy requires standardization of the airflow measurement technique. This spec addendum describes a process for airflow impedance characterization of a DIMM array using an airflow bench for air delivery, flow measurement, and impedance measurement.

*** FBD Airflow Impedance compliance testing and characterization is not included in the Intel Validation Suite reference.**

2.2 Airflow Supply and Measurement

Airflow impedance through an array of Fully Buffered DIMMs in a test fixture can be made using a metered airflow chamber designed in accordance with AMCA 210-99/ASHRAE 51-19 (Figure 2). These airflow chambers, also known as flow-benches, measure pressure drop across a calibrated nozzle to determine volumetric airflow rates. Additionally, they are equipped to measure the impedance across a test section, in this case an array of DIMMs.

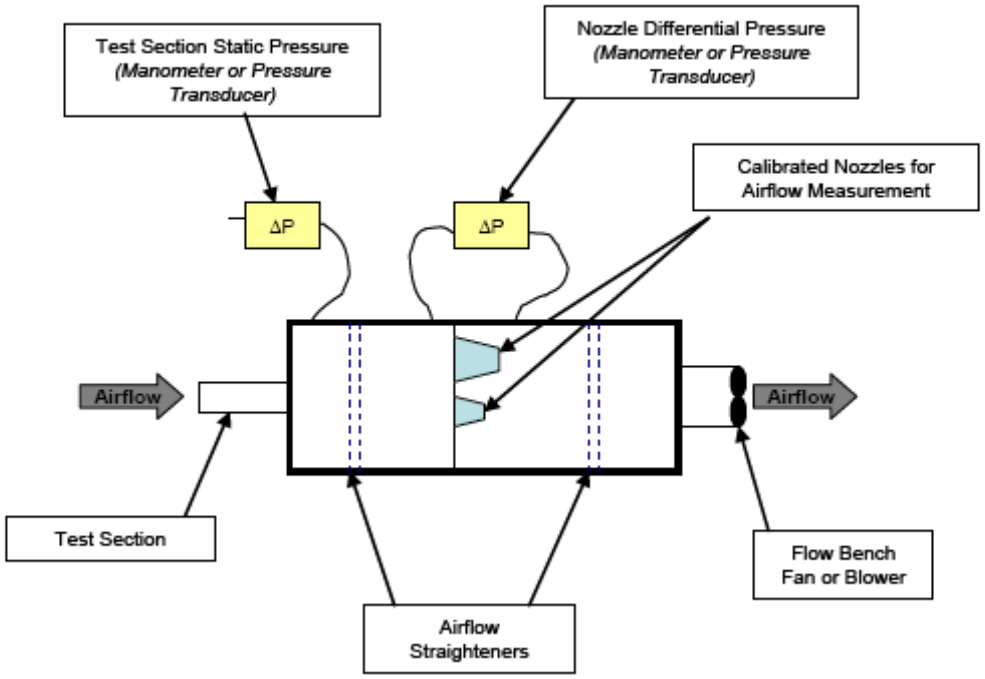
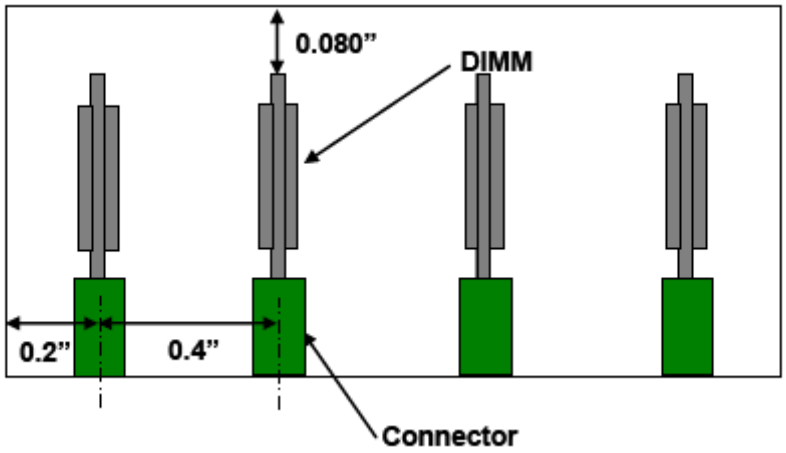


Figure 2: AMCA 210-99/ASHRAE 51-19 Airflow Measurement Chamber

Hot wire anemometers in a wind tunnel can also be used to measure velocity and calculate flow rate through a test fixture. If velocity measurements are used to calculate flow rates, airflow should be fully developed and laminar, however using velocity measurements to calculate flow rate is less accurate then using a flow bench.

2.3 Test Fixture

A 4-DIMM array was used for developing the impedance characterization in Figure 1. The DIMMs tested had a 0.400" center-to-center spacing (Figure 3) and this array was centered in a 35.25" long duct, which was fixtured to the end of the flow bench (Figure 4). The flow bench was used to generate the airflow for the characterization testing.



Where:
DIMM Pitch: 0.4"
Distance between Top of the DIMM to the ceiling of the chamber: 0.080"
Distance between the side of the chamber to the center line of the adjacent DIMM: 0.2"

Figure 3: DIMM Array Cross-Section for Flow Bench Impedance Characterization

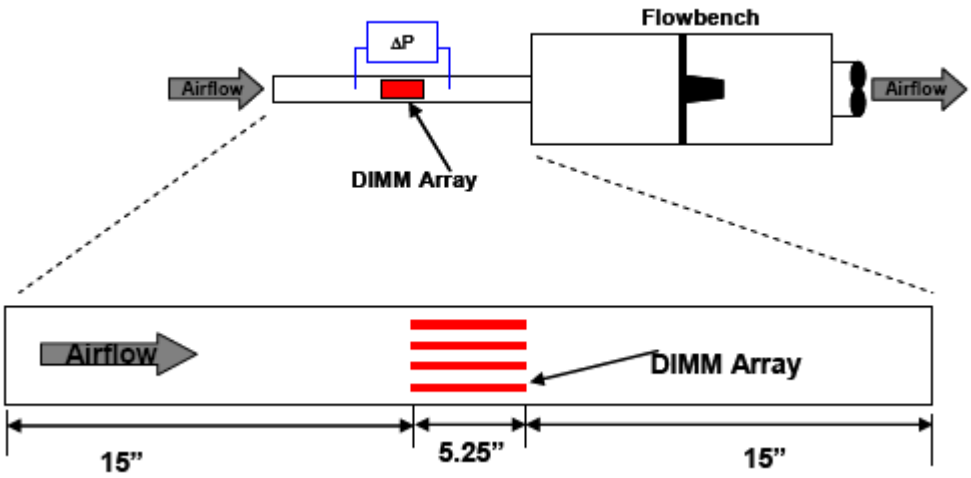


Figure 4: DIMM Fixture Length

2.4 Impedance Measurement

A calibrated pressure transducer or a liquid manometer should be used to take pressure readings for both the nozzle differential pressure to determine airflow rate, as well as to measure the impedance across the DIMM test fixture.
The flow bench described above provides a pressure tap inside of the flow chamber which can be used to determine a pressure difference between the outside air and the air inside the chamber, downstream of the test section. The "Test Section Static Pressure" box in Figure 2 illustrates this.
This measurement captures the pressure drop across the entire test section, but it includes effects of both the test section, and the test duct shown in Figure 4. To isolate the impedance of the DIMM Array from the impedance of the air duct, one can observe that because the air duct impedance is dominated by entrance and exit losses, with minor impacts due to channel length, in this instance:

$$\Delta P_{DIMMs+Duct} = \Delta P_{DIMMS} + \Delta P_{Duct}$$

Simply stated, the impedance of the DIMMs can be found by subtracting the impedance of the empty duct from the impedance of the DIMMs in the duct. For example, consider the sample data in Table 1. The reported value of a DIMM Array's impedance at 600 feet/minute approach air velocity would be 0.11 inches of water, as shown in the right-most column.

Table 1: Sample Impedance Data

Approach Velocity (LFM)	Impedance of DIMMs in Duct (inches H2O)	Impedance of Empty Duct (inches H2O)	Impedance of DIMMs (inches H2O)
600	0.17	0.06	0.11

3 FB-DIMM and AMB Latency Range

Refer to JEDEC FB-DIMM AMB spec for tRESAMPLE and tRESYNC definition.

3.1 FB-DIMM Latency Range

DIMM latency bounds are critical in order to insure interoperability between different DIMMs and different AMBs. These bounds result in a worst case channel-to-channel skew for lock-stepped channels that does not exceed the host controller's ability to de-skew. DIMM skew is a function of both DIMM channel length and AMB latency, so both are specified.

AMB latency ranges are a function of DIMM latency ranges, when northbound and southbound channel lengths on the DIMMs are known. DIMM latency ranges are specified in the following table. Values for both northbound (NB) and southbound (SB) are listed since DIMM routing varies between NB and SB.

AMB latency ranges are represented as a function of the DIMM latency ranges, and therefore also have both a NB and SB value tabulated.

Parameter	Data Rate	Min	Max	Units
tC2D_DIMM	533	20.7	25.5	nS
	667	17.5	21.5	nS
tRESAMPLE_DIMM_SB	533	1.4	2.7	nS
	667	1.4	2.4	nS
tRESAMPLE_DIMM_NB	533	1.3	2.6	nS
	667	1.3	2.3	nS
tRESYNC_DIMM_SB	533	2.8	4.4	nS
	667	2.5	3.7	nS
tRESYNC_DIMM_NB	533	2.7	4.3	nS
	667	2.4	3.6	nS

Notes:

tC2D_DIMM = Measured delay at FBDIMM gold finger between the center of the1st UI of command frame on the primary southbound lane 8[1] (connector pins 102 & 103) and the center of the 1st UI of return data on the primary northbound lane 0 (connector pins 22 & 23) – [CL (DRAM CAS latency) value] * [frame clock period – AL (DRAM additional latency) value * frame clock period].

tRESAMPLE_DIMM_SB = Measured delay at FBDIMM gold finger between the center of the 1st UI of a frame on the primary southbound lane 8 (connector pins 102 & 103) and the center of the 1st UI of the same frame on the secondary southbound lane 8 (connector pins 222 & 223).

[1] This definition assumes that there is no large skew between the arrival times of the SB lanes at the gold finger. If the skew is larger than 150ps (about one inch of micro strip trace), a lane other than SB lane 8 could be the latest arriving lane at the AMB balls, and this lane has to be used for the tC2D_DIMM measurement instead of lane 8. In order to simplify the measurement, it is required to ensure that no other lane arrives later than 150ps after the SB 8 lane at the gold finger.

tRESAMPLE_DIMM_NB = Measured delay at FBDIMM gold finger between the center of the 1st UI of a frame on the secondary northbound lane 0 (connector pins 142 & 143) and the center of the 1st UI of the same frame on the primary northbound lane 0 (connector pins 22 & 23).

tRESYNC_DIMM_SB = Measured delay at FBDIMM gold finger between the center of the 1st UI of a frame on the primary southbound lane 8 (connector pins 102 & 103) and the center of the 1st UI of the same frame on the secondary southbound lane 8 (connector pins 222 & 223).

tRESYNC_DIMM_NB = Measured delay at FBDIMM gold finger between the center of the 1st UI of a frame on the secondary northbound lane 0 (connector pins 142 & 143) and the center of the 1st UI of the same frame on the primary northbound lane 0 (connector pins 22 & 23).

3.2 AMB Latency Range

Parameter	Data Rate	Min	Max	Units
tRESAMPLE_AMB_SB	533	tRESAMPLE_DIMM_SB_533 (min) - 0.50	tRESAMPLE_DIMM_SB_533 (max) - 0.50	nS
	667	tRESAMPLE_DIMM_SB_667 (min) - 0.50	tRESAMPLE_DIMM_SB_667 (max) - 0.50	
tRESAMPLE_AMB_NB	533	tRESAMPLE_DIMM_NB_533 (min) - 0.44	tRESAMPLE_DIMM_NB_533 (max) - 0.44	nS
	667	tRESAMPLE_DIMM_NB_667 (min) - 0.44	tRESAMPLE_DIMM_NB_667 (max) - 0.44	
tRESYNC_AMB_SB	533	tRESYNC_DIMM_SB_533 (min) - 0.50	tRESYNC_DIMM_SB_533 (max) - 0.50	nS
	667	tRESYNC_DIMM_SB_667 (min) - 0.50	tRESYNC_DIMM_SB_667 (max) - 0.50	
tRESYNC_AMB_NB	533	tRESYNC_DIMM_NB_533 (min) - 0.44	tRESYNC_DIMM_NB_533 (max) - 0.44	nS
	667	tRESYNC_DIMM_NB_667 (min) - 0.44	tRESYNC_DIMM_NB_667 (max) - 0.44	

Notes:

tRESAMPLE_AMB_SB = Measured delay at AMB balls between the center of the 1st UI of a frame on the primary southbound lane 8 (AMB balls U29 & U28) and the center of the 1st UI of the same frame on the secondary southbound lane 8 (AMB balls Y26 & W26).

tRESAMPLE_AMB_NB = Measured delay at AMB balls between the center of the 1st UI of a frame on the secondary northbound lane 0 (AMB balls V4 & V5) and the center of the 1st UI of the same frame on the primary northbound lane 0 (AMB balls U1 & U2).

tRESYNC_AMB_SB = Measured delay at AMB balls between the center of the 1st UI of a frame on the primary southbound lane 8 (AMB balls U29 & U28) and the center of the 1st UI of the same frame on the secondary southbound lane 8 (AMB balls Y26 & W26).

tRESYNC_AMB_NB = Measured delay at AMB balls between the center of the 1st UI of a frame on the secondary northbound lane 0 (AMB balls V4 & V5) and the center of the 1st UI of the same frame on the primary northbound lane 0 (AMB balls U1 & U2).

3.3 AMB CMD2DATANXT Utilization for Merge Data Training

AMB designs support a limited range of CMD2DATANXT register settings during runtime. (Refer to the JEDEC AMB Component Specification).

In addition, the AMB CMD2DATANXT mechanism will be used temporarily by memory reference code during memory subsystem training to train each memory channel with adequate timing margin to prevent Merge Data errors when mixing different AMB's on a channel. Memory reference code will over ride the SPD CMD2DATANXT value only during Merge Data training, and not while accessing DRAM. Once training completes, the original CMD2DATANXT value will be restored before normal system operation initiates.

AMB designs need to support a range of CMD2DATANXT values for purposes of non-DRAM access, Merge Data training ONLY. The supported range needs to extend at least 16UI higher than the value recommended and specified in the SPD for normal operation.

AMB designs that do not support a particular DLYFRAC value due implementation granularity must functionally round up to the next supported value.

CMD2DATANXT Register Definition

Function:1 **Offset:E8h**			
Bit	**Attr**	**Default**	**Description**
7:4	RWST	0h	**DLYFRMS: Number of frames** This specifies full frame delay part of the command to data delay. 0 - 9: Valid delays 10 - 15: Reserved
3:0	RWST	0h	**DLYFRAC: Fractional delay of command to data** This specifies fractional frame delay part of the command to data delay. 0 - 11: Specifies the delay in 1UI increments 12 - 15: Reserved

4 AMB Power Measurement and Power Specification

AMB Power is measured with DIMMs installed in an FBD platform. This provides a real world conditions for the measurement process. The document AMB Current/Power Measurement Procedure: AMB-FBDIMM provides the step by step procedure, as well as all of the hardware and software requirements.

Current and Power Specification for x8 DIMMs.

			533 MHz		667 MHz		800 MHz		
Symbol	Conditions	Power Supply	Thermal Design	Max Current	Thermal Design	Max Current	Thermal Design	Max Current	Units
Idd_Idle_0	**Idle Current, single or last DIMM** L0 state, idle (0 BW) Primary channel enabled, Secondary Channel Disabled CKE high. Command and address lines stable. DRAM clock active.	1.5V	2.1	2.2	2.4	2.6	TBD	TBD	A
		1.8V	0.6	0.7	0.6	0.7	TBD	TBD	A
		Power	3.5		4.0		TBD		W
Idd_Idle_1	**Idle Current, first DIMM** L0 state, idle (0 BW) Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	1.5V	2.7	3.0	3.1	3.4	TBD	TBD	A
		1.8V	0.6	0.7	0.6	0.7	TBD	TBD	A
		Power	4.6		5.1		TBD		W
Idd_TDP_0	**Active Power, TDP BW, Single or Last DIMM** L0 state TDP Channel BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 DIMM BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 67% read, 33% write. Primary channel Enabled Secondary channel Disabled CKE high. Command and Address	1.5V	2.4	2.6	2.8	3.0	TBD	TBD	A
		1.8V	1.1	1.3	1.2	1.3	TBD	TBD	A
		Power	5.2		5.8		TBD		W
Idd_TDP_1	**Active Power, TDP BW, First DIMM** L0 state TDP Channel BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 DIMM BW =2/3 Channel BW = 1.3GB/s@533; 1.6GB/s@667; 2GB/s@800 67% read, 33% write. Primary channel Enabled Secondary channel Enabled CKE high. Command and Ad	1.5V	3.0	3.3	3.5	3.8	TBD	TBD	A
		1.8V	0.9	1.0	0.9	1.0	TBD	TBD	A
		Power	5.8		6.4		TBD		W
Idd_Active_1	**Active Power** L0 state. 50% DRAM BW, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.	1.5V	3.1	3.4	3.6	3.9	TBD	TBD	A
		1.8V	1.2	1.3	1.2	1.3	TBD	TBD	A
		Power	6.4		7.1		TBD		W
Idd_Active_2	**Active Power, data pass through** L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	1.5V	2.9	3.2	3.3	3.7	TBD	TBD	A
		1.8V	0.6	0.7	0.6	0.7	TBD	TBD	A
		Power	5.0		5.6		TBD		W
Idd_Training	**Training** Primary and Secondary channels enabled. 100% toggle on all channel lanes DRAMs idle. 0 BW. CKE high, Command and address lines stable. DRAM clock active.	1.5V		3.5		4.0	TBD	TBD	A
		1.8V		0.7		0.7	TBD	TBD	A
Idd_IBIST	**IBIST** Over all IBIST modes DRAM Idle (0 BW) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active	1.5V		3.8		4.5	TBD	TBD	A
		1.8V		0.7		0.7	TBD	TBD	A
Idd_MEMBIST	**MemBIST** Over all MemBIST modes >50% DRAM BW (as dictated by the AMB) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active	1.5V		3.3		3.8	TBD	TBD	A
		1.8V		2.1		2.1	TBD	TBD	A
Idd_EI	**Electrical Idle** DRAM Idle (0 BW) Primary channel Disabled Secondary channel Disabled CKE low. Command and Address lines Floated DRAM clock active, ODT and CKE driven low	1.5V		2.0		2.5	TBD	TBD	A
		1.8V		0.2		0.2	TBD	TBD	A

Current and Power Specification for x4 DIMMs.

			533 MHz		667 MHz		800 MHz		
Symbol	Conditions	Power Supply	Thermal Design	Max Current	Thermal Design	Max Current	Thermal Design	Max Current	Units
Idd_Idle_0	**Idle Current, single or last DIMM** L0 state, idle (0 BW) Primary channel enabled, Secondary Channel Disabled CKE high. Command and address lines stable. DRAM clock active.	1.5V	2.1	2.2	2.4	2.6	TBD	TBD	A
		1.8V	0.9	0.9	0.9	0.9	TBD	TBD	A
		Power	3.9		4.4		TBD		W
Idd_Idle_1	**Idle Current, first DIMM** L0 state, idle (0 BW) Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	1.5V	2.7	3.0	3.1	3.4	TBD	TBD	A
		1.8V	0.9	0.9	0.9	0.9	TBD	TBD	A
		Power	4.9		5.5		TBD		W
Idd_TDP_0	**Active Power, TDP BW, Single or Last DIMM** L0 state TDP Channel BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 DIMM BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 67% read, 33% write. Primary channel Enabled Secondary channel Disabled CKE high. Command and Address	1.5V	2.4	2.6	2.8	3.0	TBD	TBD	A
		1.8V	1.5	1.6	1.5	1.6	TBD	TBD	A
		Power	5.9		6.5		TBD		W
Idd_TDP_1	**Active Power, TDP BW, First DIMM** L0 state TDP Channel BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 DIMM BW =2/3 Channel BW = 1.3GB/s@533; 1.6GB/s@667; 2GB/s@800 67% read, 33% write. Primary channel Enabled Secondary channel Enabled CKE high. Command and Ad	1.5V	3.0	3.3	3.5	3.8	TBD	TBD	A
		1.8V	1.3	1.4	1.3	1.4	TBD	TBD	A
		Power	6.3		6.9		TBD		W
Idd_Active_1	**Active Power** L0 state. 50% DRAM BW, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.	1.5V	3.1	3.4	3.6	3.9	TBD	TBD	A
		1.8V	1.6	1.7	1.6	1.7	TBD	TBD	A
		Power	6.9		7.6		TBD		W
Idd_Active_2	**Active Power, data pass through** L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	1.5V	2.9	3.2	3.3	3.7	TBD	TBD	A
		1.8V	0.9	0.9	0.9	0.9	TBD	TBD	A
		Power	5.5		6.1		TBD		W
Idd_Training	**Training** Primary and Secondary channels enabled. 100% toggle on all channel lanes DRAMs idle. 0 BW. CKE high, Command and address lines stable. DRAM clock active.	1.5V		3.5		4.0	TBD	TBD	A
		1.8V		0.9		0.9	TBD	TBD	A
Idd_IBIST	**IBIST** Over all IBIST modes DRAM Idle (0 BW) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active	1.5V		3.8		4.5	TBD	TBD	A
		1.8V		0.9		0.9	TBD	TBD	A
Idd_MEMBIST	**MemBIST** Over all MemBIST modes >50% DRAM BW (as dictated by the AMB) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active	1.5V		3.3		3.8	TBD	TBD	A
		1.8V		2.4		2.4	TBD	TBD	A
Idd_EI	**Electrical Idle** DRAM Idle (0 BW) Primary channel Disabled Secondary channel Disabled CKE low. Command and Address lines Floated DRAM clock active, ODT and CKE driven low	1.5V		2.0		2.5	TBD	TBD	A
		1.8V		0.2		0.2	TBD	TBD	A

5 S3 current Specification

S3 is an ACPI mode in which the DIMMs are put into a very lower power state, with the DRAMs in self refresh mode. This AMB S3 current specification is required for the sizing of the power supply used for the S3 mode.

In this mode is defined as:
DRAMs in self refresh.
AMB maintaining the DRAMs in self refresh by driving the CKE signals low.
REFCLK not toggling.
VDD = VDDmax (1.9V).
VCC = 0V
VTT = 0V

			533 MHz		667 MHz		800 MHz		
Symbol	Conditions	Power Supply	Nominal	Max Current	Nominal	Max Current	Nominal	Max Current	Units
Idd_S3	**S3 current** VDD = 1.9V VCC = 0V VTT = 0V Across process variations Across the operating TCASE temperature range. DIMM types: Raw Card A, B, C, D, E, H, & J.	VDD (1.8V)		75		75		75	mA

Note that the total DIMM current will include the AMB IDD_S3 value as well as the self refresh current of all of the DRAMs on the DIMM.

6 DIMM Heat Spreader Mechanical Requirements

The objective of defining the mechanical requirements is to ensure that the FB DIMM Heat Spreader are sufficiently robust to withstand shocks when shipped on a board in a system, withstand vibration when mounted in a system which is being shipped and to withstand shock of dropping the DIMM's in their free state onto a floor during handling. The first two cases are performed on a unpackaged board whereas the third case is performed on a FB DIMM in its free state (not attached to a board). Board unpackaged testing does not pre-qualify a board for shipping as a un-mounted unit inside a shipping container.

6.1 Shock Testing of a Unpackaged Board with FB DIMMs

The test will be performed on at least 2 FB DIMMs in one Customer Reference Board (CRB) or an equivalent board product. The Board will be configured as in a complete system with all the other memory slots populated, processors installed and where possible, any required support cards will also be installed. The board must be mounted in a rigid fixture that duplicates the support points in the actual application of the board.

Test Objective

Trapezoidal shock	50 g ± 10%
Velocity change	170 inches/sec, ± 10%
Duration	Not Specified

Three drops in each of the six directions are applied to the board sample.

Expected Failure Mechanisms

1. Displaced or dislodged FB DIMM from the DIMM connector.
2. Displaced or dislodged Heatspreader/Clip from the FB DIMM Raw Cards

Pass Criteria

1. No visible damage
2. No displacement of FB DIMM from the connector
3. No displacement of heat spreader or clips from the FB DIMM Raw Cards

Basis for Profile

1. Specification limits are defined by Intel Corporation
2. MIL-STD-810E, Method 516, Transportation and Application Environments was the source of the test profile used here.
3. The board shock is more stressful that the system shock to guardband for the amplification that can be generated by a chassis. The board shock defined in this test is similar to shocks measured during system package testing on boards inside a packaged system.
4. Mounting a board to a rigid test fixture as defined in this test does not simulate stresses inside a board shipping container
5. The recommended filter frequency for response waveform collection is only a suggestion, using a common waveform filter frequency on all tests allows easier comparison of data taken at package, system or board level tests.
6. The rigid fixture used to mount the board must not amplify the stress being applied by to the shock table to the board. The fixture usually consists of a 1-inch aluminum plate with standoffs mounted in the proper position to duplicate the support of the chassis.

7. Care should be taken to use only those support points that will actually be used in mounted the board to an actual chassis.
8. The testing should be conducted on a programmable shock machine.
    a. Table drop height and programmer pressure is adjusted to produce the desired delta velocity of ~170 inches/sec and ~50 g
    b. Table response used to set the desired input shock is to be filtered using a frequency 20 times the fundamental frequency of the input waveform

        Example: f = (1/(t x2) x 20
9. The board is then mounted to the table and dropped. Recommended filter frequency for any response waveform data collection is 225 Hz
10. Three drops in each of the six directions are applied to the board sample.

6.2 Vibration Testing of a Unpackaged Board with FB DIMMs

The test will be performed on at least 2 FB DIMMs in one Customer Reference Board (CRB) or an equivalent board product. The Board will be configured as in a complete system with all the other memory slots populated, processors installed and where possible, any required support cards will also be installed. The board must be mounted in a rigid fixture that duplicates the support points in the actual application of the board.

Test Objective

Random Profile: 5 Hz @ 0.01 g^2/Hz t 20 Hz @ 0.02 g^2/Hz (slope up)
20Hz to 500Hz @ 0.02 g^2/Hz (flat)
Input acceleration is 3.13 g RMS
10 minutes per axis for all 3 axes
Random control limit tolerance is ± 3 dB

Expected Failure Mechanisms

1. Displaced or dislodged FB DIMM from the DIMM connector.
2. Displaced or dislodged Heatspreader/Clip from the FB DIMM Raw Cards
3. Cracking or breaking of FB DIMM Raw Cards

Pass Criteria

1. No visible damage
2. No displacement of FB DIMM from the connector
3. No displacement of heat spreader or clips from the FB DIMM Raw Cards

Basis for Profile

1. Specification limits are defined by Intel Corporation
2. MIL-STD-810E, Method 516, Transportation and Application Environments was the source of the test profile used here.
3. The board should be mounted in a rigid fixture that duplicates the support points in the actual application of the board.
4. The fixture must not amplify the stress being applied by the table to the board. The fixture usually consists of a 1-inch aluminum plate with standoffs mounted in the proper position to duplicate the support of the chassis.
5. Care should be taken to use only those support points that will actually be used in the final product.
6. Vibrate per profile in all 3 axes for 10 minutes per axis.
7. The FB DIMM module should be inspected for damage after the tests.

6.3 Shock Testing of a FB DIMM in its free state

This test will determine the robustness of the modules under mechanical shock in its free state to simulate dropping them for a height. A minimum sample size of 5 modules shall be used.

Test Method:
Reference JESD22-B110 "Subassembly Mechanical Shock". Perform visual inspection and test each module for functionality prior to testing. Utilize service condition B (1500G @ 0.5 ms shock pulse height) or any of the other service conditions listed in the Table 1 in JESD22-B110. Each module shall experience 5 shocks on each direction on each of the three axis of the module.

Expected Failure Mechanisms

1. Visual damage to the modules

Pass Criteria

1. No visible damage
2. Modules are functional

7 DIMM Thermal Resistance

7.1 DIMM Thermal Characterization

System thermal management must match the thermal characteristics of the DIMM with the system cooling capability. The required DIMM thermal characteristics for lower airflow system conditions are the thermal resistances of the devices on the DIMM. These thermal resistance values are included in the JEDEC SPD standard as bytes 94-97. Intel supports the JEDEC specification and definition of these bytes. Before a standard measurement process can be put in place, Intel also supports the specification of 'category' bits, bits [5:0] of SPD byte 99. These 'category' bits are simple physical descriptions of the DIMM such as DRAM and heat spreader types. Intel will use these simple physical descriptions to establish buffer and DRAM thermal resistance values that will be used by systems. Intel will test for compliance to these thermal resistance values, which are listed in Appendix A. This document will outline the following:

1. SPD definitions for Thermal Characterization
2. Thermal Resistance Values for DIMMs
3. Thermal Resistance test Methodology

7.2 SPD Definitions for Thermal Resistance

The following are SPD DIMM thermal characterization byte definitions.

Bytes 94-97 are thermal resistance of the AMB and DRAM devices on the FB DIMM. The byte definitions are a JEDEC standard.

SPD BYTE LOCATION	BYTE NAME	BYTE DEFINTION	COMMENT
Byte 94	Ψ_{AMB}	Thermal Resistance of AMB Junction to Ambient	
Byte 95	$\Psi_{AMB\text{-}DRAM}$	Thermal Resistance of AMB Junction to DRAM Case	
Byte 96	Ψ_{DRAM}	Thermal Resistance of DRAM Case to Ambient	
Byte 97	$\Psi_{DRAM\text{-}AMB}$	Thermal Resistance of DRAM case to AMB junction	

The following DIMM thermal characterization bytes are simple physical descriptions of the DIMMs. These are referred to as 'category' bits. These bits are used to map to thermal resistance values (refer to Section 7.6) measured and tested by Intel in the absence of valid thermal resistance values specified in the SPD.

Byte 99, bits [5:3] are category bits that define the packaging types of the DRAM devices used on the DIMM. The package types used have different thermal resistances.

SPD BYTE LOCATION/BITS	VALUE	DRAM TYPE	DEFINTION	COMMENT
Byte 99 Bits [5:3]	000	Unknown	DRAM package type does not match the pre-defined type.	
	001	Planar	DRAM package type is a single die per package. Does not use package stacking or multi-die package technology.	Examples are FB DIMM Raw Cards E and H.

	010	Dual Die	DRAM package type is two die in a single DRAM package. Does not use package stacking technology.	
	011	Stacked	DRAM package type is two separate, packaged DRAM devices stacked on top of each other.	Example includes FB DIMM Raw Card D.
	100–111	Reserved	Reserved for future definitions.	

Byte 99, bits [2:0] are category bits that define heat spreader configuration of the DIMM. The heat spreader used impact the thermal resistances and thermal performance of the DIMM.

SPD BYTE LOCATION/BITS	VALUE	HS TYPE	DEFINTION	COMMENT
Byte 99 Bits [2:0]	000	Unknown	DIMM heat spreader type does not match the pre-defined type.	
	001	AMB Only	Heat spreader for AMB only. Contacts AMB only and covers AMB only. Does not extend over DRAM devices.	
	010	Full DIMM Heat Spreader	Heat spreader extends the entire length of the DIMM and covers the AMB and the DRAMs. Heat spreader exists for both sides of the DIMM.	Heat spreader is assumed to contact DRAM devices for best thermal performance.
	011–111	Reserved	Reserved for future definitions.	

7.3 Thermal Resistance Values for DIMM

Intel will use the Resistance Values as defined in Section 7.6 for the DIMM categories defined above. DIMMs will be tested for thermal performance to meet or exceed the values in the table.

7.4 Default Thermal Resistance Values Implementation

Current implementations of the Thermal Resistance Values include default values for two primary DIMM configurations: AMB-only heat spreader and full-DIMM heat spreader (see Section 7.6 for the default values).

An AMB-only heat spreader consists of a highly conductive heat spreader (nominally 25mm square thin copper sheet) mechanically attached to the DIMM with sufficient hold down force for effective thermal conduction across the interface. The larger area will provide a greater surface area for AMB heat removal by convection to the air, but at the expense of additional interface and spreading resistance. An optimal balance needs to be achieved. The heat spreader must be attached with a TIM in between the heat spreader and AMB. The TIM must meet or exceed the performance of Honeywell PCM45.

A full-DIMM heat spreader consists of thin sheets of highly conductive material on both sides of the DIMM. The heat spreader is typically aluminum or copper. These heat spreaders must have a mechanical attach method that allows good contact with ALL DRAM and the AMB. There must also be a TIM between EVERY component and the heat spreader; otherwise the heat spreader will actually reduce thermal performance by blocking airflow to the DRAM without the TIM, essentially acting as an insulator.

When the system sees values of 0 (zero) in the 4 Thermal Resistance Bytes (i.e. Byte 97, 96, 95, and 94), the system will read the Category Byte (i.e. Byte 99, Bit[5:0]), and use the default thermal resistance

values as defined in Appendix A. The implementation of these category Bytes allows the use of FBDs that have not been fully characterized in an airflow/power/temperature test and do not have DIMM specific Thermal Resistance Bytes determined.

Properly implemented heat spreader solutions should not have thermal problems through the use of these default values. DIMMs can be inspected for heat spreader type, connection method, and thermal interface material (TIM) presence. Proper use of these components can also be validated by running the DIMM in the thermal test set-up and verifying the thermal performance is within the default thermal envelope as defined by the default thermal values in Appendix A. Improper installation of thermal hardware or bad thermal design (e.g. no TIM between heat spreader and DRAMs) will cause the part to be rejected as it will not meet the default thermal performance.

7.5 Terminology

Case Temperature – The temperature at the external surface of the silicon component
AMB – Advanced Memory Buffer
DRAM – Dynamic Random Access Memory
DIMM – Dual in-line memory module
MRC – Memory Reference Code
TIM – Thermal Interface Material
Junction Temperature – The peak temperature internal to the silicon component
Ψ_x – Thermal resistance (in °C/W) from the component X to the ambient cooling airstream. For the AMB
Ψ_{xy} – Thermal resistance cross terms (in °C/W) with power from the component X through component Y

7.6 Appendix A

				Intel Spec Addendum Thermal Resistances															
Raw Card	DRAM Type	Heat Spreader Type	Byte 99 Bits (5:0)	Max Ramb (degC/W, at X m/s)				Max Rad (degC/W, at X m/s)				Max Rdram (degC/W, at X m/s)				Max Rda (degC/W, at X m/s)			
				1 m/s	1.5 m/s	3 m/s	5 m/s	1 m/s	1.5 m/s	3 m/s	5 m/s	1 m/s	1.5 m/s	3 m/s	5 m/s	1 m/s	1.5 m/s	3 m/s	5 m/s
A	Planar	AMB Only	001001	11.6	9.8	7.1	5.3	3.9	3.0	1.8	1.1	4.6	3.8	2.8	2.2	5.7	4.6	3.3	2.6
A	Planar	Full Dimm	001010	8.0	7.0	5.5	4.5	5.7	4.5	2.9	1.9	4.0	3.3	2.3	1.6	4.4	3.7	2.9	2.4
B	Planar	AMB Only	001001	11.2	9.3	6.6	4.9	5.3	4.1	2.6	1.8	4.9	4.0	2.7	1.8	4.3	3.4	2.2	1.5
B	Planar	Full Dimm	001010	8.0	7.0	5.5	4.5	5.7	4.5	2.9	1.9	4.0	3.3	2.3	1.6	4.4	3.7	2.9	2.4
C	Planar	AMB Only	001001	11.2	9.3	6.6	4.9	5.3	4.1	2.6	1.8	4.9	4.0	2.7	1.8	4.3	3.4	2.2	1.5
C	Planar	Full Dimm	001010	8.0	7.0	5.5	4.5	5.7	4.5	2.9	1.9	4.0	3.3	2.3	1.6	4.4	3.7	2.9	2.4
D/J	Stacked	AMB Only	011001	11.2	9.3	6.6	4.9	5.3	4.1	2.6	1.8	4.9	4.0	2.7	1.8	4.3	3.4	2.2	1.5
D/J	Stacked	Full Dimm	011010	8.0	7.0	5.5	4.5	5.7	4.5	2.9	1.9	4.0	3.3	2.3	1.6	4.4	3.7	2.9	2.4
D/J	Dual die	AMB Only	010001	11.2	9.3	6.6	4.9	5.3	4.1	2.6	1.8	4.9	4.0	2.7	1.8	4.3	3.4	2.2	1.5
D/J	Dual die	Full Dimm	010010	8.0	7.0	5.5	4.5	5.7	4.5	2.9	1.9	4.0	3.3	2.3	1.6	4.4	3.7	2.9	2.4
E/H	Planar	AMB Only	001001	11.4	10.0	8.1	6.8	4.0	3.0	1.8	1.1	3.1	2.5	1.8	1.4	5.1	4.4	3.4	2.8
E/H	Planar	Full Dimm	001010	8.0	7.0	5.5	4.5	5.7	4.5	2.9	1.9	4.0	3.3	2.3	1.6	4.4	3.7	2.8	2.3

Note 1: These maximum values must be met if SPD bytes 94:97 are zero

Note 2: If SPD bytes 94:97 are programmed, they effectively offset (up or down) the maximum curves by the difference between the byte and the maximum value listed in the 1.5 m/s column. For example, for a R/C A with AMB only, if byte 94 (Ramb) is programmed to 8.8 degC/W, then the curve should be lowered by (9.8 – 8.8) = 1.0 degC/W, and the adjusted maximum values would be 10.6, 8.8, 6.1 and 4.3 at the four air velocities.

Note 3. Thermal resistances measured with DIMMs on 0.40" pitch, with 1 mm gap between top of DIMMs and air guide

8 DDR2 DIMM Product Label

Background:

The DDR2 Module Label specification does not address FB-DIMM AMBs and with a full DIMM heat spreader you will not be able to tell what brand and version it is. We have found that matched AMB revisions in lockstep pairs provides the best performance, so we are proposing adding two new fields that will provide AMB and rev to the label.

DDR2 DIMM Label Format, End User Markets:

The following label shall be applied to all DDR2 memory modules targeted at end-user type products to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A minimum font size of 8 points should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields. If the part doesn't have an AMB the last field can be dropped.

ggggg eRxff PC2-wwwwm-abc-dd-ef-Ax

Where:

ggggg = Module total capacity, in bytes

256MB, 512MB, 1GB, 2GB, 4GB, etc.

eR = Number of ranks of memory installed

1R = 1 rank of DDR2 SDRAM installed

2R = 2 ranks

4R = 4 ranks

xff = Device organization (bit width) of DDR2 SDRAMs used on this assembly

x4 = x4 organization (4 DQ lines per SDRAM)

x8 = x8 organization

x16 = x16 organization

wwww = Module bandwidth in MB/s

3200 = 3.20 GB/s

4200 = 4.26 GB/s

5300 = 5.33 GB/s

6400 = 6.40 GB/s

m = Module Type

E = Unbuffered DIMM ("UDIMM"), with ECC (x72 bit module data bus)

F = Fully Buffered DIMM ("FB-DIMM")

M = Micro-DIMM

N = Mini-Registered DIMM ("Mini-RDIMM"), no address/command parity function

P = Registered DIMM ("RDIMM"), with address/command parity function

R = RDIMM, no address/command parity function

S = Small Outline DIMM ("SO-DIMM")

T = Mini-Registered DIMM ("Mini-RDIMM"), with address/command parity function

U = Unbuffered DIMM ("UDIMM"), no ECC (x64 bit module data bus)

a = DDR2 SDRAM CAS Latency, in clocks at maximum operating frequency

b = DDR2 SDRAM minimum tRCD specification, in clocks at maximum operating frequency

c = DDR2 SDRAM minimum tRP specification, in clocks at maximum operating frequency

dd = JEDEC SPD Revision Encoding and Additions level used on this DIMM

e = Reference design file used for this design (if applicable)

- A = Reference design for raw card 'A' is used for this assembly
- B = Reference design for raw card 'B' is used for this assembly
- Z = None of the reference designs were used for this assembly

f = Revision number of the reference design used

- 0 = Initial release
- 1 = First revision
- 2 = Second revision
- ⋮
- 9 = Ninth revision
- P = Pre-release or Engineering sample
- Z = To be used

A = AMB supplier

- N = I**n**tel
- D = I**D**T
- E = N**E**C
- I = **I**nfineon
- P = IN**P**HI
- M = **M**ontage

x = AMB rev number

- 0 = Initial release
- 1 = First revision
- 2 = Second revision
- ⋮
- 9 = Ninth revision
- P = Pre-release or Engineering sample
- Z = To be used

Examples, single font:

1GB 1Rx4 PC2-3200F-333-10-C0-N2

is a 1GB DDR2 Fully Buffered DIMM, using 1 rank of x4 SDRAMs operational to PC2-3200 performance with CAS Latency = 3, t_{RCD} = 3, t_{RP} = 3, using JEDEC SPD revision 1.0 (encoding type FB-DIMM), raw card reference design file C initial release used for the assembly, with Intel AMB second revision.

Examples, with font change:

512MB 1Rx8 PC2-6400F-555 11-A1-D2

is a 512MB DDR2 Fully Buffered DIMM, using 1 rank of x8 SDRAMs operational to PC2-6400 performance with CAS Latency = 5, t_{RCD} = 5, t_{RP} = 5, using JEDEC SPD revision 1.1, raw card reference design file A revision 1 used for the assembly, with IDT second revision.

9 DDR2 DRAM Temperature Requirement for FB-DIMM

Intel requires DRAMs to support both 85C single refresh and 95C double refresh. This is the standard FB-DIMM requirement.

10 Dual Differential Signals Strip-line Spacing Requirement for FB-DIMM Design

Noise can be coupled onto to a differential pair from a close-by differential pair running in parallel if a certain width to height ratio is not maintained. This addendum provides routing guidelines in the case when two strip-line differential signal pairs are routed in parallel. The intra-pair coupling could impact the proper termination and hence measure has to be taken to prevent reflection at the far end of the pairs.

The rules are as follows based on dimensions given in Fig.6.

1. For data to clock differential pairs,
    a. Nom (Xdiff + Ydiff) > 1.7 (S+H)

    Note:
    This dual strip line rule is applied in case that the signal lines are parallel to each other and the signals run in opposite directions of each other.

    This rule applies to coupling between high-speed data and other high-speed data signals or between high-speed data signals and the reference clock.

2. For data to data differential pairs,
    a. Nom (Xdiff + Ydiff) > 1.3 (S+H)

    Note:
    This dual strip line rule is applied in case that the signal lines are parallel to each other and the signals run in the same direction. An exception to this rule is allowed if the total parallel trace length is no more than 6mm.

    This rule only applies to coupling between high-speed data and other high-speed data signals

Note:

- Nom stands for nominal dimensions.
- H is the distance of the signal from the nearest ground layer

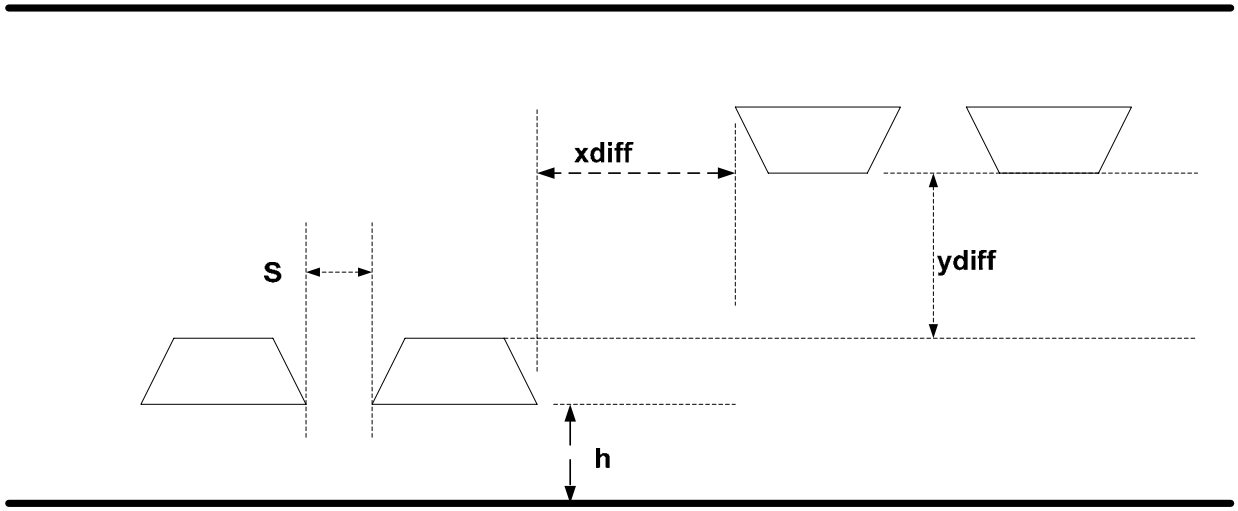


Fig 6. Dual-strip-line Differential Pairs

11 AMB Spec Ambiguities Clarification

11.1 TEMPSTAT register updates

Expect for the “increasing” bit, the bits of the tempstat register may update at any time. The temperature values may be but are not guaranteed to be latched by the AMB.

11.2 S3 restore registers

The functionality of the AMB S3 restore registers is design dependent. Some of the S3 restore registers may or may not be implemented depending the AMB design.

11.3 FERR register behavior

RECCFG: Configuration Register Error Log

This register contains the received address for an unimplemented configuration register access error. The contents of this register are only valid when the error that set this register is logged in the FERR or NERR register.

Device: NodeID **Function:** 1 **Offset:** 98h			
Bit	**Attr**	**Default**	**Description**
15:13	RV	0	**Reserved**
12:10	RWST	0h	**function**
9:8	RWST	0h	**size:** 00 = one byte 01 = two bytes 10 = three bytes 11 = four bytes **Note: This field is only defined for errors on Config Register Writes. This field is undefined for other transactions.**
7:0	RWST	0h	**register address**

11.4 Clarification of NBCALSTATUS write failure

NBCALSTATUS: Northbound Calibration Status

This register contains the pass/fail information of the last calibration on a per lane basis for the southbound. The AMB is expected to log the information when it is asked to go through calibration. The register is always cleared when entering the calibration state. This register is effectively 'Read Only' as the data written in current cycle is overwritten in the next cycle. This register will be used for debug purposes.

Device: NodeID Function: 1 Offset: 7Eh			
Bit	**Attr**	**Default**	**Description**
15:14	RV	0h	**Reserved**
13:0	RWST	0h	**CALSTATUS: Calibration status** 0 - Pass 1- Fail

12 FB-DIMM SPD Programming Clarification and Recommendation

DRAM RELATED BYTES

Byte 17: Write Latency Supported

Per JEDEC SPD Spec 1.1 defined values are

Bit [7:4]	Bit [3:0]
WL Range (total number of values)	WL Minimum (clocks)
0001=1	0010=2
0010=2	All other values TBD
0011=3	
0100=4	
0101 = 5	
0110 = 6	
0111 = 7	
1000 = 8	
1001 = 9	
All other values TBD	

Notes:
1. The upper four bits describe the range, defined as total number of values supported. Note that DDR2 SDRAM spec specifies WL=RL-1=AL+CL-1.
2. The Blackford BIOS ignores this byte, so it would not affect launch.

Byte 18: Additive Latency Supported

Per JEDEC SPD Spec 1.1 defined values are

Bit [7:4]	Bit [3:0]
AL Range (total number of values)	AL Minimum (clocks)
0001=1	0000=0
0010=2	All other values TBD
0011=3	
0100=4	
0101 = 5	
0110 = 6	
All other values TBD	

Notes:
1. The upper four bits describe the range, defined as total number of values supported.
2. The Blackford BIOS ignores this byte, so it would not affect launch. For example, Blackford chipset sets to AL = 3 where CL=4, and AL=4 where CL=5.

FBDIMM SPD BYTE ADDITIONS

Byte 79: FBD ODT Termination

This Byte specifies the optimal values for the FBD ODT. ODT values defined here must be subset of the ODT defined in Byte 30 which is part of generic DRAM spec and describes ODT supported by DRAM.
If both ODT ranks are disabled (Byte 79 = 0x00), the BIOS should use SPD Byte 7 to lookup the recommended ODT values according to the FB-DIMM Design specification. Note that the ODT values may not be optimal, and some designs may not be distinguishable from others.

Bit [7:6]	Bit [5:4]	Bit [3:2]	Bit [1:0]
Reserved	**Rank 1 ODT**	**Reserved**	**Rank 0 ODT**
00	00 = Disabled	00	00 = Disabled
00	01 = 75 Ohm	00	01 = 75 Ohm
00	10 = 150 Ohm	00	10 = 150 Ohm
00	11 = 50 Ohm	00	11 = 50 Ohm

Intel recommends using the values shown below:

Raw Card	SPD values (hex) for 533/667MHz	SPD values (hex) for 800MHz
A, C	01h	01h
B, E, H	22h	21h
D, J	12h	30h

AMB-DRAM Thermal Resistance Bytes

These bytes are required for correct system operation (thermal throttling). The contents of these bytes should be programmed to 00h (per current Intel platform usage model, the maximum thermal resistance values specified in Section 7.6 will be used). Refer to section 7.7 for details.

Byte 94: R(AMB) Ratio of AMB temp. change from ambient, divided by AMB total power change; DRAM power constant.

Byte 95: R(AMB-DRAM) Ratio of hottest DRAM temp. change from ambient, divided by AMB total power change; DRAM power constant.

Byte 96: R(DRAM) Ratio of hottest DRAM temp. change from ambient, divided by total DRAM power change; AMB power constant.

Byte 97: R(DRAM-AMB) Ratio of AMB temp. change from ambient, divided by total DRAM power change; AMB power constant.

Intel recommends using the values shown below:

SPD byte number	Value (in HEX)
Byte 94	00h
Byte 95	00h
Byte 96	00h
Byte 97	00h

Byte 98: AMB maximum junction temperature (Tj max)

Bit [4:0]=Tjmax [°C], Bit [7:5]=Reserved. Individual AMB Datasheet documents contain TjMAX value for each AMB part.

Intel recommends using the values shown below:

TjMAX Value (in degrees C)	Bit [7:5]	Bit [4:0]	SPD Values (hex)
110	00	00000	00h
95	00	00001	01h
96	00	00010	02h
97	00	00011	03h
98	00	00100	04h
99	00	00101	05h
100	00	00110	06h
101	00	00111	07h
102	00	01000	08h
103	00	01001	09h
104	00	01010	0Ah
105	00	01011	0Bh
106	00	01100	0Ch
107	00	01101	0Dh
108	00	01110	0Eh
109	00	01111	0Fh
110	00	10000	10h
111	00	10001	11h
112	00	10010	12h
113	00	10011	13h
114	00	10100	14h
115	00	10101	15h
116	00	10110	16h
117	00	10111	17h
118	00	11000	18h
119	00	11001	19h
120	00	11010	1Ah
121	00	11011	1Bh
122	00	11100	1Ch
123	00	11101	1Dh
124	00	11110	1Eh
125(or more)	00	11111	1Fh

Byte 99: Air Flow Impedance and FB-DIMM Category

This byte describes following:
Air Flow Impedance - Bit [7:6]
FBDIMM Category: DRAM Type – Bit [5:3]; Heat Spreader Type – Bit [2:0]

Air Flow Impedance		FBDIMM Category			
Air Flow	Bit [7:6]	DRAM type	Bit [5:3]	HS Type	Bit [2:0]
Unknown	00	Unknown	000	Unknown	000
Type 1	01	Planar	001	AMB only	001
Type 2	10	Dual Die	010	Full DIMM	010
Type 3	11	Stacked	011	Reserved	011 to 111
		Reserved	100 to 111		

Note:
1. Refer to section 7.2 for DRAM and HS type definition

Intel recommends using the values shown below:

Raw Card	DRAM Type	Heat Spreader Type	Byte 99 Bits [5:0]	SPD value (hex), if Air Flow impedance is unknown	SPD value (hex), if Air Flow impedance is Type 1	SPD value (hex), if Air Flow impedance is Type 2	SPD value (hex), if Air Flow impedance is Type 3
A	Planar	AMB Only	001001	09h	49h	89h	c9h
A	Planar	Full Dimm	001010	0ah	4ah	8ah	cah
B	Planar	AMB Only	001001	09h	49h	89h	c9h
B	Planar	Full Dimm	001010	0ah	4ah	8ah	cah
C	Planar	AMB Only	001001	09h	49h	89h	c9h
C	Planar	Full Dimm	001010	0ah	4ah	8ah	cah
D/J	Stacked	AMB Only	011001	19h	59h	99h	d9h
D/J	Stacked	Full Dimm	011010	1ah	5ah	9ah	dah
D/J	Dual die	AMB Only	010001	11h	51h	91h	d1h
D/J	Dual die	Full Dimm	010010	12h	52h	92h	d2h
E/H	Planar	AMB Only	001001	09h	49h	89h	c9h
E/H	Planar	Full Dimm	001010	0ah	4ah	8ah	cah

13 OVERTEMP Function of the AMB

The intention of the over temperature feature of the AMB is to protect the AMB and possibly the DRAMs from failure should all other thermal control mechanisms be ineffective or not functioning. It is meant to be the last level of defense to avoid hardware damage and therefore is catastrophic in nature. The over temperature condition is expected to be temporary so as not to damage the long term reliability of the silicon.

The response of the AMB to an overtemp condition is intended to immediately reduce power as much as possible. During an over temperature shutdown the SMBus is not accessible; the SMBus will be accessible on the AMB after it cools back down below Tjmax. A hardware RESET must be issued to the AMB to exit the overtemp condition prior to retraining. The hardware reset will reset all status bits in the AMB, requiring any status information to be read via the SMBus prior to the hardware reset.

There are two major functions that the AMB can do based on the temperature going above the TEMPHI setting:

Set the OVERTEMP bit in the FERR/NERR registers.
Shut Down the AMB.

Each of these can be enabled or disabled.

The AMB spec text is as follows:

If OVERTEMP error type enabled in EMASK Register
1. The OVERTEMP bit will be set in the FERR or NERR register as appropriate
2. Error/Alert Asserted bit set in FBD Status 0 register
If TEMPHIENABLE set in TEMPSTAT register also
3. Shut down DDR channel:
Drive CKE low to the DRAMs and float the command, address, and data signals. CKE, ODT, and clock continue to be driven. The clocks to the DRAMS may be stopped after the CKE has been registered low
4. The FBD interface goes to electrical idle, with the receivers shut off to reduce power.
5. The core will continue to be clocked, and the Advanced Memory Buffer will respond to SMBus commands. This allows the host controller to determine the error condition

NOTE: No recovery expected, just trying to prevent Si meltdown
The AMB will remain in this state until the temperature is below
TEMPHI and the OVERTEMP bit is reset via SMBus or a hardware reset.
Else ignore error

NOTE: A hardware reset will place the TEMPHIENABLE bit in its default state of disabled.

NOTE: To acknowledge and record an overtemperature event, the AMB should be allowed to cool below its Tcase_max specification before accessing its SMBus registers.

Overtemp bit in the FERR/NERR registers

This simply sets a bit in the register which can be read later. It does NOT send alert frames northbound. This would normally be used with the Shutdown of the AMB, allowing the BIOS to later come back and see which AMB caused the problem. Th access would be through SMBus.

Shutting down the AMB

When shutting down the AMB there is no attempt to close pages or put the DRAMs in self refresh mode. CKE is taken low to the DRAMs which put them in a low power state. The command/address/control signals are floated, which reduces power on the AMB. DRAM data will be lost due to lack of refresh.

The high speed link is taken to Electrical Idle, as that is the lowest power mode for the AMB.

Following an AMB shut down, data integrity is compromised and no specific operation is guaranteed. A fast reset will not restore the system to an operating mode, as the over temperature AMB will cause the channel to fail training. Failure mechanisms may appear as CRC and/or ECC errors. In some cases, especially when running in single channel mode with multiple DIMMs (not a recommended configuration), data may appear with correct CRC and ECC. It is a persistent error, so there are likely major consequences such as a system crash that will soon follow.