Leading at the edge of Moore’s Law with Intel Custom Foundry

Sunit Rikhi
General Manager, Intel Custom Foundry
Vice President, Technology and Manufacturing Group

SPCS011
Agenda

• Overview

• Platform Offerings

• Summary
Intel Custom Foundry: Flexible Business Models
Intel Custom Foundry: Flexible Business Models

Customer Design + Intel and Third Party IP = Custom Product
Intel Custom Foundry: Flexible Business Models

Customer Design + Intel and Third Party IP = Custom Product

Intel Standard Product Design + Customer and Third Party IP = Semi-Custom Product
Delivering value beyond a traditional foundry model
Intel Custom Foundry: Flexible Execution Models

Delivering value beyond a traditional foundry model

Customer Owned Tooling (COT)
Intel Custom Foundry: Flexible Execution Models

Delivering value beyond a traditional foundry model
Business & Execution Models Matrix

- **Custom Product**
  - Customer Owned Tooling
  - Full Service (ASIC Model)

- **Semi-Custom Product**
  - Customer Owned Tooling
  - Full Service (ASIC Model)
## Intel Custom Foundry: Design Ecosystem

### Design Services

| Intel | Cadence | Open-Silicon | SMARTplay | Synopsys | Wipro |

### Soft IP

| Intel | Cadence | Northwest Logic | Synopsys |

### Advanced IP

| Intel | Cadence | Synopsys |

### Foundation IP

| Intel | Synopsys |

### Design Tools & Flows

| Intel | ANSYS | Cadence | Mentor Graphics | Synopsys |

### Note:

Logos in alphabetical order.
Intel Custom Foundry: Worldwide Assets
Intel Custom Foundry: Worldwide Assets

- Oregon
- Ireland
- Arizona
- New Mexico
- Dalian
- Israel
- Wafer Fabs
Intel Custom Foundry: Worldwide Assets

- California
- Oregon
- Arizona
- New Mexico
- Costa Rica
- Idaho
- Ireland
- Toronto
- Israel
- Canada
- Bangalore
- Thailand
- Vietnam
- Dalian
- Chengdu
- Penang
- Kulim

Legend:
- Wafer Fabs
- Assembly/Test
- Foundry Platform Dev & Support
Intel Custom Foundry: Announced Customers

Note: This list of customers does not include those who choose not to disclose relationship with Intel Custom Foundry. Logos are in alphabetical order.
Agenda

• Overview

• Platform Offerings

• Summary
Intel Custom Foundry Platform Offerings
Intel Custom Foundry Platform Offerings
Intel Custom Foundry Platform Offerings

- Design Platform
- Kits
- IP
- Design Services

- Technology Platform
- Silicon
- Package
- Test
Intel Custom Foundry Platform Offerings

- **Manufacturing Platform**
- **Design Platform**
- **Technology Platform**

<table>
<thead>
<tr>
<th>Manufacturing Platform</th>
<th>Engineering Services</th>
<th>Production Services</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Design Platform</strong></td>
<td>Kits</td>
<td>IP</td>
</tr>
<tr>
<td><strong>Technology Platform</strong></td>
<td>Silicon</td>
<td>Package</td>
</tr>
</tbody>
</table>
Intel Custom Foundry Platform Offerings

- **Online Service Platform**: Information Exchange, Service Transactions
- **Manufacturing Platform**: Engineering Services, Production Services
- **Design Platform**: Kits, IP, Design Services
- **Technology Platform**: Silicon, Package, Test
Intel Custom Foundry Platform Offerings

Online Service Platform
- Information Exchange
- Service Transactions

Manufacturing Platform
- Engineering Services
- Production Services

Design Platform
- Kits
- IP
- Design Services

Technology Platform
- Silicon
- Package
- Test
The Wide Moving Edge of Moore's Law

Delivering performance/watt improvement to a wide range of products

Lower Leakage Power

Higher Transistor Performance (switching speed)

Server Computing

Client Computing

Mobile Computing

Mobile Always-On Circuits

65 nm 45 nm 32 nm 22 nm 14 nm
# Intel Custom Foundry: Silicon Technology Platform Offerings

<table>
<thead>
<tr>
<th>Cloud/Infrastructure</th>
<th>22nm</th>
<th>14nm</th>
<th>10nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>General Purpose</td>
<td>✔</td>
<td>✔</td>
<td></td>
</tr>
<tr>
<td>Low Power</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Client/Consumer</th>
<th>General Purpose</th>
<th>Low Power</th>
<th>In Dev</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>✔</td>
<td>✔</td>
<td></td>
</tr>
</tbody>
</table>
SOC Features in 14nm technology

- High Q Inductors
- High Density MIMCAP
- Precision Resistors
- RF Transistors
- Low Leakage, Long L Transistors
- High Voltage I/O Transistors

Full featured technology enables integration of system functions on a chip
Cost per Transistor

Intel 14 nm continues to deliver lower cost per transistor
Confident Pursuit

Future Technology Options

Expect More From Moore

Future options subject to change

Source: Intel
Intel Custom Foundry Platform Offerings

**Online Service Platform**
- Information Exchange
- Service Transactions

**Manufacturing Platform**
- Engineering Services
- Production Services

**Design Platform**
- Kits
- IP
- Design Services

**Technology Platform**
- Silicon
- Package
- Test
Intels Flip Chip Package Portfolio

- Cloud/Infrastructure
- Client
- SOC/Consumer

- Package-on-Package
- Ultra-thin
- Small Form Factor Chip Scale Packages

Serving the requirements of multiple market segments
Intel’s Flip Chip Package Portfolio

Cloud/Infrastructure

• Thin Core Substrate
• Multi-chip packages
• Embedded and surface passives

Client

• Enhanced thermal solutions
• LGA socket

Desktop

Mobile

Serving the requirements of multiple market segments
Intel’s Flip Chip Package Portfolio

<table>
<thead>
<tr>
<th>Cloud/Infrastructure</th>
<th>Server</th>
<th>HPC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>• High pin count LGA sockets</td>
<td>• Very High pin count LGA sockets</td>
</tr>
<tr>
<td></td>
<td>• Optimized for high speed signaling</td>
<td>• Very large footprint BGA</td>
</tr>
<tr>
<td></td>
<td>• Large die</td>
<td>• Reticle size die assembly</td>
</tr>
</tbody>
</table>

Serving the requirements of multiple market segments
Introducing: Embedded Multi-die Interconnect Bridge (EMIB)

An elegant approach to in-package high density interconnect of heterogeneous die
### EMIB Wafer Process Compared to Typical 2.5D

#### Typical 2.5D Interposer Process

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Starting Wafer</td>
<td></td>
</tr>
<tr>
<td>TSV Formation &amp; Fill</td>
<td></td>
</tr>
<tr>
<td>BEOL Metallization</td>
<td></td>
</tr>
<tr>
<td>Wafer Thinning</td>
<td></td>
</tr>
<tr>
<td>TSV Reveal &amp; Backside Surface</td>
<td></td>
</tr>
</tbody>
</table>

#### EMIB Bridge Wafer Process

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Starting Wafer</td>
<td></td>
</tr>
<tr>
<td>Not Required!</td>
<td></td>
</tr>
<tr>
<td>Not Required!</td>
<td></td>
</tr>
</tbody>
</table>

*EMIB wafer fabrication is simpler than typical silicon interposer*
EMIB Assembly Process Compared to Typical 2.5D

**Typical 2.5D Interposer Process Flow**

Die 2  Die 1  Die 3

Assembly A

Assembly B

**EMIB Process Flow**

Die 2  Die 1  Die 3

Assembly

**EMIB Requires Less Assembly Processing Than typical Silicon Interposer Assembly**
EMIB Assembly Process Compared to Typical 2.5D

Typical 2.5D Interposer Process Flow

EMIB Process Flow

EMIB Requires Less Assembly Processing Than typical Silicon Interposer Assembly
EMIB Assembly Process Compared to Typical 2.5D

Typical 2.5D Interposer Process Flow

EMIB Process Flow

EMIB Requires Less Assembly Processing Than typical Silicon Interposer Assembly
EMIB Progress

EMIB Package (Cross Section)

Available for sampling in 2015
Intel Custom Foundry Platform Offerings

- **Online Service Platform**
  - Information Exchange
  - Service Transactions

- **Manufacturing Platform**
  - Engineering Services
  - Production Services

- **Design Platform**
  - Kits
  - IP
  - Design Services

- **Technology Platform**
  - Silicon
  - Package
  - Test
Introducing High Density Modular Test (HDMT)

- **Common Architecture**
  - Fast TTM Engineering Module
  - >30 sites with parallel, asynchronous operation in production module

- **Flexible Architecture**
  - Enables standard instrumentation integration (PXI)

- **Low Cost**
  - > 2X Cost improvement over conventional test platforms
Intel Custom Foundry Platform Offerings

- **Online Service Platform**
  - Information Exchange
  - Service Transactions

- **Manufacturing Platform**
  - Engineering Services
  - Production Services

- **Design Platform**
  - Kits
  - IP
  - Design Services

- **Technology Platform**
  - Silicon
  - Package
  - Test
Foundry Design Kit (FDK)

Analog / Mixed Signal Flows

Digital Flows

Primitive Libraries

Process Collaterals

Design Tool Drivers: Technology files

DFM Templates: Device, Layout, Fill

Design Rules: Run-sets LVS$^1$, DRC$^2$, RV$^3$

Models: Simulation and RC$^4$ Extraction
Foundry Design Kit (FDK)

- Analog / Mixed Signal Flows
- Digital Flows
- Primitive Libraries
- Process Collaterals

- Full Chip Integration Collateral Library
- Memory (SRAM\(^1\)) Cell Library
- Analog Primitive Library\(^2\)

1 Static Random Access Memory
2 Capacitors, resistors, inductors, etc.
Foundry Design Kit (FDK)

- Analog / Mixed Signal Flows
- Digital Flows
- Primitive Libraries
- Process Collaterals

Logic Synthesis
Floor Planning / Place & Route
Design for Test / Test Pattern Generation
Timing and Noise Analysis
Physical Verification
Reliability Verification: EM$^1$/SH$^2$/IR$^3$ Drop
RC$^4$ Extraction
Design for Manufacturing: Fill
Foundry Design Kit (FDK)

**Analog / Mixed Signal Flows**

- Schematic Capture
- Circuit Simulation
- Custom Routing
- Custom Layout
- Physical Verification
- Reliability Verification: EM$^1$/SH$^2$/IR$^3$ Drop
- RC$^4$ Extraction
- Design for Manufacturing: Fill

**Digital Flows**

**Libraries**

**Process Collaterals**

1. Electro-migration
2. Self Heat
3. Voltage (Multiplication of current and resistance) drop
4. Resistance $\times$ Capacitance
## FDK: Digital Flows

### Breadth of Industry Standard Tools

<table>
<thead>
<tr>
<th>Tool</th>
<th>Synopsys</th>
<th>Cadence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Synthesis</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Floor Planning / Place &amp; Route</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Test Pattern Generation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timing and Noise Analysis</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Physical Verification</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reliability Verification</td>
<td></td>
<td>ANSYS</td>
</tr>
<tr>
<td>RC¹ Extraction</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Design for Manufacturing: Fill</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Resistance * Capacitance
## FDK: Analog Mixed Signal Flows
### Breadth of Industry Standard Tools

<table>
<thead>
<tr>
<th>Feature</th>
<th>Synopsys</th>
<th>Cadence</th>
<th>Mentor Graphics</th>
<th>ANSYS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Schematic Capture</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Circuit Simulation</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Custom Routing</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Custom Layout</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Physical Verification</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reliability Verification</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RC¹ Extraction</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Design for Manufacturing: Fill</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Resistance \* Capacitance
Intel Custom Foundry Platform Offerings

**Online Service Platform**
- Information Exchange
- Service Transactions

**Manufacturing Platform**
- Engineering Services
- Production Services

**Design Platform**
- Kits
- IP
- Design Services

**Technology Platform**
- Silicon
- Package
- Test
IP Offerings: Foundational IP

- Processor IP
- Interface IP
- Advanced Mixed Signal IP
- Foundational IP

- High Speed Lib
- High Density Lib

- Foundational Digital Libraries
- Foundational Memory

- Register File Compilers
- SRAM Compilers
- TCAMs Compilers
- ROMs
- Fuses (High density/High Speed)
IP Offerings: Advanced Mixed Signal IP

- Phase Locked Loop/Delay Locked Loop
- Low Drop Out voltage Regulator
- Crystal Oscillator
- Adaptive Voltage Scaling circuits
- Clock Receiver & Divider
- Digital Thermal Sensor
- General Purpose IO
- High Speed Programmable IO
- Voltage Reference IO
- Digital Random Number Generators
### IP Offerings: Interface IP

<table>
<thead>
<tr>
<th>Processor IP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interface IP</td>
</tr>
<tr>
<td>Memory</td>
</tr>
<tr>
<td>SerDes</td>
</tr>
<tr>
<td>Storage</td>
</tr>
<tr>
<td>Display</td>
</tr>
</tbody>
</table>

**Interface IP**
- DDR2/3
- DDR4
- LPDDR3/4
- HBM
- WIO

**Memory**
- USB2/3
- PCI Express
- Ethernet

**SerDes**
- MIPI (DPHY, HSI)
- LP 1-12.5G
- CEI/IEEE 25-32G
- CEI/IEEE 40-56G

**Storage**
- eMMC4/5
- SD3.0

**Display**
- eDP/DP
- HDMI1.4/2.0

---

1. Roadmap item under consideration
2. KR, XAUI, CEI.
3. Multi Standard
IP Offerings: Processor IP

Processor IP

Intel® Architecture Cores

Intel® Atom™ processor

Interface IP

Advanced Mixed Signal IP

Foundational IP

1 Roadmap item in planning and development
Intel Custom Foundry Platform Offerings

- **Online Service Platform**: Information Exchange, Service Transactions
- **Manufacturing Platform**: Engineering Services, Production Services
- **Design Platform**: Kits, IP, Design Services
- **Technology Platform**: Silicon, Package, Test
ASIC Design Enablement & Services

- Prototyping Shuttle
- Support
- Design Implementation

Block Level physical implementation for COT business model
Full Chip physical implementation for ASIC business model
ASIC Design Enablement & Services

Prototyping Shuttle

Support

Design Implementation

Customer bring-up / Training
Optimized reference methodology and flows
Common debug environment
ASIC Design Enablement & Services

Prototyping Shuttle

Support

Design Implementation

From GDS to Prototype units

22nm  14nm  10nm

Coming Soon
Intel Custom Foundry Platform Offerings

- **Technology Platform**
  - Silicon
  - Package
  - Test

- **Design Platform**
  - Kits
  - IP
  - Design Services

- **Manufacturing Platform**
  - Engineering Services
  - Production Services

- **Online Service Platform**
  - Information Exchange
  - Service Transactions
Engineering Services

One-stop comprehensive engineering services

- Package Design Service
- Wafer and Final Test Service
- Failure Analysis & Debug Service
- Product Qualification Service
- Engineering Samples

- Leading edge technology capabilities
- Integrated engineering data network

Faster Time to Production Ramp
Example:
Post Silicon Debug – Fabless Industry Model

Failure detection, Analysis and Resolution

Customer
Example:
Post Silicon Debug with Intel Custom Foundry

Integrated Engineering Data Network

One-stop Engineering Services

Customer
Intel Custom Foundry Platform Offerings

- Online Service Platform: Information Exchange, Service Transactions
- Manufacturing Platform: Engineering Services, Production Services
- Design Platform: Kits, IP, Design Services
- Technology Platform: Silicon, Package, Test
Production Services

Integrated Supply Chain

- Manufacturing scale and business continuity
- Integrated quality management
- Yield optimization
Intel Custom Foundry Platform Offerings

- **Online Service Platform**: Information Exchange, Service Transactions
- **Manufacturing Platform**: Engineering Services, Production Services
- **Design Platform**: Kits, IP, Design Services
- **Technology Platform**: Silicon, Package, Test
Online Services Platform

Customers 🔄 Ecosystem Partners

Online Services Portal

Information Exchange
- Design kits/IP exchange
- Documentation access
- Design data upload
- Mfg data download
- Collaborative Meetings

Service Transactions
- Tapeout services
- Shuttle services
- Material tracking & control
- Issue resolution
- Ad hoc online support
Agenda

• Overview

• Platform Offerings

• Summary
Summary

• Intel Custom Foundry is open for business. We support a full range of flexible custom and semi-custom service business models.
Summary

• Intel Custom Foundry is open for business. We support a full range of flexible custom and semi-custom service business models.
• Our customers have access to co-optimized advanced manufacturing technologies including silicon, packaging and test.
Summary

• Intel Custom Foundry is open for business. We support a full range of flexible custom and semi-custom service business models.

• Our customers have access to co-optimized advanced manufacturing technologies including silicon, packaging and test.

• To enable customer designs, our design platform offers industry standard kits, silicon proven IP blocks and design services for low power SOCs to high performance infrastructure devices.
Summary

- Intel Custom Foundry is open for business. We support a full range of flexible custom and semi-custom service business models.
- Our customers have access to co-optimized advanced manufacturing technologies including silicon, packaging and test.
- To enable customer designs, our design platform offers industry standard kits, silicon proven IP blocks and design services for low power SOCs to high performance infrastructure devices.
- Our manufacturing platform offers highly optimized silicon engineering and production services that take full advantage of Intel’s Integrated Device Manufacturing (IDM) capabilities.
Come lead with us at the edge of Moore’s Law
Additional Sources of Information

• A PDF of this presentation is available from our Technical Session Catalog: www.intel.com/idfsessionsSF. This URL is also printed on the top of Session Agenda Pages in the Pocket Guide.

• Sunit Rikhi’s presentation at Intel Analyst Event in London (May 2013):

• Recent Press Release
  - VLSI video interview:
    ▪ http://electronics.wesrch.com/wequest-EL1QIXV-intel-custom-foundry
  - EMIB/HDMT announcement:
  - Panasonic announcement:
  - Altera and Intel Extend Manufacturing Partnership to Include Development of Multi-Die Devices:
Legal Disclaimer

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL PRODUCTS AND/OR SERVICES. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN AN EXECUTED AGREEMENT, INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS AND SERVICES INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS OTHERWISE AGREED IN A SIGNED WRITING BY INTEL, THE INTEL PRODUCTS AND SERVICES ARE NOT DESIGNED NOR INTENDED FOR ANY APPLICATION IN WHICH THE FAILURE OF THE INTEL PRODUCT COULD CREATE A SITUATION WHERE PERSONAL INJURY OR DEATH MAY OCCUR.

Intel may make changes to specifications and product /process descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products and services described in this document may contain defects or errors known as errata which may cause deviations from published specifications. Current characterized errata are available on request.

Intel, Atom, Look Inside and the Intel logo are trademarks of Intel Corporation in the United States and other countries.

* Other names and brands may be claimed as the property of others.

Copyright ©2014 Intel Corporation.
Risk Factors

The above statements and any others in this document that refer to plans and expectations for the second quarter, the year and the future are forward-looking statements that involve a number of risks and uncertainties. Words such as “anticipates,” “expects,” “intends,” “plans,” “believes,” “seeks,” “estimates,” “may,” “will,” “should” and their variations identify forward-looking statements. Statements that refer to or are based on projections, uncertain events or assumptions also identify forward-looking statements. Many factors could affect Intel's actual results, and variances from Intel's current expectations regarding such factors could cause actual results to differ materially from those expressed in these forward-looking statements. Intel presently considers the following to be important factors that could cause actual results to differ materially from the company's expectations. Demand for Intel's products is highly variable and, in recent years, Intel has experienced declining orders in the traditional PC market segment. Demand could be different from Intel's expectations due to factors including changes in business and economic conditions; consumer confidence or income levels; customer acceptance of Intel's and competitors' products; competitive and pricing pressures, including actions taken by competitors; supply constraints and other disruptions affecting customers; changes in customer order patterns including order cancellations; and changes in the level of inventory at customers. Intel operates in highly competitive industries and its operations have high costs that are either fixed or difficult to reduce in the short term. Intel's gross margin percentage could vary significantly from expectations based on capacity utilization; variations in inventory valuation, including variations related to the timing of qualifying products for sale; changes in revenue levels; segment product mix; the timing and execution of the manufacturing ramp and associated costs; excess or obsolete inventory; changes in unit costs; defects or disruptions in the supply of materials or resources; and product manufacturing quality/yields. Variations in gross margin may also be caused by the timing of Intel product introductions and related expenses, including marketing expenses, and Intel's ability to respond quickly to technological developments and to introduce new products or incorporate new features into existing products, which may result in restructuring and asset impairment charges. Intel's results could be affected by adverse economic, social, political and physical/infrastructure conditions in countries where Intel, its customers or its suppliers operate, including military conflict and other security risks, natural disasters, infrastructure disruptions, health concerns and fluctuations in currency exchange rates. Intel's results could be affected by the timing of closing of acquisitions, divestitures and other significant transactions. Intel's results could be affected by adverse effects associated with product defects and errata (deviations from published specifications), and by litigation or regulatory matters involving intellectual property, stockholder, consumer, antitrust, disclosure and other issues, such as the litigation and regulatory matters described in Intel's SEC filings. An unfavorable ruling could include monetary damages or an injunction prohibiting Intel from manufacturing or selling one or more products, precluding particular business practices, impacting Intel's ability to design its products, or requiring other remedies such as compulsory licensing of intellectual property. A detailed discussion of these and other factors that could affect Intel's results is included in Intel's SEC filings, including the company's most recent reports on Form 10-Q, Form 10-K and earnings release.