International Packaging Specifications 11

11.1 Electronic Industries Association of Japan (EIAJ)

EIAJ publishes the following rules and standards as they apply to the preparation of outline drawings of integrated circuits.

Number	Nomenclature
ED -7300	Recommended practice on standard for the preparation of outline drawings of semiconductor packages
ED -7301	Manual or the standard of integrated circuits package
ED -7302	Manual for integrated circuits package design guideline
ED -7303	Name and code for integrated circuits package
ED -7304	Measuring method for package dimensions of ball grid array (BGA)
ED -7304-1	Measuring method for package dimensions of Small Outline Package (SOP)
ED -7304-2	Measuring method for package dimensions of Small Outline J-leaded package (SOJ)
ED -7305	Unit design guide for the preparation of package outline drawing of integrated circuits (gullwing-lead)
ED -7311	Standards of integrated circuits package
ED -7311-1	Standard of integrated circuits package [TSOP(1)]
ED -7311-2	Standard of integrated circuits package [TSOP(2)]
ED -7311-3	Standard of integrated circuits package [Tape Ball Grid Array 1.0mm pitch (T-BGA)]
ED -7311-4	Standard of integrated circuits package [Tape Ball Grid Array 1.27mm pitch (T-BGA)]
ED -7311-5	Standard of integrated circuits package [32/48 pins Fine-pitch Ball Grid Array (FBGA)]
ED -7311-6	Standard of integrated circuits package [60/90 pins Fine-pitch Ball Grid Array (FBGA)]
ED -7311-7	Standard of integrated circuits package [Plastic Fine pitch Ball Grid Array (P-FBGA)]
ED -7311-8	Standard of integrated circuits package [Plastic Fine pitch Ball Grid Array 0.8mm pitch (P-FBGA)]
ED -7311-9A	Standard of integrated circuits package [P-BGA (Cavity up type)]
ED -7311-10A	Standard of integrated circuits package [P-BGA (Cavity down type)]
ED -7311-11A	Standard of integrated circuits package (119/153 pins P-BGA)
ED -7311-12	Standard of integrated circuits package (52 pins 64 pins 80 pins and 100 pins low-profile quad flat package with exposed heatsink)
ED -7400	Standards for the dimensions of semiconductor devices (integrated circuits)
ED -7400-1	Standards for the dimensions of semiconductor devices (integrated circuits)
ED -7400-2	Standards for the dimensions of semiconductor devices (integrated circuits)
ED -7401-4	Method of measuring semiconductor device package dimensions (integrated circuits)
ED -7405	General rules for the preparation of outline drawings of integrated circuits zigzag in-line packages (ZIP)
ED -7405-1	General rules for the preparation of outline drawings of integrated circuits shrink zigzag in-line packages (SZIP)

ED -7406A	General rules for the preparation of outline drawings of integrated circuits small outline J-lead packages (SOJ)
ED -7408A	General rules for the preparation of outline drawings of integrated circuits pin grid array packages (PGA)
ED -7414	General rules for the preparation of outline drawings of integrated circuits guarding quad flat packages (GQFP)
ED -7415	General rules for the preparation of outline drawings of integrated circuits small outline packages with heat sink (HSOP)
ED -7417	General rules for the preparation of outline drawings of integrated circuits bumpered quad flat packages (BQFP)
ED -7418	General rules for the preparation of outline drawings of integrated circuits glass sealed quad flat packages (QFP-G)
ED -7419	General rules for the preparation of outline drawings of integrated circuits glass sealed dual in-line packages (DIP-G)
ED -7421	General rules for the preparation of outline drawings pf integrated circuits ceramic dual in-line packages (DIP-C)
ED -7422	General rules for the preparation of outline drawings of integrated circuits glass sealed quad flat J-leaded packages (QFJ-G)
ED -7423	General rules for the preparation of outline drawings of integrated circuits ceramic quad flat J-leaded packages (QFJ-C)
ED -7431-1A	Recommended outline drawings for carriers quad tape carrier packages (QTP carrier)
ED -7431A	General rules for the preparation of outline drawings of integrated circuits quad tape carrier packages (QTP)
ED -7432	General rules for the preparation of outline drawings of integrated circuits dual tape carrier packages (type1) (DTP(1))
ED -7433	General rules for the preparation of outline drawings of integrated circuits dual tape carrier packages (type 2)
ED -7441B	Standard for the package of universal memory devices
ED -7500A	Standards for the dimensions of semiconductor devices (discrete semiconductor devices)
EDR-7311	Design guideline of integrated circuits for quad Flat package (QFP)
EDR-7312	Design guideline of integrated circuits for thin small outline package (type1)
EDR-7313	Design guideline of integrated circuits for thin small outline package (type 2) (TSOP2)
EDR-7314	Design guideline of integrated circuits for shrink small outline package (SSOP)
EDR-7315A	Design guideline of integrated circuits for ball grid array (BGA)
EDR-7316	Design guideline of integrated circuits for Fine-pitch Ball Grid Array and Fine-pitch Land Grid Array (FBGA/ FLGA)
EDR-7317	Design guideline of integrated circuits for Surface Vertical Package (SVP)
EDR-7318	Design guideline of integrated circuits for plastic very thin small outline non-lead package (P-VSON)
EDR-7319	Design guideline of integrated circuits for quad flat J-lead packages (QFJ)
EDR-7320	Design guideline of integrated circuits for small outline package (SOP)
EDR-7601	Guidance of embossed carrier taping for integrated circuits

11.2 Joint Electron Device Engineering Council (JEDEC)

JEDEC Publication 95 lists all package outlines. More information about JEDEC can be located on their web site at http://www.jedec.org.

11.3 Mil Standards

The following military standards include specifications required to meet U. S. Military requirements.

- **MIL-M-38510** General Specifications for Microcircuits
- **MIL-STD-883** Test Methods/Procedures for Microelectronics

11.4 Semiconductor Equipment and Materials Institute, Inc.

For a list of SEMI standards, reference the *Book of SEMI Standards*, 1990, Vol.4, Packaging Division, 605 E. Middlefield Road, Mountain View, CA 94043, U.S.A. Phone:(415) 964-5111. FAX: (415) 967-5375. TELEX: 856-777 SEMI-MNTV

11.5 Interconnecting and Packaging Electronic Circuits (IPC) Standards

Number	Nomenclature
ANSI/IPC-S-815B	General requirements for soldering electronic connections
ANSI/IPC-SM-780	Component packaging and inter-connecting, with emphasis on surface mounting
ANSI/IPC-SM-782	Surface mount land patterns
ANSI/IPC-SM-786	Impact of moisture on plastic I/C package cracking
For a list of additional IPC standards, contact: IPC, 7380 N. Lincoln Ave., Lincolnwood, Illinois, 60646. Phone: (708) 677-2850.	