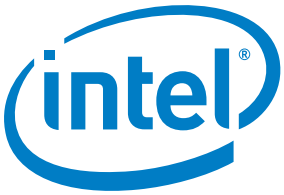


6th Generation Intel® Processor and Intel® 100 Series Chipset Family Platform Controller Hub (PCH) - Intel® Xeon® Processor E3-1515M v5 and Intel® GL82CM236 Platform Controller Hub (PCH) Evaluation Kit

User Guide

April 2016

Revision 001

Document Number: 334217-001US

Contents

Figures

April 2016
Document Number: 334217-001US

Tables

Revision History

Date	Revision	Description
April 2016	001	Initial release.

§

1.0 Introduction

This User Guide describes the typical hardware set-up procedures, features, and use of the Intel® Xeon® Processor E3-1515M v5 and Intel® GL82CM236 Platform Controller Hub (PCH) Evaluation Kit Customer Reference Board (CRB). Throughout this document, Intel Xeon Processor E3-1515M v5 and Intel GL82CM236 PCH Evaluation Kit may be referred to simply as "CRB." This document should be read in its entirety prior to powering ON the CRB.

Section 4.0 Quick Start Guide provides quick start procedures for reference. It is recommended to have both the schematic and CRB present as you proceed through this document.

The CRB is a dual channel DDR4 mobility platform. It's designed to support the 6th Generation Intel® Core™ i7 Processor Ball Grid Array (BGA) and the Intel® 100 Series and Intel® 230 Series Chipset Family.

This document is only relevant to the Intel Xeon Processor E3-1515M v5 and Intel GL82CM236 PCH Evaluation Kit CRB. The references in this document correlate to reference designators and board properties of the CRB. Socket and connector locations are labeled with a letter-number combination (for example, the first memory SODIMM connector is located at DIMM1). Refer to the silkscreen labeling on the CRB for socket locations.

1.1 Terminology

Table 1. Terminology

Term	Description
BGA	Ball Grid Array
CRB	Customer Reference Board
DDI	Digital Display Interface
DMI	Direct Media Interface
eDP*	Embedded Display Port
LAN	Local Area Network
LED	Light Emitting Diode
PCH	Platform Controller Hub
PCI	Peripheral Control Interface
PCIe*	PCI Express*

Term	Description
RTC	Real Time Clock
SATA*	Serial AT Attachment
Super-IO	Super Input/Output
SODIMM	Small Outline Dual In-line Memory Module
USB	Universal Serial Bus
XDP	Extended Debug Port

1.2 Reference Documents

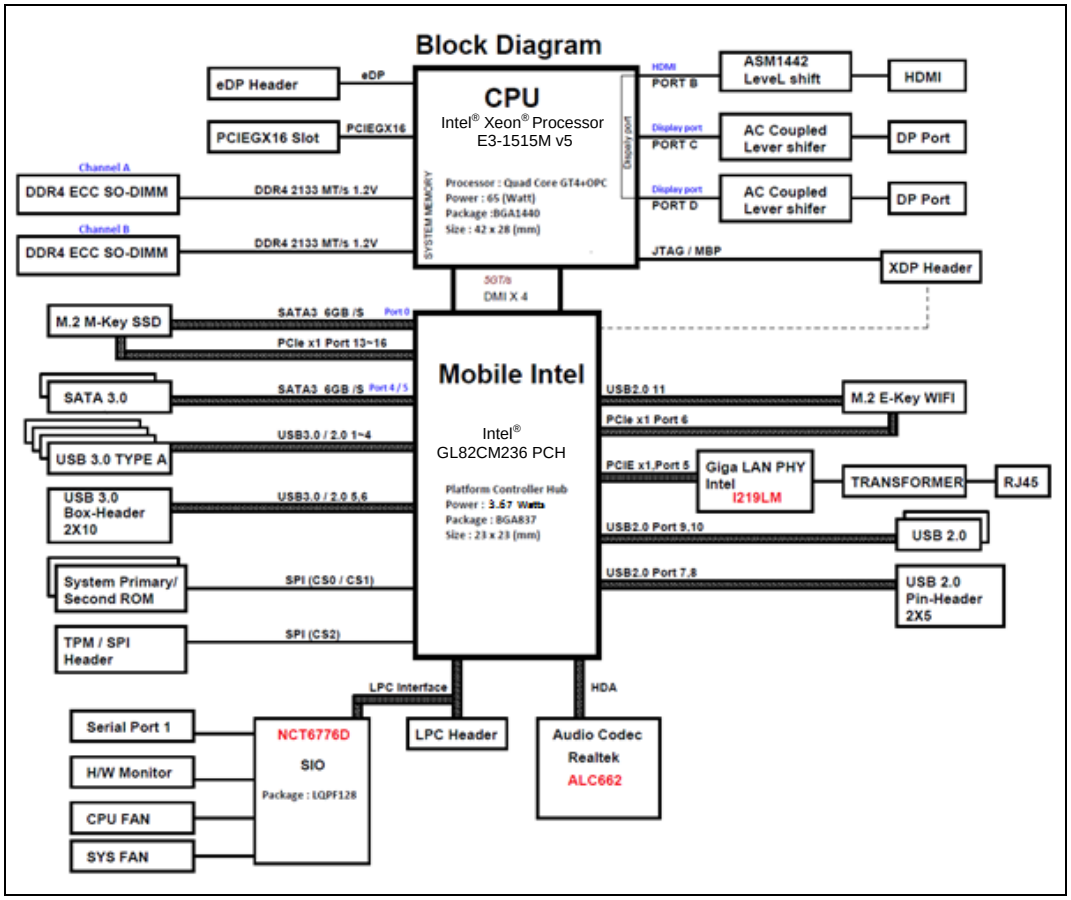
Table 2. Reference Documents

Document	Document No./Location
6th Generation Intel® Core™ Processor Family and Intel® Xeon® Processor E3-1200 v5 Product Family External Design Specification (EDS), Volume 1 of 2	544924
6th Generation Intel® Core™ Processor Family and Intel® Xeon® Processor E3-1200 v5 Product Family External Design Specification (EDS) – Volume 2 of 2	544925
Intel® 100 Series and Intel® C230 Series Chipset Family Platform Controller Hub (PCH) External Design Specification - Volume 1 of 2	546717
Intel® 100 Series and Intel® C230 Series Chipset Family Platform Controller Hub (PCH) External Design Specification, Volume 2 of 2	546955
Intel® Xeon® Processor E3-1515M v5 and Intel® GL82CM236 Platform Controller Hub (PCH) Evaluation Kit - Schematics	559896
Intel® Xeon® Processor E3-1515M v5 and Intel® GL82CM236 Platform Controller Hub (PCH) Evaluation Kit - Board File	559895
Intel® Xeon® Processor E3-1515M v5 and Intel® GL82CM236 Platform Controller Hub (PCH Evaluation Kit - Bill of Materials (BOM)	559501
Intel® Xeon® Processor E3-1505L v5/Intel® CM236 Series Chipset IOTG BIOS Version CSBKG004	560295
Skylake Platform Sightings Report	552319
Best Known Configuration for Mobile Intel® Xeon® Processor E3-1515M v5	560370
Skylake H Platform - Design Guide	546884

§

2.0 CRB Features

Figure 1. CRB Block Diagram



2.1 CRB Feature Set Summary

Table 3. CRB Feature Set Summary

	CRB Implementation	Comments
Processor	Intel® Xeon® Processor E3-1515M v5	• Supports 2 DIMMS per DDR4 channels with ECC and DDR3L • Supports x4 (in each direction) Direct Media Interface (DMI) interface (lane reversed) • 1440-pin BGA Foot-Print
Chipset	Intel® GL82CM236 PCH	• 837-pin BGA Foot-Print
Memory	2x DDR4 ECC Small Outline Dual In-line Memory Module (U-DIMM) slots	CBH supports: • DDR4 frequency of up to 1866 MT/s • DIMM1 (Channel A) • DIMM2 (Channel B)
PCIe*/ External Graphics	1x PCI Express* 3.0 x16	Can be supported as: • 1x16 PEG through x16 slot on CRB
Video	High Definition Multimedia Interface (HDMI*)	• Digital Display Interface (DDI) Port B • Back panel HDMI connector
Video	Display Port	• 2 x Back panel Display Port connectors • DDI Port C and Port D
Video	Embedded DisplayPort (eDP*)	• eDP Port E on board
On-Board LAN	Ethernet	• 10/100/1000 Mbps Ethernet through the onboard (Jacksonville) PHY • On board LAN1 interface
BIOS (SPI)	SPI flash devices	• Support for Serial Flash Discovery parameter (SFDP) • Supports TPM • 2x 8 MB SPI Flash device parts provided on board • Support new Dual I/O Fast read, Quad I/O Fast read, Quad Output Fast read
TPM	TPM on SPI Interface	• 20-pin header
SATA*	Up to 6x Serial AT Attachment (SATA) Ports	• All 2 ports capable of 6GT/s available external on board.

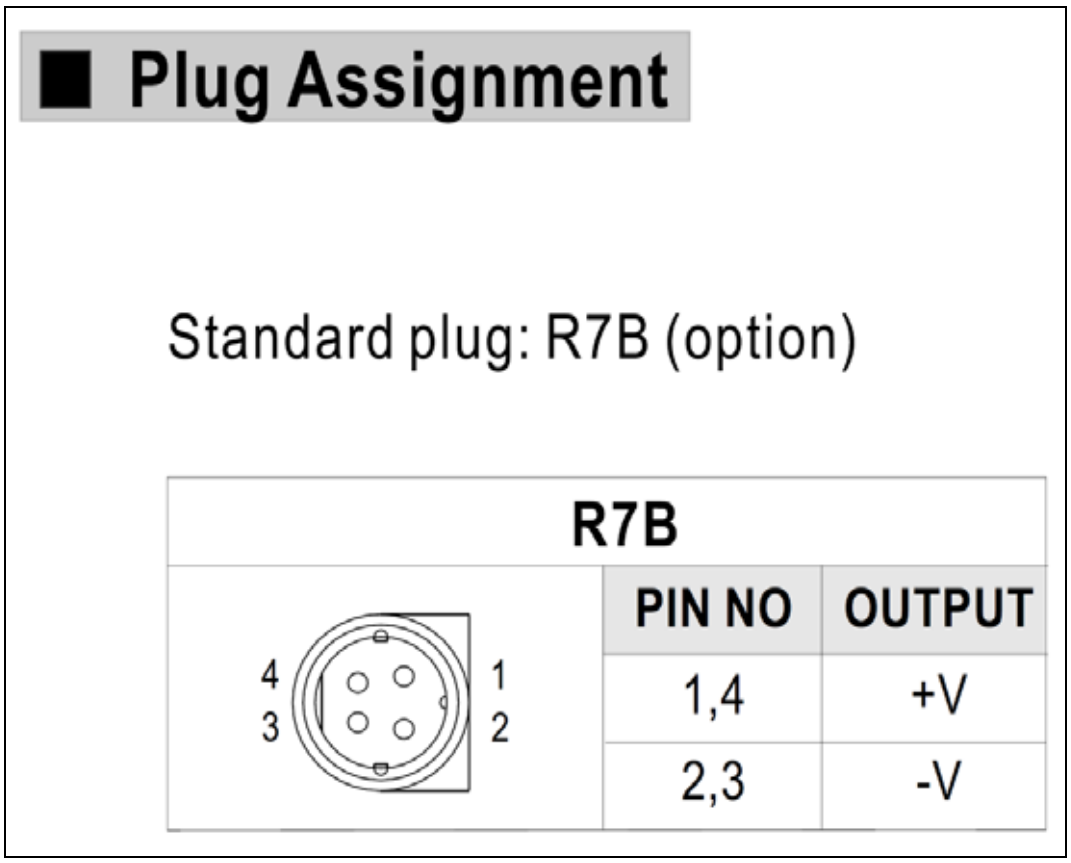
	CRB Implementation	Comments
USB2.0	Up to 10 Universal Serial Bus (USB 2.0)/1.1 Ports	• 10 USB2.0 ports are externally available on the CRB. 6 USB 2.0 ports are available at back panel. • USB11 is connected to the M.2 WLAN
USB3.0	6 USB3.0 Ports	• 4 USB 3.0 ports at back panel and 2 USB 3.0 ports at front panel. • Over current protection provided
SIO	Serial IO	• 2x5 for Serial header • Two fan controllers for CPU and Chassis • Supports PECI
Audio	HD audio codec ALC662 from Realtek	Audio connector on the IO back panel • Audio Output (Lime) • Microphone (Pink)
RTC	Battery-backed real time clock (RTC)	• Implementation similar to earlier Platforms.
Clock	Integrated clock from PCH	• The PCH Integrated Clock Controller (ICC) generates and supplies all the PCH reference clocks for internal needs and it provides the complete platform system clocking solution.
Power Supply	12V DC Jack Connector	• 15 A Maximum
Debug Interfaces	CPU and PCH XDP	• On board CPU PCH Extended Debug Port (XDP)
LPC	LPC Header	• LPC Header available externally on board
Form Factor	Mini-ITX form factor	• 8 layer board – 6.7” x 6.7”

2.2 Power Supply Solutions, Usage, and Recommendations

The CRB must be supplied by a power brick with the following specifications:

- DC Voltage : +V = 12 V; -V = Ground
- Current Range: 15 A Maximum
- Rated Power: 180 W Maximum
- Pin out as shown in Figure 2

Figure 2. Pin Out Specification



Caution: Intel recommends using a power brick that matches the power and pin-out specification. Using the wrong power type or pin type may damage the board permanently. For example, Mean Well GS220A12-R7B matches the requirement for the power supply.

§

3.0 CRB Summary

Figure 3 and Figure 4 describe the layout of the Customer Reference Board. Refer to Table 4 for a list of CRB components.

3.1 Features

Figure 3. CRB Top View

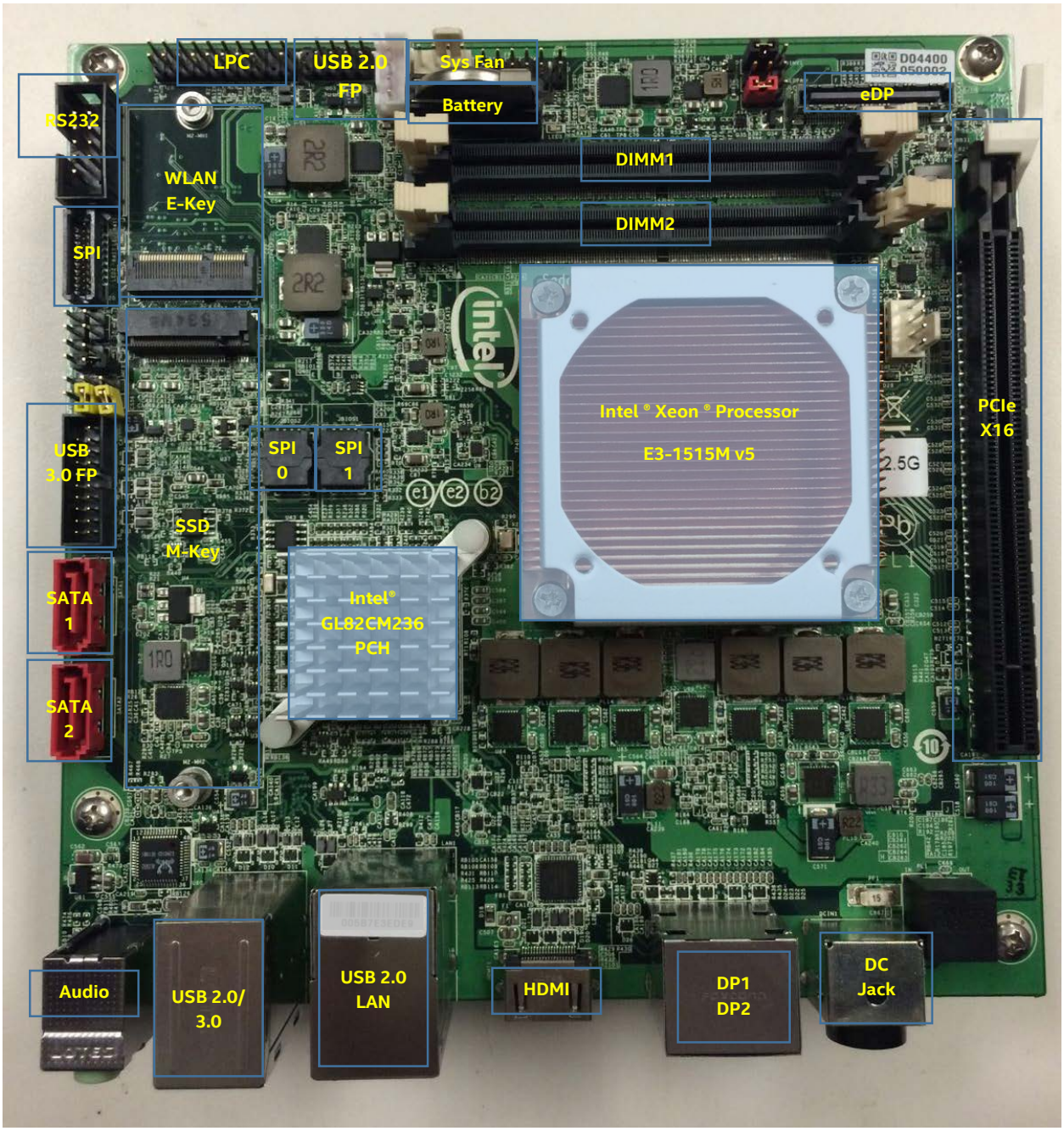


Figure 4. CRB Bottom View

Table 4. CRB Components List

Item#	Description	Reference
1	CPU	U40
2	CPU PCH XDP	JXDP1
3	CPU Fan Connector	CPUFAN1
4	DDR4 SODIMM 1	DIMM1
5	DDR4 SODIMM 2	DIMM2
6	PCH	U41
8	SATA*1 Connector	SATA1
9	SATA2 Connector	SATA2
10	SATA HD Power	PWROUT1
11	PCIe* 3.0 x16 Connector	X16PCEG1
12	Front Panel Header	FP1
13	Front Panel Light Emitting Diode (LED) Header	JFP1
14	Coin Cell Battery Holder	BAT2
15	Super-IO NCT6776F	U58
16	SPI Based TPM Header	TPM1
17	Power Button Header	FP1
18	System Fan	SYSFAN1
19	eDP* Connector	EDP1
20	M.2 E-Key Wi-Fi*	WIFI1
21	M.2 M-Key SSD	SSD1
22	LPC Header	LPC1

3.2 Connectors, Headers, and Jumpers

This section describes the board's various connectors, headers, and jumpers.

Caution: Many of the connectors provide an operating voltage (+5 V DC and +12 V DC, for example) to devices inside the computer chassis, such as fans and internal peripherals. Most of these connectors are not over-current protected. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.

3.2.1 Back Panel Connectors

Figure 5 shows the back panel connectors on the board.

Figure 5. CRB Back Connectors

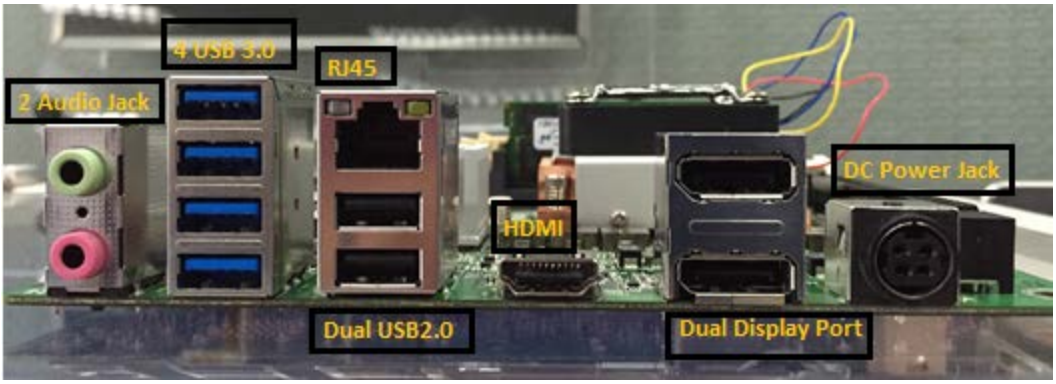


Table 5. Back Panel Components List

Item#	Description	Reference
1	HDMI* connector	HDMI1
3	Dual Display Port	DP1
4	Dual USB 2.0 with RJ45 Connector	LAN1
5	Audio Connector	AUDIO1
6	DC JACK-4P	DCIN1
7	4 USB 3.0 Ports	USB1

3.2.2 Front Panel Header

The CRB has a front panel header comprising of the pin out for Power Switch, Reset Switch, Hard Drive Activity LED, Power LED, and +5V DC. Figure 6 shows the pin out for the header. Refer to Figure 6 for location of the Front Panel Header, FP1, on the CRB board.

Figure 6. Front Panel Header Pin Out Diagram

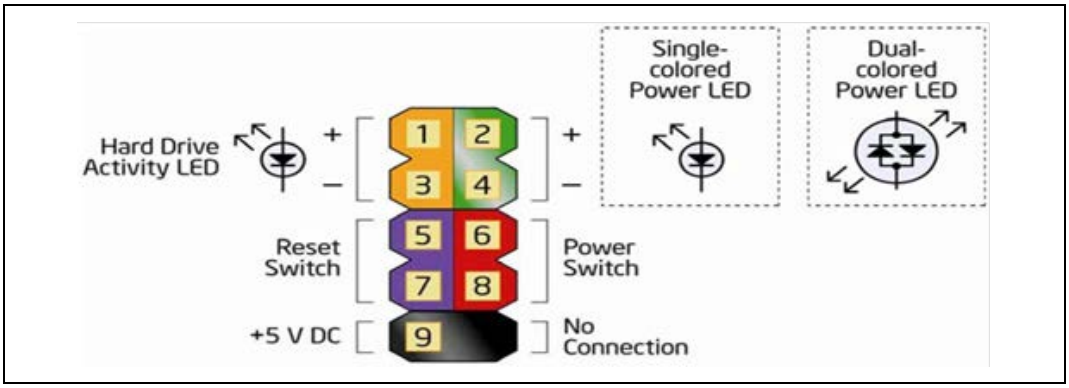


Table 6. Front Panel Header Pin Out Description

Hard Drive Activity LED			
Pin	**Signal**	**In/Out**	**Description**
1	HD_PWR	Out	Hard disk LED Pull-up to +5 V
3	HAD#	Out	Hard Disk Active LED
Power LED			
Pin	**Signal**	**In/Out**	**Description**
2	FP_LED_P	Out	Front Panel Green LED
4	FP_LED_N	Out	Front Panel Yellow LED
Reset Switch			
Pin	**Signal**	**In/Out**	**Description**
5	Ground		Ground
7	FR_RST#	In	Reset Switch
On/Off Switch			
Pin	**Signal**	**In/Out**	**Description**
6	PWRBTN#	In	Power Switch
8	Ground		Ground

Power			
Pin	**Signal**	**In/Out**	**Description**
9	+5 V		Power
Not Connected			
Pin	**Signal**	**In/Out**	**Description**
10	N/C		Not Connected

Note: The Power LED can use either a Single-colored or a Dual-colored Power LED. The header is also alternatively accessible from header JFP1.

3.2.3 CPU Straps

Table 7. CPU Straps

Reference	CRB Implementation (Resistor)	Comments
CFG [0]	RA19- 1KΩ to Ground	Stall reset sequence after PCU PLL lock until de-asserted. 1 = (Default) Normal Operation; No stall. 0 = Stall.
CFG [2]	RA20- 1KΩ to Ground	PCI Express* Static x16 Lane Numbering Reversal. 1 = Normal operation (Default) 0 = Lane numbers reversed.
CFG 4	RA22- 1KΩ to Ground	Embedded Display Port (eDP) Enable 1 = Disabled(Default) 0 = Enabled
CFG [6:5]	RA23 - 1KΩ to Ground RA24 - 1KΩ to Ground	PCI Express Bifurcation 00 : 1 x8, 2 x4 PCIe 01 : Reserved 10 : 2 x8 PCIe 11 : 1 x16 PCIe (Default)
CFG[7]	RA25 - 1KΩ to Ground	PEG Training 1 = PEG Train immediately following RESET# de-assertion.(default) 0 = PEG Wait for BIOS for training.
CFG [1] CFG[3] CFG[19:8]	N/A	Reserved

Refer to the *6th Generation Intel® Core™ Processor Family and Intel® Xeon® Processor E3-1200 v5 Product Family, External Design Specification (EDS), Volume 1 of 2* listed in Table 2 for further information.

3.2.4 Configuration Jumpers/Switches

Caution: Do not move jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing jumper settings. Modifying jumpers with the power on may cause damage to the board.

Table 8. Configuration Jumper/Switches

Reference	Comments Note:
JME1	Flash Descriptor Security Override (1-2): Enable Security Open : Disable (Default) [1] Refer to HDA_SDO strap of *Intel® 100 Series and Intel® C230 Series Chipset Family Platform Controller Hub (PCH) EDS - Volume 1 of 2*
JME2	RTC Reset (1-2) : Clear PCH RTC Open : Normal (Default) [1] Refer to RTCRST# Info of *Intel® 100 Series and Intel® C230 Series Chipset Family Platform Controller Hub (PCH) EDS - Volume 1 of 2* (section 27.4)
JPCH1	SRTC Reset (1-2) : Clear ME RTC Open : Normal (Default) [1] Refer to SRTCRST# info of *Intel® 100 Series and Intel® C230 Series Chipset Family Platform Controller Hub (PCH) EDS - Volume 1 of 2* (section 27.4)
JLCD1	LCD VDD Power Rail (1-2) ON LCD_VDD = +5V (2-3) ON LCD_VDD = +3.3V (Default)

[1] Refer to Table 2 in *Intel® 100 Series and Intel® C230 Series Chipset Family Platform Controller Hub (PCH) EDS - Volume 1 of 2* for more information.

3.3 LEDs

The following LEDs provide status of various functions:

Table 9. CRB LEDs

Reference	Function
LED3	SATA LED
LED1, LED2	Local Area Network (LAN) Status LED

§

4.0 Quick Start Guide

The following sections summarize the necessary hardware and power-on instructions for the CRB.

4.1 Required Peripherals

- Fan/Heat sink combination for processor
- DDR4L ECC SODIMM
- Mobile 12V DC Power Brick
- Keyboard, Mouse
- SATA* Hard Drive
- SATA Cable
- M.2 M-Key SSD
- PCI Express* Graphics Card if not using Internal Graphics
- External Display

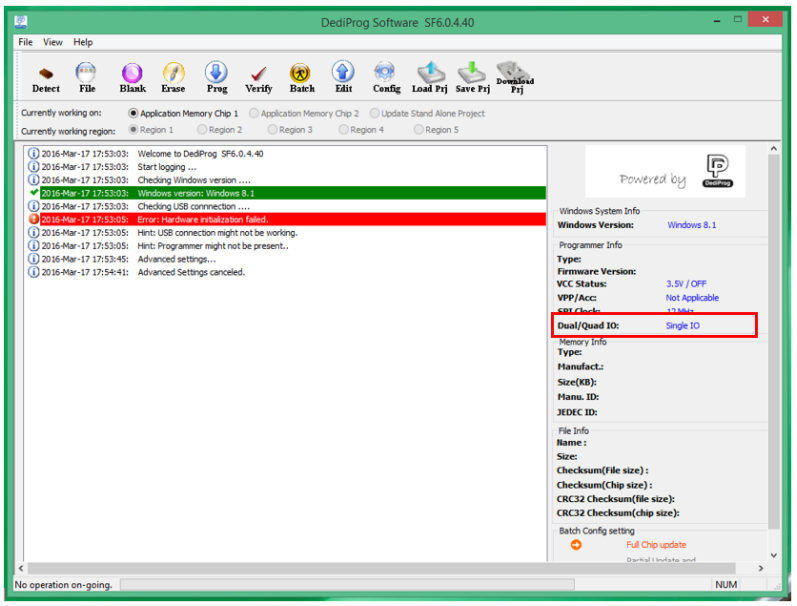
4.2 Instructions to Flash BIOS to SPI Header

The following is setup information to flash the BIOS to the SPI:

- The Flash BIOS can be programmed in dual I/O mode as well as quad I/O mode for more speed.
- In-Circuit programming of SPI flash is supported only when the system power is **OFF**.
- Connect DediProg SF600 with Adaptor B to the SPI header. Refer to Table 4 for location of the header.

1. Install the latest USB drivers for the DediProg SF600 Programmer on the host platform. The in-circuit programming of SPI flash is supported only when the system power is OFF.
2. Launch the DediProg tool and it will detect the SPI chip that is on the board. Confirm the settings in the “Config” menu “Miscellaneous Settings” option. Set the “Dual/Quad IO” to the “Single IO” default as shown in Figure 7.
3. Ensure that “Currently working on” is in “Application Memory Chip 1.”

Figure 7. DediProg SF600 with Adaptor B



4. Go to “File” and select the **.bin file** to program chip1.
5. Execute the batch operation to erase and program the chip.

Note: Ensure Quad IO/Single IO is set when the programming begins.

6. On seeing “no operation on-going” at the bottom left, switch to “Application Memory chip 2.”
7. Select the **.bin file** for chip2 and execute the batch operation.

4.3 Operate, Connect, Power Up, and Power Down the CRB

Note: See Table 4 for a list of all component locations.

4.3.1 Board Setup

Complete the following procedures to operate the CRB:

1. Place one or more DDR4 SODIMM in memory sockets, populating DIMM1 and/or DIMM2.
2. Attach the heat sink/fan for the processor at U40 and plug the fan power cable into CPUFAN1.
3. Install the configuration jumpers as shown in Table 8, “Configuration Jumper/Switches.”
4. Verify the presence of RTC battery in Battery Holder at BAT2.

4.3.2 Board Component Setup

Note: The following steps must be completed by the user:

1. Verify that the DediProg hardware is disconnected before booting the platform to the OS selected.
2. Plug a Power Brick into the chassis.
3. Attach a hard drive at SATA1, SATA2 and/or M.2 M-Key SSD at SSD1.
4. Connect a USB keyboard in one of the USB connectors.
5. Connect a USB mouse in one of the USB connectors.
6. If internal graphics are not used, plug a PCI Express* Graphics card in the PCIe* x16 slot, X16PCEG1, and connect a monitor to the card.

4.3.3 Board Power Up

1. Press the jumper connection at Front Panel FP1.
2. As the system boots, press **F2** to enter the BIOS setup screen.
3. Check time, date, and configuration settings. The default settings should be sufficient for most users.
4. Save and exit the BIOS setup. Then the system directs the user to the OS.

4.3.4 Board Power Down

Below are three options for powering down the CRB:

- Use OS-controlled shutdown through the Windows* Start menu (or equivalent).
- Press the jumper connection connected to the motherboard at FP1 to begin power-down.
- If the system is hung up or stalled, it is possible to asynchronously shut the system down by holding the power button down continuously for four seconds.

Caution: Intel does not recommend powering down the board by simply shutting off power at the power supply. Sudden power-off might cause the damage to components on the CRB while it is still in operation mode.

§