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<th>Revision Number</th>
<th>Description</th>
<th>Revision Date</th>
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<tr>
<td>338747</td>
<td>001</td>
<td>- Initial release</td>
<td>April 2019</td>
</tr>
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</table>
| 338747          | 002             | - Updated Table 5-1, "Second Generation Intel® Xeon® Scalable Processors Non-MCP SKU Thermal Specifications"  
                  |                  | - Updated Table 5-4, "Second Generation Intel® Xeon® Scalable Processors - SP ISS Thermal Specifications" | June 2019         |
| 338747          | 003             | - Updated Table 5-1, "Second Generation Intel® Xeon® Scalable Processors Non-MCP SKU Thermal Specifications"  
                  |                  | - Added Table 5-3, "Second Generation Intel® Xeon® Scalable Processors Refresh Non-MCP SKU Thermal Specifications"  
                  |                  | - Updated Table 5-4, "Second Generation Intel® Xeon® Scalable Processors - SP ISS Thermal Specifications" | June 2019         |
| 338747          | 004             | - Added Table 5-2, "Second Generation Intel® Xeon® Scalable Processors High Frequency Thermal Specifications"  
                  |                  | - Updated Table 5-3, "Second Generation Intel® Xeon® Scalable Processors Refresh Non-MCP SKU Thermal Specifications" | August 2019       |
| 338747          | 005             | - Updated SKU Intel® Xeon® Gold 5219W CPU in Table 5-3, "Second Generation Intel® Xeon® Scalable Processors Refresh Non-MCP SKU Thermal Specifications" | September 2019    |
1 Introduction

This document provides specifications and guidelines for the design of thermal and mechanical solutions for the Second Generation Intel® Xeon® Scalable Processors.

1.1 Objective

This document explains and demonstrates the processor thermal and mechanical solution features and requirements. This document also provides an understanding of the processor thermal characteristics, and discusses guidelines for meeting the thermal requirements imposed on the entire life of the processor. As such, the purpose of this design guide is to describe the reference thermal solution and design parameters required for the Second Generation Intel® Xeon® Scalable Processors. The thermal/mechanical solutions described in this document are intended to aid component and system designers in developing and evaluating processor compatible solutions.

The components and information described in this document include:

- Thermal profiles and other processor specifications and recommendations
- Processor mechanical load limits
- Processor socket and board structural support
- Processor Heatsink Module (PHM) specifications and recommendations
- Heatsink specifications and recommendations

The goals of this document are:

- To assist board and system thermal mechanical designers
- To assist designers and suppliers of processor heatsinks

1.2 Scope

The thermal/mechanical solutions described in this document pertain only to a solution(s) intended for use with the Second Generation Intel® Xeon® Scalable Processors in 1U, 2U, 4U form factor systems. This guide contains the mechanical and thermal requirements of the processor compatible cooling solution. Additional reference information is provided in the appendices of this document. The components described in this document include:

- The processor package
- The LGA3647-0 socket (socket P0)
- The Processor Heatsink Module (PHM) and the associated retention hardware
- Socket P0 retention mechanism
Introduction

Figure 1-1. PHM Assembly

Heatsink shown is for illustration only.

Note: The PHM assembly is shown with narrow retention mechanism and heatsink.

1.3 References

Material and concepts available in the following documents may be beneficial when reading this document.

Table 1-1. Reference Documents

<table>
<thead>
<tr>
<th>Document Title</th>
<th>Reference Number</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Second Generation Intel® Xeon® Scalable Processors Datasheet Volume One: Electrical</td>
<td>338845</td>
<td></td>
</tr>
<tr>
<td>Second Generation Intel® Xeon® Scalable Processors Datasheet Volume Two: Registers</td>
<td>338846</td>
<td></td>
</tr>
<tr>
<td>Second Generation Intel® Xeon® Scalable Processors Specification Update</td>
<td>338848</td>
<td></td>
</tr>
</tbody>
</table>
## 1.4 Terminology

### Table 1-2. Terms and Descriptions (Sheet 1 of 2)

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bypass</td>
<td>Bypass is the area between a passive heatsink and any object that can act to form a duct. For this example, it can be expressed as a dimension away from the outside dimension of the fins to the nearest surface.</td>
</tr>
<tr>
<td>DTS</td>
<td>Digital Thermal Sensor reports a relative die temperature as an offset from TCC activation temperature.</td>
</tr>
<tr>
<td>FSC</td>
<td>Fan Speed Control</td>
</tr>
<tr>
<td>HTg</td>
<td>Printed circuit board material, such as FR4, with high glass transition temperature</td>
</tr>
<tr>
<td>IHS</td>
<td>Integrated Heat Spreader: a component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.</td>
</tr>
<tr>
<td>LECS4B</td>
<td>54 Pin high speed low loss edge connector design specifically for Intel processors</td>
</tr>
<tr>
<td>LGA3647 Socket</td>
<td>Surface mounted socket with 3647-contacts enabling the processor to interface with the system board</td>
</tr>
<tr>
<td>Margin to TCONTROL</td>
<td>Least margin based on each die type with a TCONTROL</td>
</tr>
<tr>
<td>Margin to Throttle</td>
<td>Least margin based on each die type</td>
</tr>
<tr>
<td>Pad Crater</td>
<td>Mechanically induced fracture in the resin between copper foil and outermost layer of fiberglass of a printed circuit board</td>
</tr>
<tr>
<td>PECI</td>
<td>The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between the Intel processor and the chipset components to the external monitoring devices.</td>
</tr>
<tr>
<td>PHM</td>
<td>Processor Heatsink Module - An assembly of processor and heatsink</td>
</tr>
<tr>
<td>PHLM</td>
<td>Processor Heatsink Load Mechanism</td>
</tr>
<tr>
<td>$\Psi_{CA}$</td>
<td>Case-to-ambient thermal characterization parameter. A measure of thermal solution performance. Defined as $(T_{CASE} - T_{LA}) / \text{Total Package Power}$. Heat source should always be specified for $\Psi$ measurements.</td>
</tr>
<tr>
<td>$\Psi_{CS}$</td>
<td>Case-to-sink thermal characterization parameter. A measure of thermal interface material performance. Defined as $(T_{CASE} - T_{S}) / \text{Total Package Power}$.</td>
</tr>
<tr>
<td>$\Psi_{SA}$</td>
<td>Sink-to-ambient thermal characterization parameter. A measure of heatsink thermal performance using total package power. Defined as $(T_{S} - T_{LA}) / \text{Total Package Power}$.</td>
</tr>
<tr>
<td>$T_{\text{CASE}}$</td>
<td>The case temperature of the processor measured at the geometric center of the topside of the IHS</td>
</tr>
<tr>
<td>$T_{\text{CASE-MAX}}$</td>
<td>The maximum case temperature as specified in a component specification</td>
</tr>
<tr>
<td>TCC</td>
<td>Thermal Control Circuit: Thermal monitor uses the TCC to reduce the die temperature by using clock modulation and/or operating frequency and input voltage adjustment when the die temperature is very near its operating limits.</td>
</tr>
<tr>
<td>TCONTROL</td>
<td>TCONTROL is a static value below TCC activation that is used as a trigger point for fan speed control. When DTS $&gt;$ TCONTROL, the processor must comply to the thermal profile.</td>
</tr>
<tr>
<td>TDP</td>
<td>Thermal Design Power: Thermal solution should be designed to dissipate this target power level. TDP is not the maximum power that the processor can dissipate.</td>
</tr>
<tr>
<td>Thermal Monitor</td>
<td>A power reduction feature designed to decrease temperature after the processor has reached its maximum operating temperature</td>
</tr>
<tr>
<td>Thermal Profile</td>
<td>A line that defines the case temperature specification of a processor at a given power level.</td>
</tr>
<tr>
<td>TIM</td>
<td>Thermal Interface Material: The thermally conductive compound between the heatsink and the processor case. This material fills the air gaps and voids, and enhances the transfer of the heat from the processor case to the heatsink.</td>
</tr>
</tbody>
</table>
Table 1-2. Terms and Descriptions (Sheet 2 of 2)

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{LA}$</td>
<td>The measured ambient temperature locally surrounding the processor. The ambient temperature should be measured just upstream of a passive heatsink or at the fan inlet for an active heatsink.</td>
</tr>
<tr>
<td>$T_{SA}$</td>
<td>The system ambient air temperature external to a system chassis. This temperature is usually measured at the chassis air inlets.</td>
</tr>
<tr>
<td>U</td>
<td>A unit of measure used to define server rack spacing height. 1U is equal to 1.75 in, 2U equals 3.50 in., and so forth.</td>
</tr>
</tbody>
</table>
2 Processor Package Mechanical Specification

This section provides an overview of the processor package mechanical design and integration. The package serves as the primary interface between the processor silicon die and the rest of the system. The package provides electrical signaling and power delivery as well as thermal transmission, mechanical physical attach, dimensional scale translation and structural strength and stiffness. A solid understanding of the processor design targets provides the necessary foundation to identify and establish thermal and mechanical design requirements for the motherboard and the system.

To ensure compatibility with the processor and the platform, the mechanical processor retention and thermal solution must meet the requirements and keep out zones of both the processor and the LGA3647-0 socket. This section provides the processor package specific mechanical specifications and handling guidance.

2.1 Processor Package Description

The processor is housed in an Flip-Chip Land Grid Array (FC-LGA14) package that interfaces with the motherboard via an LGA3647-0 SMT socket. The package consists of a processor Integrated Heat Spreader (IHS), which is attached to the package substrate and die and serves as the mating surface for the processor component thermal solutions, such as a heatsink. The IHS transfers the non-uniform heat from the die to the top of the IHS, out of which the heat flux is more uniform and spread over a larger surface area (not the entire IHS area). This allows more efficient heat transfer out of the package to an attached cooling device. The IHS is designed to be the interface for contacting a heatsink.

Processor package dimension includes an IHS. The bottom side of the package has 3647 lands in a 43.18 x 50.24 mm pad array which interfaces with the LGA3647-0 SMT socket. Regardless of the package form factor of the Second Generation Intel® Xeon® Scalable Processors 2S with two Intel® Ultra Path Interconnects (Intel® UPI), and Second Generation Intel® Xeon® Scalable Processors with three Intel® UPI SKUs are compatible with the LGA3647-0 SMT socket. Mechanical compatibility with the socket is controlled through a predefined package to socket keying size and location. The following figure shows a sketch of the processor package components and how they are assembled together.

Note: The processor package actual land count is greater than the socket contact count. The 137 additional pads are reserved for use during the manufacturing process.
Figure 2-1. Processor Assembly - ISO View

The next package illustrations include the following features:

1. Integrated Heat Spreader (IHS) - Step
2. Integrated Heat Spreader (IHS) - Top Surface
3. PHM package carrier keying slot
4. Socket keying slot
5. Processor package substrate
6. Integrated Heat Spreader (IHS) - Step
7. Socket keying slot
8. Integrated Heat Spreader (IHS) - Step
9. Pin 1 indicator
10. PHM package carrier latch slot
2.2 Processor Mechanical Dimensions

The processor package mechanical drawings are referenced in Appendix B. They include dimensions necessary to design a thermal solution for the processor. These dimensions include:

1. Package reference dimensions with tolerances (total height, length, width, and so on)
2. IHS parallelism and tilt
3. Land dimensions
4. Top-side and back-side component keep-out dimensions
5. Reference datum

2.3 Processor Keep-Out Zones

The processor contains components on the top and bottom sides of the interposer that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the identified keep-out zones. See processor package mechanical drawing for location, size, and additional information on keep-out zones. The location and quantity of package capacitors may change but will remain within the component keep-in areas.

2.4 Processor Mechanical Loads

The processor package has mechanical load limits that should not be exceeded during the processor ILM actuation, heatsink installation and removal, mechanical stress testing, or standard shipping conditions as permanent damage to the processor may occur. For example, when a compressive static load is necessary to ensure thermal performance of the Thermal Interface Material (TIM2) between the heatsink base and the IHS, it should not exceed the corresponding specification. The processor substrate should not be used as a mechanical reference or load-bearing surface for thermal solutions.

Table 2-1 provides load specifications for the processor package. These maximum limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Exceeding these limits during test may result in component failure. The processor substrate should not be used as a mechanical reference or load bearing surface for thermal solutions unless identified within this document.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. Allowable Static Compressive Load</td>
<td>1334 N [300 lbf]</td>
<td>2</td>
</tr>
<tr>
<td>Max. Allowable Dynamic Compressive Load</td>
<td>588 N [132 lbf]</td>
<td>1, 2, 3</td>
</tr>
</tbody>
</table>

Notes:
1. Duration of the load does not exceed one second (1 s).
2. These specifications apply to uniform compressive loading in the direction normal to the processor IHS.
3. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
4. Through the life of product. The condition must be satisfied at the beginning of life and at the end of life.
5. Loads include coupling load for 0.6 kg HS in 3.13 gRMS.

The heatsink will also add an additional dynamic compressive load to the package during a mechanical shock event. Amplification factors due to the impact force during shock must be taken into account in dynamic load calculations. The total combination
of dynamic and static compressive load should not then exceed the processor compressive dynamic load during a vertical shock. Using any portion of the processor substrate as a load-bearing surface in either static or dynamic compressive load conditions is not recommended.

2.4.1 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Do not contact the test pad area with conductive material. Decoupling capacitors are typically mounted to either the topside or land-side of the package substrate. See the processor package mechanical drawing for location, size, and additional information on keep-out zones. The location and quantity of package capacitors may change due to manufacturing efficiencies but will remain within the component keep-in areas.

2.4.1.1 Processor Materials

Table 2-2 lists some of the package components and associated materials.

Table 2-2. Processor Materials

<table>
<thead>
<tr>
<th>Component</th>
<th>Material</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integrated Heat Spreader (IHS)</td>
<td>Nickel Plated Copper</td>
</tr>
<tr>
<td>Substrate</td>
<td>Halogen Free, Fiber Reinforced Resin</td>
</tr>
<tr>
<td>Substrate Lands</td>
<td>Gold Plated Copper</td>
</tr>
</tbody>
</table>

2.5 Processor Mass Specification

The typical mass of the processor is 112 grams. This mass includes all the components that are included in the package.

2.6 Package Insertion Specifications

Table 2-3. Package Interface Requirement

<table>
<thead>
<tr>
<th>Socket Insertion</th>
<th>The processor can be inserted into and removed from an LGA3647-0 socket 30 times.</th>
</tr>
</thead>
</table>
2.7 Processor Markings

Figure 2-3 shows the topside markings on the processor. This diagram is to aid in the identification of the processor.

Figure 2-2. Second Generation Intel® Xeon® Scalable Processors Package Topside Markings

- **Serial Number 2DID**
- **Production Mark (SSPEC):**
  - **GRP1LINE1:** INTEL LOGO
  - **GRP1LINE2:** BRAND
  - **GRP1LINE3:** PROCESSOR NUMBER
  - **GRP1LINE4:** SSPEC SPEED
  - **GRP1LINE5:** FPO (eX)
2.7.1 Package Handling Guidelines

The processor package may contain components on the top or bottom sides of the interposer. To remove the processor from its shipping container or the tray, grab and hold the processor along its long edges.

**Note:** Avoid contacting the processor bottom side lands and/or gold fingers.

When installing the processor into the socket, care should be taken to ensure that the processor is properly oriented, that is the processor pin-1 is in the same direction as the socket pin-1, and that there are no contaminations or foreign material on the land pads or gold fingers.

In a case where the processor is not installed into the socket, it should be placed or stored in the appropriate tray or container as to avoid damaging the package interposer or its bottom side components.
3 Socket Specifications

This section describes the LGA3647-0 surface mount Land Grid Array (LGA) socket. The socket contains a total of 3647 contacts and provides I/O, power, and ground connections from the main board to the processor package.

The socket definitions listed intend to identify the minimum socket requirements and features necessary to ensure compatibility with the Second Generation Intel® Xeon® Scalable Processors and the Second Generation Intel® Xeon® Scalable Processors based platform. In addition to these, socket suppliers may include design features to ensure their socket design meets Intel specifications as well as their manufacturing process requirements. See the supplier listing for ordering and contacting information.

3.1 Socket Overview

The LGA3647-0 socket is made up of two sections. Each section of the socket consists of the socket body and the Pick and Place (PnP) cover. The two halves are not interchangeable and are distinguishable from one another by the colors of the keying features: yellow for one half and black for the other. They are delivered by the socket supplier as a single integral assembly. The main body of the socket, which is made of electrically insulated material with resistance to high temperature, houses the socket contacts. Figure 3-1 illustrates the socket features. Keying features (wall protrusions) within the contact array area and raised edges of the socket body help align the package with respect to the socket contacts.

Figure 3-1. LGA3647-0 Socket with PNP Capacitor

Note: Picture shown is of a generic LGA3647 socket. See socket drawing for feature details such as package keying associated with the LGA3647-0 socket.
Figure 3-2. LGA3647-0 Socket with PNP Capacitor Post SMT Process

Figure 3-3. LGA 3647-0 Socket (Right Side)
Note: Socket contacts are not shown.

Table 3-1. Socket Features Attribute

<table>
<thead>
<tr>
<th>Socket Feature</th>
<th>Attributes</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Socket wall exterior dimensions</td>
<td>82 mm x 62 mm</td>
<td>As measured post assembly and includes both sections of the socket</td>
</tr>
<tr>
<td>Socket wall interior dimensions</td>
<td>76.11 mm x 56.6 mm</td>
<td></td>
</tr>
<tr>
<td>Solder ball pitch</td>
<td>0.86 mm (X) x 0.99 mm (Y)</td>
<td>Hexagonal pattern</td>
</tr>
<tr>
<td>Ball count</td>
<td>3647</td>
<td>Not all socket contacts are assigned to a processor signal. Some are reserved or are considered NCTF.</td>
</tr>
</tbody>
</table>

The socket interfaces with the Processor Heatsink Module (PHM). Socket loading is achieved through locking down the PHM to the PHLM. Uniform load on the socket solder joints is achieved through the backplate held to the motherboard secondary side.

The socket cover is intended to be reusable and recyclable. It will enable socket pick and placing during motherboard assembly. The socket cover will also protect the socket contacts from contamination and damage during board assembly and handling.
3.2 Socket Features

The LGA3647 socket is made of two sections, right (B) and left (A) sides. Sections are similar, but not identical. Key differences between the sections are the locations of the package keying. Care should be taken to ensure package keying matches the LGA3647-0 socket.

Key features of the LGA3647 socket include contact array, socket cavity, package keying, side walls, package seating plane, slides and guides for the pick and place capacitor, and the clearance for the PHM package carrier.

Figure 3-5. LGA3647-0 Mechanical Features

3.3 Socket Housing

3.3.1 Housing Material

The socket housing material should be thermoplastic or equivalent, UL 94 V-0 flame rating, temperature rating and design capable of maintaining structural integrity following a temperature of 260 °C for 40 seconds, which is typical of a reflow/rework profile for solder material used on the socket. The material must have a thermal coefficient of expansion in the XY plane capable of passing reliability tests rated for an expected high operating temperature, mounted on HTg FR4-type motherboard material.

The material of socket housing is required to have minimum yield strength of 35 MPa at 90 ºC to minimize the risk of seating plane deformation.

The creep properties of the material must be such that the mechanical integrity of the socket is maintained for the stress conditions outlined in Appendix A.
3.3.2 Housing Color

The color of the socket housing must be dark as compared to the solder balls to provide the contrast needed for OEM's pick and place vision systems. Components of the socket may be different colors as long as they meet the previous requirement.

3.3.3 Package Installation/Removal Access

Access must be provided to facilitate the manual insertion and removal of the package. No tool should be required to install or remove the package from the socket.

3.3.4 Package Alignment/Orientation

A means of providing fixed alignment and proper orientation with the pin 1 corner of the package must be provided. There are three different levels of package alignment:

- The first level is called gross alignment, which happens between PHM and the posts on the bolster plate.
- The second level is called intermediate alignment, which utilizes the socket exterior corner walls and package clip.
- The third level, which is fine alignment, relies on the socket inner wall surfaces.

The socket also has orientation posts or protrusions (keys) placed on opposite sides of the socket as noted in Appendix C. The package substrate will have keying notches at the corresponding locations. When package keying notches align with socket orientation posts, it prevents the package from being mistakenly installed with a 180 degree in-plane rotation. The package will sit flush on the socket contacts when aligned.

3.3.5 Heatsink Retention and Processor Package Carrier Compatibility

A direct keying feature between the bolster plate and LGA3647-0 socket does exist. Keying is achieved through the board hole pattern for the bolster plate which is defined specifically for LGA3647-0 compatible bolster plates (narrow and square). During board assembly special attention should be given to the bolster plate part number and the processor package keying on the socket.

Two cutouts on the ends of socket provides clearance for the PHM package carrier-package latch feature. In addition, the PHM package carrier utilizes the socket side walls as the pre-alignment between the socket and processor.

3.3.6 Markings

All markings required in this section must withstand a temperature of 260 °C for 40 seconds, which is typical of a reflow/rework profile for solder material used on the socket, as well as any environmental test procedure outlined in Appendix A, without degrading. Socket marks must be visible after it is mounted on the motherboard.

- Name:

  LF-LGA3647-0 (font type is Helvetica Bold – minimum 4 point [or 1.411 mm])

Note: This mark shall be molded or laser marked as shown in Appendix C.

  Manufacturer’s Insignia (font size at supplier’s discretion).
This mark will be molded or laser-marked into the top side of the socket housing.

Both socket name and manufacturer’s insignia must be visible when first seated on the motherboard.

- Lot Traceability

Each socket will be marked with a lot identification code to allow traceability of all components, date of manufacture (year and week), and assembly location. The mark must be placed on a surface that is visible after the socket is mounted on the motherboard. In addition, this identification code must be marked on the exterior of the box in which the unit is shipped.

- Visual Aids

The socket must have pin A1 and package/socket alignment keys.

### 3.3.7 Contact Characteristics

#### Number of Contacts

Total number of contacts: 3647

#### Layout

The contacts are laid out in two “C” shape regions opposing each other. The arrows in the figure indicate the wiping orientation of the contacts in the two regions to be 60° about the horizontal axis. There are 1823 and 1824 contacts in the right and left halves of the socket, respectively.

#### Base Material

High-strength copper alloy.

#### Contact Area Plating

For the area on socket contacts where processor lands will mate, there is either a 0.762 μm [30 μ-inches] or 0.381 μm [15 μ-inches] gold plating over 1.27 μm [50 μ-inches] minimum nickel under plating in critical contact areas (area on socket contacts where processor lands will mate) is required. No contamination by solder in the contact area is allowed during solder reflow.

#### Lubricants

For the final assembled product, no lubricant is permitted on the socket contacts. If lubricants are used elsewhere within the socket assembly, these lubricants must not be able to migrate to the socket contacts.

#### Co-Planarity

The co-planarity (profile) requirement for all contacts mating to the top side of the socket is defined in the socket drawing.

#### True Position

The contact pattern has a true position requirement with respect to applicable datum in order to mate with the package land pattern.
Stroke/Load

The minimum vertical height of the contact above the package seating plane is defined in the socket drawing. The minimum vertical stroke of the contact must, under all tolerance and warpage conditions, generate a normal force load to ensure compliance with all electrical requirements of the socket. The cumulative normal force load of all contacts must not exceed the load limits.

3.3.8 Contact/Pad Mating Location

The offset between processor package LGA land center and solder ball center is defined in the following figure. All socket contacts should be designed such that the contact tip does not damage solder resist, defining the LGA land during actuation and remains within the substrate pad boundary as illustrated. All sockets must also not interfere with solder resist at minimum static compressive load per contact and at final installation after actuation load is applied. This requirement includes all the X-Y tolerances such as socket size, substrate size, and pad true positional tolerance, as defined in socket drawings. Also it is recommended that the contact tip remains within the substrate pad before any actuation load is applied.
3.3.9 Contact-Deflection Curve

The contact should be designed with an appropriate spring rate and deflection range to ensure adequate contact normal force in order to meet EOL performance at all contact locations. The load-deflection curve is not necessary to be linear between the minimum and maximum deflection points. The LGA contact working range is defined as the difference of contact deflection at the minimum contact load and the maximum contact deflection.
3.3.10 Solder Ball Characteristics

**Number of Solder Balls**

Total number of solder balls: 3647

**Layout**

The solder balls are laid out in two “C” shape regions, see socket drawing for details.

**Material**

Lead free SAC solder alloy with a silver content between 3% and 4% with a melting point temperature of 217 °C maximum (for example, SnAgCu) and is compatible with standard lead free processing such as Immersions silver (ImAg) and OSP MB surface finish with SnAg/SnAgCu solder paste.

**Co-Planarity**

The co-planarity (profile) requirement for all solder balls on the underside of the socket is defined in the socket drawing.

**True Position**

The solder ball pattern has a true position requirement with respect to applicable datum in order to mate with the motherboard land pattern. Refer to the socket drawing for details.
Solder Ball Wetting Angle

To minimize the risk associated with shock, vibration, and transient bend stresses, the solder ball wetting angle must be controlled via ball attach process optimization such that the post SMT wetting angle, as defined in Figure 3-10, is less than or equal to 90 degrees. In the event that a correlation can be identified between wetting height and wetting angle, the wetting height may also be used as a measurable success criterion.

Figure 3-10. Solder Ball Wetting Angle and Height

3.4 Socket Mechanical Requirements

3.4.1 Socket Size

The socket should meet the dimensions provided in the Appendix C.

3.4.2 Socket Standoffs

Standoffs must be provided on the solder ball side of the socket base to ensure the minimum socket height after solder reflow and to prevent socket housing over deflection after being loaded. It is required that wherever there is a top side primary socket seating plane for package, there should be a corresponding standoff on the bottom side. A gap between the solder-ball seating plane and the standoff prior to reflow is required to ensure sufficient ball collapse during surface mount.

3.4.3 Package Seating Plane

The socket seating plane for the package defines the minimum package height from the motherboard. See the processor mechanical drawing for details on package and IHS height above the motherboard. The datum is defined by the top surfaces of seating plane standoffs which cause a hard stop of package over the socket when the package and socket are loaded. There are primary socket seating planes and secondary socket seating planes.

- Primary seating planes are located at areas where contacts are depopulated and around socket cavity and center split location as illustrated.
- Secondary seating planes are interstitial seating planes, which are small islands within a pitch range and around each core pin except for manufacturing keep-outs.
Both primary and secondary seating plane area and numbers of the seating planes are maximized to avoid significant creep of the housing material when being loaded; however, the seating plane standoffs should not touch the LGA lands on the bottom of the package. It is recommended that the nominal height of interstitial seating plane be the same as the nominal height of primary seating planes, but the highest points of interstitial seating planes must be no higher than the highest points of primary socket seating planes. The seating plane co-planarity needs to meet the specification after socket surface mount.

### 3.4.4 Package Translation

The socket should be built so that the post-actuated seating plane of the package is flush with the seating plane of the socket. Movement will be along the axis normal to the seating plane.

### 3.4.5 Insertion/Removal/Actuation Forces

Any actuation must meet or exceed SEMI S8-95 Safety Guidelines for Ergonomics/Human Factors Engineering of Semiconductor Manufacturing Equipment, example Table R2-7 (Maximum Grip Forces).

Access must be provided to facilitate the manual insertion and removal of the package. The socket must be designed so that it requires no force to insert the package into the socket. No tool should be required to install or remove the package from the socket.
3.4.6 Orientation in Packaging, Shipping, and Handling

Packaging media needs to support high-volume manufacturing. Media design must be such that no component of the socket (solder balls, contacts, housing, and so on) is damaged during shipping and handling. Each part number will be shipped from suppliers in separate Joint Electron Device Engineering Council (JEDEC*) trays; for example, all left halves of the socket in 1 tray and all right halves in another. Tray height could be taller than standard.

3.4.7 Pick and Place and Handling Cover

To facilitate high-volume manufacturing, the socket should have a detachable cover to support the vacuum type pick and place system. The cover will remain on the socket during reflow to help prevent contamination. The cover can withstand 260 °C for 40 seconds (typical reflow/rework profile) and the conditions listed without degrading. The cover could also be used as a protective device to prevent damage to the contact field during handling.

Cover retention must be sufficient to support the socket weight during lifting, translation, and placement, during board manufacturing, and throughout board and system shipping and handling. The cover design should allow use of a tool to remove the cover. The force required for removing of the cover should meet or exceed the applicable requirements of SEMI S8-0999 Safety Guidelines for Ergonomics/Human Factors Engineering of Semiconductor Manufacturing Equipment. The removal of the cover should not cause any damage to the socket body nor to the cover itself within the cover durability limit.

The pick and place cover should provide a viewing window to make the pin A1 indicator visible on the underlying socket.

Table 3-2. Socket PnP Cover Insertion/Removal

<table>
<thead>
<tr>
<th>Direction</th>
<th>Condition</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>In plane</td>
<td>Removal</td>
<td>0.77 kgf [1.7 lb f] max.</td>
<td>Pinch Grip Orientation</td>
</tr>
<tr>
<td>In and Out Plane</td>
<td>Shock</td>
<td>0.36 kgf [0.8 lb f] min.</td>
<td>Shipping condition</td>
</tr>
<tr>
<td>Vertical</td>
<td>Closed position at 260 °C</td>
<td>0.34 kgf [0.75 lb f] min.</td>
<td>To support socket vertical lift-off during SMT process</td>
</tr>
<tr>
<td></td>
<td>Closed position at room temperature</td>
<td>0.34 kgf [5.0 lb f] min. 10 kgf [22.0 lb f] max.</td>
<td>PnP cover shall not fall-off in rework</td>
</tr>
</tbody>
</table>

3.4.8 Durability

The socket must withstand 30 cycles of processor insertion and removal. The maximum part average and single pin resistance from Appendix G, "Board Flexure Initiative" must be met when mated in the first and 30th cycles.

3.4.9 Socket Keep-In/Keep-Out Zone

Socket keep-in and keep-out zones are identified on the motherboard to ensure that sufficient space is available for the socket, and to prevent interference between the socket and the components on the motherboard. These areas are illustrated in board volumetric keep-outs for the socket. It is the responsibility of the socket supplier and the customer to identify any required deviation from specifications identified here.
3.4.10 Attachment

The socket will be attached to the motherboard via its 3647 solder balls. There are no additional external methods (that is, screw, extra solder, adhesive, and so on) to attach the socket.

The socket will be tested against the mechanical shock and vibration requirements under the expected use conditions with all assembly components under the loading conditions.

3.4.11 Socket Loading and Deflection Specifications

The socket must meet the mechanical loading and strain requirements outlined in the following table. These mechanical load limits should not be exceeded during component assembly, mechanical stress testing, or standard drop and shipping conditions. All dynamic requirements are under room temperature conditions while all static requirements are under 125 °C conditions.

Table 3-3. Socket Loading and Deflection Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Values</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min.</td>
<td>Max.</td>
</tr>
<tr>
<td>Static Compressive Load Per Contact</td>
<td>10 gf</td>
<td>25 gf</td>
</tr>
<tr>
<td>Dynamic Compressive Load</td>
<td>N/A</td>
<td>588 N [132 lbf]</td>
</tr>
<tr>
<td>Board Transient Bend Strain</td>
<td>62 to 72 mil board thickness</td>
<td>500 µs (MicroStrain)</td>
</tr>
<tr>
<td></td>
<td>93 to 130 mil board thickness</td>
<td>450 µs (MicroStrain)</td>
</tr>
</tbody>
</table>

Notes:
1. The compressive load applied on the LGA contacts to meet electrical performance.
2. The total compressive load applied by the heatsink onto the socket through the processor package.
3. Maximum allowable strain below socket BGA corners during transient loading events (i.e., slow displacement events) which might occur during board manufacturing, assembly or testing. See the LGA3647 Board Flexure Initiative (BFI) Strain Guidance Sheet. Contact your CQE for this datasheet.
4. Dynamic compressive load applies to all board thicknesses.
5. The quasi-static equivalent compressive load applied during the mechanical shock. Dynamic compressive limit has been calculated using the assumption of 2x dynamic amplification factor at processor location using a 600 gm heat sink and a 50 G table input. The product application can have flexibility in specific values, but the ultimate product of mass times acceleration times corresponding amplification factor should not exceed this dynamic compressive load limit. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement. This load is superimposed onto the socket static compressive load to obtain total dynamic load.
6. Board transient bent strain limits apply only to board manufacturing process steps such as ICT. It is not for substitute for shock and vibration. Maximum allowable strain at the socket BGA corners during transient loading events, such as slow displacement events, which might occur during board manufacturing, assembly, or testing. See the LGA3647-1 Board Flexure Initiative (BFI) Strain Guidance Sheet. Contact your manufacture Certified Quality Engineer (CQE) representative for this datasheet.
7. The minimum Total Static Compressive Load (BOL) specification only applies to the processor with fabric. The processor without fabric only requires that the minimum Total Static Compressive Load (EOL) be met over its lifetime (Only fabric processors are present in the first generation).

The minimum Static Total Compressive load will ensure socket reliability over the life of the product and that the contact resistance between the processor and the socket contacts meets the values outlined in the previous table.
3.4.12 **Socket Critical-to-Function Interfaces**

Critical-to-function (CTF) dimensions for the motherboard layout and the assembled components interface to the socket are identified in the socket drawing. All sockets manufactured must meet the specified CTF dimensions.

3.5 **Material and Recycling Requirements**

Cadmium should not be used in the painting or plating of the socket.

Chlorofluorocarbon Compounds (CFC) and Hydrofluorocarbon Compounds (HFC) should not be used in manufacturing the socket.

Components should comply with recycling standards (e.g., European Blue Angel), and must comply with environmental legislation including those related to restrictions on the use of lead and bromine containing flame-retardants. Legislation varies by geography; European Union (RoHS/WEEE), China, California, etc.

3.6 **LGA3647 Socket Land Pattern**

Solder balls enable the socket to be surface mounted to the processor board. Each contact will have a corresponding solder ball. Solder ball position may be at an offset with respect to the contact tip and base. Hexagonal area array ball-out increases contact density by 12% while maintaining 39 mil minimum via pitch requirements.

**Contact Pattern**

LGA3647-0 socket contacts are in 1.0 mm (0.039”) hexagonal pitch in a 105 x 43 grid array with depopulated section in the center of the array and selective depopulation elsewhere. See the socket drawing for details. The tips of the contacts will extend beyond the surface of the socket to make contact with the pads located at the bottom of the processor package.

**BGA Pattern**

The land pattern for the LGA3647 socket is a 39 mil hexagonal array. For CTF joints, the pad size will primarily be a circular Metal Defined (MD) pad and these pads should be designated as a critical dimension to the PCB vendors with a 17 mil ±1 mil tolerance. Some CTF pads will have an SMD pad (20 x 17 mil).
3.7 Strain Guidance for Socket

Intel provides manufacturing strain guidance commonly referred to as Board Flexure Initiative or BFI Strain Guidance. The BFI strain guidance applies only to transient bend conditions seen in a board manufacturing assembly environment, for example during in circuit test. BFI strain guidance limits do not apply once PHM is installed. It should be noted that any strain metrology is sensitive to boundary conditions. Intel recommends the use of BFI to prevent solder joint defects from occurring in the test process. For additional guidance on BFI, see Manufacturing With Intel® Components - Strain Measurement for Circuit Board Assembly, also referred as BFI Manufacturing Advantage Services (MAS) and BFI Strain Guidance Sheet (LGA3647-0 Socket). Consult your Intel Customer Quality Engineer for additional guidance in setting up a BFI program in your factory.

Note: When the PHM is installed onto the board, the boundary conditions change, and the BFI strain limits are not applicable. The PHM, by design, increases stiffness in and around the socket and places the solder joints in compression. Intel does not support strain metrology with the ILM assembled.
This section describes the mechanical specification of a processor and socket loading mechanism, and design considerations. This specifications applies to the processor loading mechanism in maintaining its interface with the socket and encompasses the processor thermal solution and its retention mechanism.

Any thermal mechanical design using some of the reference components in combination with any other thermal mechanical solution needs to be fully validated according to the customer criteria. Also, if customer thermal mechanical validation criteria differ from the Intel criteria the reference solution should be validated against the customer criteria.

### 4.1 Mechanical Load Specification

The processor heatsink module is designed to achieve the minimum socket static pre-load compressive load specification. The minimum static pre-load compressive load is the force provided by the PHM and should be sufficient for rudimentary continuity testing of the socket and/or board. This load value will not ensure normal operation throughout the life of the product.

PHM should apply additional load to achieve the socket static total compressive load. The heatsink load will be applied to the Integrated Heat Spreader (IHS).

Table 4-1 provides load specifications for the PHM. The maximum limits should not be exceeded during assembly, shipping conditions, or standard use condition. Exceeding these limits may result in component failure. The socket body or the processor substrate should not be used as a mechanical reference or load-bearing surface for the thermal solution.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Compressive Load</td>
<td>890 N [200 lbf]</td>
<td>1334 N [300 lbf]</td>
<td>1, 2, 4</td>
</tr>
<tr>
<td>Dynamic Load</td>
<td>NA</td>
<td>588N [132 lbf]</td>
<td>1, 3</td>
</tr>
<tr>
<td>Heatsink Mass</td>
<td>NA</td>
<td>600 g [1.32lb]</td>
<td></td>
</tr>
<tr>
<td>TIM2 Activation Pressure</td>
<td>137.9 kpa [20 psi]</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

1. These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
2. These load limits define load limits at the Beginning Of Life (BOL) for the Intel’s reference enabling solution to meet the socket End of Life (EOL) loading requirement. PHM load may be different for custom designs. Intel will validate only the stated load distribution. The customer bears the responsibility of verifying the PHM load to ensure compliance with the package and socket loading as well as validating the socket reliability within their system implementation.
3. Dynamic loading is defined as heatsink mass (0.6 kg) x 50g load superimposed for an 11 ms duration average on the static load requirement.
4. Conditions must be satisfied at the Beginning Of Life (BOL), and the loading system stiffness for non-reference designs need to meet a specific stiffness range to satisfy end of life loading requirements.
4.2 Mechanical Design Considerations

A retention/loading mechanism must be designed to support the heatsink because there are no features on the socket on which to directly attach a heatsink. In addition to holding the heatsink in place on top of the IHS, this mechanism plays a significant role in the performance of the system, in particular:

- Ensuring thermal performance of the TIM applied between the IHS and the heatsink. TIMs, especially those based on phase change materials, are very sensitive to applied pressure: the higher the pressure, the better the initial performance. TIMs such as thermal greases are not as sensitive to applied pressure. Designs should consider the possible decrease in applied pressure over time due to potential structural relaxation in enabled components.

- Ensuring system electrical, thermal, and structural integrity under shock and vibration events, particularly the socket solder joints. The mechanical requirements of the attachment mechanism depend on the weight of the heatsink and the level of shock and vibration that the system must support. The overall structural design of the baseboard and system must be considered when designing the heatsink attachment mechanism. Their design should provide a means for protecting socket solder joints, as well as preventing package pullout from the socket.

**Note:**
The load applied by the attachment mechanism and the heatsink must comply with the package specifications, along with the dynamic load added by the mechanical shock and vibration requirements.

**Note:**
The load applied by the attachment mechanism must comply with the processor mechanical specifications, along with the dynamic load added by the mechanical shock and vibration requirements.

A potential mechanical solution for heavy heatsinks is the use of a supporting mechanism such as a backer plate or the utilization of a direct attachment of the heatsink to the chassis pan. In these cases, the strength of the supporting component can be utilized rather than solely relying on the baseboard strength. In addition to the previous general guidelines given, contact with the baseboard surfaces should be minimized during installation to avoid any damage to the baseboard.

Placement of board-to-chassis mounting holes also impacts board deflection and resultant socket solder ball stress. Customers need to assess the shock for their designs as heatsink retention (backplate), heatsink mass, and chassis mounting holes may vary.
5 Processor Thermal Management

Processor thermal management features and specifications are defined to ensure processor performance optimization within the targeted system and the processor thermal environmental conditions. The system and components thermal architects need to ensure compliance with the processor thermal specifications. Compromising processor thermal requirements will impact the processor performance and reliability.

5.1 Processor Thermal Features

5.1.1 TCC Activation Temperature

The processor has a software readable field in the TEMPERATURE_TARGET register that contains the minimum temperature at which the Thermal Control Circuit (TCC) will be activated and PROCHOT_N will be asserted. The TCC activation temperature is calibrated on a part-by-part basis and normal factory variation may result in the actual TCC activation temperature being higher than the value listed in the register.

TCC activation temperatures may change based on processor stepping, frequency or manufacturing efficiencies. Consult the Second Generation Intel® Xeon® Scalable Processors Datasheet Volume Two: Registers, document number 338846, for more information about this register.

Use of software that reports absolute temperature could be misleading since TCC activation temperature varies from part-to-part.

5.1.2 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology is a feature available on certain Second Generation Intel® Xeon® Scalable Processor SKUs that opportunistically and automatically allows the processor to run faster than the marked frequency if all of the following conditions are met:

1. Processor operating at base frequency (that is, P1 P-state)
2. Power management not active (that is, not throttling)
3. Processor operating below its temperature limit (that is, DTS < 0)
4. Processor operating below its power and current limits (that is, < TDP and <ICC_MAX). Refer to Section 5.3.2, “Fan Speed Control” for more information.

With Intel® Turbo Boost Technology enabled, the instantaneous processor power can exceed TDP for short durations resulting in increased performance.

System thermal design should consider the following important parameters (set via the BIOS).

- **POWER_LIMIT_1 (PL1) =** Average processor power over a long time window (default setting is TDP)
- **POWER_LIMIT_2 (PL2) =** Average processor power over a short time window above TDP (short excursions). Maximum allowed by the processor is 20% above TDP for all SKUs (1.2 * TDP).
**Note:** The actual power will include IMON inaccuracy.

- **POWER_LIMIT_1_TIME (Tau)** = Time constant for the exponential weighted moving average (EWMA) which optimizes performance while reducing thermal risk (dictates how quickly power decays from its peak)

**Note:** Although the processor can exceed PL1 (default TDP) for a certain amount of time, the Exponential Weighted Moving Average (EWMA) power will never exceed PL1.

A properly designed processor thermal solution is important to maximizing Intel® Turbo Boost Technology performance. However, heatsink performance ($\psi_{CA}$) is only one of several factors that can impact the amount of benefit. Other factors are the operating environment, workload, and system design. Intel® Turbo Boost Technology performance is also constrained by ICC and VCC limits. With Intel® Turbo Mode Technology enabled, the processor may run more consistently at higher power levels (but still within TDP), and be more likely at temperatures above $T_{CONTROL}$, as compared to when Intel® Turbo Mode Technology is disabled. This may result in higher acoustics.

### 5.1.3 Thermal Management

Second Generation Intel® Xeon® Scalable Processor SKUs require careful monitoring and control of temperatures on multiple silicon dies inside the package. The case temperature of multi-die SKUs is defined as the temperature measured at various locations on the surface of the Integrated Heat Spreader (IHS) above these components. Component thermal solution designers may utilize IHS power gradient at the core locations to optimize the processor cooling solution or to verify the thermal solution capability in meeting the processor thermal requirement. To allow optimal operation and long-term reliability of Intel processor-based systems, the processor must remain between the minimum and maximum case temperature ($T_{CASE}$) specifications as defined in the tables in the following sub-sections. Thermal solutions not designed to provide sufficient thermal cooling may affect the long-term reliability of the processor and system. Thermal profiles ensure adherence to Intel reliability requirements.

Intel assumes system boundary conditions (system ambient, airflow, heatsink performance/pressure drop, preheat, etc.) for each processor SKU. For servers, each processor will be aligned to either 1U or 2U system boundary conditions. Implementing a thermal solution that violates the thermal profile for extended periods of time may result in permanent damage to the processor or reduced life. The upper point of the thermal profile consists of the Thermal Design Power (TDP) and the corresponding $T_{CASE \_MAX}$ value ($x = TDP$ and $y = T_{CASE \_MAX}$) represents a thermal solution design point.

For embedded servers, communications, and storage markets, Intel has SKUs that support thermal profiles with nominal and short-term conditions designed to meet NEBS Level 3 compliance. For these SKUs, operation at either the nominal or short-term thermal profiles should result in virtually no TCC activation. Thermal profiles for these SKUs are found in this chapter as well.

Second Generation Intel® Xeon® Scalable Processors implements a methodology for managing processor temperatures that is intended to support acoustic noise reduction through fan speed control and to assure processor reliability. Selection of the appropriate fan speed is based on the relative temperature data reported by the processor’s Platform Environment Control Interface (PECI) as described in the Electrical EDS.
If the DTS value is less than \( T_{\text{CONTROL}} \) then the case temperature is permitted to exceed the thermal profile, but the DTS value must remain at or below \( T_{\text{CONTROL}} \).

For \( T_{\text{CASE}} \) implementations, if DTS is greater than \( T_{\text{CONTROL}} \), then the case temperature must meet the \( T_{\text{CASE}} \) based thermal profiles.

For DTS implementations:
- The \( T_{\text{CASE}} \) thermal profile can be ignored during processor run time.
- If DTS is greater than \( T_{\text{CONTROL}} \), then follow the DTS thermal profile specifications for fan speed optimization.

The temperature reported over PECI is always a negative value and represents a delta below the onset of Thermal Control Circuit (TCC) activation, as indicated by PROCHOT_N (see the Electrical Specification section of the EDS). Systems that implement fan speed control must be designed to use this data. Systems that do not alter the fan speed need to guarantee the case temperature meets the thermal profile specifications.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it is immeasurable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss, and in some cases may exceed the specified maximum temperature which affects the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously.

\((x = \text{TDP and } y = T_{\text{CASE_MAX @ TDP}})\) represents a thermal solution design point. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP). The adaptive thermal monitor feature is intended to help protect the processor in the event that an application exceeds the TDP recommendation for a sustained time period. To ensure maximum flexibility for future requirements, systems should be designed to the Flexible Motherboard (FMB) guidelines, even if a processor with lower power dissipation is currently planned. The adaptive thermal monitor feature must be enabled for the processor to remain within its specifications.

### 5.2 Processor Thermal Specifications

The processor requires a thermal solution to maintain temperatures within operating limits. Any attempt to operate the processor outside these limits may result in permanent damage to the processor and potentially other components within the system. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor IHS. Typical system level thermal solutions may consist of system fans combined with ducting and venting.
5.2.1 **T\textsubscript{CASE} and DTS Thermal Specifications**

The T\textsubscript{CASE} thermal based specifications are used for heatsink sizing while DTS based specifications are used for acoustic and fan speed optimizations. The Digital Thermal Sensor (DTS) reports a relative die temperature as an offset from TCC activation temperature. SKUs may share T\textsubscript{CASE} thermal profiles, but they will have separate DTS based thermal profiles.

5.2.1.1 **T\textsubscript{CASE} Thermal Profile**

For a single die processor package or non-MCP, all thermal profiles, whether based on T\textsubscript{CASE} or DTS, follow the straight-line equation format namely, \( y = mx + b \). Where,

- \( y \) = temperature (T) in °C
- \( m \) = slope \((\Psi_{CA})\) (CA = Case to ambient)
- \( x \) = power (P) in Watts
- \( b \) = y-intercept \((T_{LA})\) (LA = local ambient)

**Figure 5-1. Typical Thermal Profile Graph (Illustration Only)**

*Note:* There is no one-to-one correlation between T\textsubscript{CASE} and DTS. The T\textsubscript{CASE} specification exists to ensure that, when the T\textsubscript{CASE} margin is 0 °C, the DTS reading should be at or below DTS\_Max (thermal throttle) for virtually all server processors. Variation in the DTS margin is normal and results from several factors including DTS accuracy, thermal stack up variance, actual power under a TDP load, etc. The T\textsubscript{CASE} and DTS thermal profiles are expected to account for these variables.

The only way to accurately determine T\textsubscript{CASE} is to measure it with a thermocouple. The T\textsubscript{CASE} thermal profile specification is primarily for thermal solution sizing to ensure that virtually all processors within a particular SKU will operate with little to no thermal throttle. The DTS thermal profile provides a real time metric for FSC and acoustics, and to ensure performance and reliability. As long as a thermal solution meets the T\textsubscript{CASE} thermal profile specification, it is expected to support part-to-part variation in the DTS margin.
<table>
<thead>
<tr>
<th>Processor Brand String</th>
<th>TDP (W)</th>
<th>Core Count</th>
<th>Frequency (GHz)</th>
<th>Die</th>
<th>Heatsink Form Factor</th>
<th>System Form Factor</th>
<th>C1E Offset Disable8</th>
<th>TCONTROL (OC)</th>
<th>TCASE Max (°C)</th>
<th>DTS Max (°C)</th>
<th>Smiling Pond Correction Factor (°C/W)</th>
<th>Stepping</th>
<th>Sample Type</th>
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<tbody>
<tr>
<td>Intel® Xeon® Platinum 8280 CPU</td>
<td>205</td>
<td>28</td>
<td>2.7</td>
<td>XCC</td>
<td>2U</td>
<td>Spread Core</td>
<td>0</td>
<td>10</td>
<td>0.180*P]+47</td>
<td>[0.263*P]+47</td>
<td>84</td>
<td>101</td>
<td>0 B1 Revenue</td>
</tr>
<tr>
<td>Intel® Xeon® Platinum 8270 CPU</td>
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<td>2.7</td>
<td>XCC</td>
<td>2U</td>
<td>Spread Core</td>
<td>0</td>
<td>10</td>
<td>0.180*P]+47</td>
<td>[0.278*P]+47</td>
<td>84</td>
<td>104</td>
<td>0 B1 Revenue</td>
</tr>
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<td>XCC</td>
<td>2U</td>
<td>Spread Core</td>
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<td>10</td>
<td>0.180*P]+47</td>
<td>[0.278*P]+47</td>
<td>84</td>
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<td>XCC</td>
<td>2U</td>
<td>Spread Core</td>
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<td>XCC</td>
<td>2U</td>
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<td>XCC</td>
<td>1U</td>
<td>Spread Core</td>
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<td>10</td>
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<td>1U</td>
<td>Spread Core</td>
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<td>10</td>
<td>0.261*P]+47</td>
<td>[0.345*P]+47</td>
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<td>104</td>
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<td>10</td>
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<td>90</td>
<td>104</td>
<td>0.006 B1 Revenue</td>
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<td>XCC</td>
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<td>Spread Core</td>
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<td>10</td>
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<td>100</td>
<td>0.0036 B1 Revenue</td>
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<td>1U</td>
<td>Spread Core</td>
<td>0</td>
<td>10</td>
<td>0.260*P]+47</td>
<td>[0.340*P]+47</td>
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<td>98</td>
<td>0.0047 B1 Revenue</td>
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<td>Spread Core</td>
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<td>10</td>
<td>0.260*P]+47</td>
<td>[0.353*P]+47</td>
<td>86</td>
<td>100</td>
<td>0.0036 B1 Revenue</td>
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<td>XCC</td>
<td>1U</td>
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<td>10</td>
<td>0.253*P]+47</td>
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<td>100</td>
<td>0.0025 B1 Revenue</td>
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<td>XCC</td>
<td>1U</td>
<td>Spread Core</td>
<td>0</td>
<td>10</td>
<td>0.253*P]+47</td>
<td>[0.367*P]+47</td>
<td>85</td>
<td>102</td>
<td>0.002 B1 Revenue</td>
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<td>XCC</td>
<td>1U</td>
<td>Spread Core</td>
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<td>10</td>
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<td>XCC</td>
<td>1U</td>
<td>Spread Core</td>
<td>0</td>
<td>10</td>
<td>0.248*P]+46</td>
<td>[0.514*P]+46</td>
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<td>1U</td>
<td>Spread Core</td>
<td>0</td>
<td>10</td>
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<td>Spread Core</td>
<td>0</td>
<td>10</td>
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<td>102</td>
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<td>XCC</td>
<td>1U</td>
<td>Spread Core</td>
<td>0</td>
<td>10</td>
<td>0.256*P]+55</td>
<td>[0.336*P]+55</td>
<td>87</td>
<td>97</td>
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<td>2.1</td>
<td>XCC</td>
<td>1U</td>
<td>Shadow Core</td>
<td>0</td>
<td>10</td>
<td>0.256*P]+55</td>
<td>[0.336*P]+55</td>
<td>87</td>
<td>97</td>
<td>0.0040 B1 Revenue</td>
</tr>
<tr>
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<td>Shadow Core</td>
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<td>10</td>
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<td>[0.344*P]+55</td>
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<td>98</td>
<td>0.00142 B1 Revenue</td>
<td></td>
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<td>1U</td>
<td>Shadow Core</td>
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<td>10</td>
<td>0.256*P]+55</td>
<td>[0.344*P]+55</td>
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<td>98</td>
<td>0.0018 B1 Revenue</td>
<td></td>
</tr>
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<td>XCC</td>
<td>1U</td>
<td>Shadow Core</td>
<td>0</td>
<td>10</td>
<td>0.256*P]+55</td>
<td>[0.344*P]+55</td>
<td>87</td>
<td>98</td>
<td>0.0014 B1 Revenue</td>
<td></td>
</tr>
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<td>XCC</td>
<td>1U</td>
<td>Spread Core</td>
<td>0</td>
<td>10</td>
<td>0.248*P]+55</td>
<td>[0.360*P]+55</td>
<td>86</td>
<td>100</td>
<td>-0.0018 B1 Revenue</td>
</tr>
<tr>
<td>Intel® Xeon® Gold 6222V CPU</td>
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<td>XCC</td>
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<td>Spread Core</td>
<td>0</td>
<td>10</td>
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<td>[0.487*P]+46</td>
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<td>0.031 L1 Revenue</td>
</tr>
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Table 5-1. Second Generation Intel® Xeon® Scalable Processors Non-MCP SKU Thermal Specifications

<table>
<thead>
<tr>
<th>Processor Brand String</th>
<th>TDP (W)</th>
<th>Core Count</th>
<th>Frequency (GHz)</th>
<th>Die</th>
<th>Heatsink Form Factor</th>
<th>System Form Factor</th>
<th>C1E Offset Disable</th>
<th>TCONTROL (°C)</th>
<th>TCASE (°C)</th>
<th>DTS (°C)</th>
<th>TCASE_MAX (°C)</th>
<th>DTS_MAX (°C)</th>
<th>Thermal Profiles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® Xeon® Gold 5220</td>
<td>125</td>
<td>18</td>
<td>2.2</td>
<td>HCC</td>
<td>1U Shadow Core</td>
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<td>10</td>
<td>[0.256*P]+55</td>
<td>87</td>
<td>102</td>
<td>0.005</td>
<td>L1</td>
<td>Revenue</td>
</tr>
<tr>
<td>Intel® Xeon® Gold 5218B</td>
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<td>10</td>
<td>2.5</td>
<td>HCC</td>
<td>1U Shadow Core</td>
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<td>10</td>
<td>[0.282*P]+53</td>
<td>77</td>
<td>93</td>
<td>0.0281</td>
<td>L1</td>
<td>Revenue</td>
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<tr>
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<td>10</td>
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<td>HCC</td>
<td>1U Shadow Core</td>
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<td>[0.270*P]+52</td>
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<td>0.0175</td>
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<td>Revenue</td>
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<td>HCC</td>
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<td>10</td>
<td>[0.282*P]+53</td>
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<td>90</td>
<td>0.0291</td>
<td>L1</td>
<td>Revenue</td>
</tr>
<tr>
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<td>10</td>
<td>2.2</td>
<td>HCC</td>
<td>1U Shadow Core</td>
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<td>10</td>
<td>[0.282*P]+53</td>
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<td>88</td>
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<td>Revenue</td>
</tr>
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<td>2.1</td>
<td>LCC</td>
<td>1U Shadow Core</td>
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<td>10</td>
<td>[0.282*P]+54</td>
<td>78</td>
<td>90</td>
<td>0.0429</td>
<td>R1</td>
<td>Revenue</td>
</tr>
</tbody>
</table>

Notes:
1. Second Generation Intel® Xeon® Scalable Processors Gold –N and –S processors have been optimized for use in some networking and storage applications. The workload (TDP) assumed for maintaining the marked frequency (also called P1) is an average across the SPECint_rate2006 benchmark suite. Note that the SPECint_rate2006 benchmark is composed of 12 different sub-benchmarks. Second Generation Intel® Xeon® Scalable Processors Gold –N and –S processors assume a less intensive core workload for the TDP operating point.

This new family of application optimized SKUs may not maintain their marked frequency while running some standard server workloads (SPECint*, SPECfp*, or POVRAY* for example). Throttling can occur even if there is thermal margin to TCASE_MAX as TDP is enforced by the Power Control Unit (PCU).

Intel recommends potential customers do performance testing using existing platforms before committing to a design using these new processors and avoid relying on previous experience and frequency scaling projections to estimate expected performance.

Table 5-2. Second Generation Intel® Xeon® Scalable Processors High Frequency Thermal Specifications

<table>
<thead>
<tr>
<th>Processor Brand String</th>
<th>TDP (W)</th>
<th>Core Count</th>
<th>Frequency (GHz)</th>
<th>Die</th>
<th>Heatsink Form Factor</th>
<th>System Form Factor</th>
<th>C1E Offset Disable</th>
<th>TCONTROL (°C)</th>
<th>TCASE (°C)</th>
<th>DTS (°C)</th>
<th>TCASE_MAX (°C)</th>
<th>DTS_MAX (°C)</th>
<th>Thermal Profiles</th>
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<td>Unique</td>
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<td>[0.132*P]+37</td>
<td>64</td>
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<td>B1</td>
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<tr>
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<td>8</td>
<td>3.9</td>
<td>XCC</td>
<td>Unique</td>
<td>Unique</td>
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<td>[0.124*P]+37</td>
<td>60</td>
<td>95</td>
<td>0.0075</td>
<td>B1</td>
<td>Revenue</td>
</tr>
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</table>
**Table 5-3. Second Generation Intel® Xeon® Scalable Processors Refresh Non-MCP SKU Thermal Specifications**

<table>
<thead>
<tr>
<th>Processor Brand String</th>
<th>TDP (W)</th>
<th>Core Count</th>
<th>Frequency (GHz)</th>
<th>Die</th>
<th>Heatsink</th>
<th>Form Factor</th>
<th>System Form Factor</th>
<th>CIE Offset Disable</th>
<th>T_CONTROL (ºC)</th>
<th>Thermal Profiles</th>
<th>DTS (ºC)</th>
<th>T_MAX (ºC)</th>
<th>Smiling Pond Correction Factor (ºC/W)</th>
<th>Stepping</th>
<th>Sample Type</th>
</tr>
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<tr>
<td>Intel® Xeon® Platinum 8279W CPU</td>
<td>205</td>
<td>28</td>
<td>2.5</td>
<td>XCC</td>
<td>WS</td>
<td>2S-WS</td>
<td>0</td>
<td>10</td>
<td>[0.166*P]+42</td>
<td>[0.249*P]+42</td>
<td>76</td>
<td>93</td>
<td>-0.001</td>
<td>B1</td>
<td>Revenue</td>
</tr>
<tr>
<td>Intel® Xeon® Platinum 8267W CPU</td>
<td>205</td>
<td>24</td>
<td>2.7</td>
<td>XCC</td>
<td>WS</td>
<td>2S-WS</td>
<td>0</td>
<td>10</td>
<td>[0.176*P]+42</td>
<td>[0.268*P]+42</td>
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<td>97</td>
<td>0.008</td>
<td>B1</td>
<td>Revenue</td>
</tr>
<tr>
<td>Intel® Xeon® Gold 6253W CPU</td>
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<td>18</td>
<td>3.1</td>
<td>XCC</td>
<td>WS</td>
<td>2S-WS</td>
<td>0</td>
<td>10</td>
<td>[0.170*P]+42</td>
<td>[0.280*P]+42</td>
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<td>98</td>
<td>0.001</td>
<td>B1</td>
<td>Revenue</td>
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<tr>
<td>Intel® Xeon® Gold 6245W CPU</td>
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<td>3.3</td>
<td>XCC</td>
<td>WS</td>
<td>2S-WS</td>
<td>0</td>
<td>10</td>
<td>[0.167*P]+42</td>
<td>[0.306*P]+42</td>
<td>72</td>
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<td>Revenue</td>
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<td>XCC</td>
<td>WS</td>
<td>2S-WS</td>
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<td>101</td>
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<td>WS</td>
<td>2S-WS</td>
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<td>0.001</td>
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<td>8</td>
<td>3.5</td>
<td>XCC</td>
<td>WS</td>
<td>2S-WS</td>
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<td>10</td>
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<td>97</td>
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<td>Revenue</td>
</tr>
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<td>Intel® Xeon® Gold 5220R</td>
<td>125</td>
<td>18</td>
<td>2.2</td>
<td>HCC</td>
<td>1U Shadow Core</td>
<td>0</td>
<td>10</td>
<td>[0.256*P]+55</td>
<td>[0.376*P]+55</td>
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<td>102</td>
<td>0.005</td>
<td>L1</td>
<td>Revenue</td>
<td></td>
</tr>
<tr>
<td>Intel® Xeon® Gold 5218R</td>
<td>16</td>
<td>2.3</td>
<td>HCC</td>
<td>1U Shadow Core</td>
<td>0</td>
<td>10</td>
<td>[0.256*P]+55</td>
<td>[0.376*P]+55</td>
<td>87</td>
<td>102</td>
<td>0.008</td>
<td>L1</td>
<td>Revenue</td>
<td></td>
<td></td>
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<tr>
<td>Intel® Xeon® Gold 5215R</td>
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<td>10</td>
<td>2.7</td>
<td>HCC</td>
<td>1U Shadow Core</td>
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<td>10</td>
<td>[0.280*P]+52</td>
<td>[0.470*P]+52</td>
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<td>99</td>
<td>0.028</td>
<td>L1</td>
<td>Revenue</td>
<td></td>
</tr>
<tr>
<td>Intel® Xeon® Silver 4216R</td>
<td>125</td>
<td>16</td>
<td>2.3</td>
<td>HCC</td>
<td>1U Shadow Core</td>
<td>0</td>
<td>10</td>
<td>[0.256*P]+55</td>
<td>[0.376*P]+55</td>
<td>87</td>
<td>102</td>
<td>0.008</td>
<td>L1</td>
<td>Revenue</td>
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</tr>
<tr>
<td>Intel® Xeon® Silver 4214R</td>
<td>100</td>
<td>12</td>
<td>2.5</td>
<td>HCC</td>
<td>1U Shadow Core</td>
<td>0</td>
<td>10</td>
<td>[0.270*P]+52</td>
<td>[0.420*P]+52</td>
<td>79</td>
<td>94</td>
<td>0.026</td>
<td>L1</td>
<td>Revenue</td>
<td></td>
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<tr>
<td>Intel® Xeon® Gold 4213W CPU</td>
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<td>16</td>
<td>3.0</td>
<td>HCC</td>
<td>1U Spread Core</td>
<td>0</td>
<td>10</td>
<td>[0.256*P]+55</td>
<td>[0.376*P]+55</td>
<td>84</td>
<td>98</td>
<td>0.031</td>
<td>L1</td>
<td>Revenue</td>
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<tr>
<td>Intel® Xeon® Gold 5219W</td>
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<td>18</td>
<td>2.2</td>
<td>HCC</td>
<td>1U Shadow Core</td>
<td>0</td>
<td>10</td>
<td>[0.256*P]+55</td>
<td>[0.376*P]+55</td>
<td>87</td>
<td>102</td>
<td>0.005</td>
<td>L1</td>
<td>Revenue</td>
<td></td>
</tr>
<tr>
<td>Intel® Xeon® Gold 5214W CPU</td>
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<td>16</td>
<td>2.3</td>
<td>HCC</td>
<td>1U Shadow Core</td>
<td>0</td>
<td>10</td>
<td>[0.256*P]+55</td>
<td>[0.376*P]+55</td>
<td>87</td>
<td>102</td>
<td>0.008</td>
<td>L1</td>
<td>Revenue</td>
<td></td>
</tr>
<tr>
<td>Intel® Xeon® Gold 5213W CPU</td>
<td>100</td>
<td>10</td>
<td>2.7</td>
<td>HCC</td>
<td>1U Shadow Core</td>
<td>0</td>
<td>10</td>
<td>[0.280*P]+52</td>
<td>[0.470*P]+52</td>
<td>80</td>
<td>99</td>
<td>0.028</td>
<td>L1</td>
<td>Revenue</td>
<td></td>
</tr>
<tr>
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<td>12</td>
<td>2.5</td>
<td>HCC</td>
<td>1U Shadow Core</td>
<td>0</td>
<td>10</td>
<td>[0.270*P]+52</td>
<td>[0.420*P]+52</td>
<td>79</td>
<td>94</td>
<td>0.026</td>
<td>L1</td>
<td>Revenue</td>
<td></td>
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<td>10</td>
<td>2.5</td>
<td>LCC</td>
<td>1U Shadow Core</td>
<td>0</td>
<td>10</td>
<td>[0.280*P]+56</td>
<td>[0.420*P]+56</td>
<td>84</td>
<td>98</td>
<td>0.042</td>
<td>R1</td>
<td>Revenue</td>
<td></td>
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<tr>
<td>Intel® Xeon® Silver 4208R</td>
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<td>8</td>
<td>2.3</td>
<td>LCC</td>
<td>1U Shadow Core</td>
<td>0</td>
<td>10</td>
<td>[0.280*P]+56</td>
<td>[0.430*P]+56</td>
<td>84</td>
<td>99</td>
<td>0.040</td>
<td>R1</td>
<td>Revenue</td>
<td></td>
</tr>
<tr>
<td>Intel® Xeon® Silver 3206R</td>
<td>85</td>
<td>8</td>
<td>2.1</td>
<td>LCC</td>
<td>1U Shadow Core</td>
<td>0</td>
<td>10</td>
<td>[0.282*P]+54</td>
<td>[0.424*P]+54</td>
<td>78</td>
<td>90</td>
<td>0.039</td>
<td>R1</td>
<td>Revenue</td>
<td></td>
</tr>
</tbody>
</table>
5.2.2 Intel® Speed Select Technology (Intel® SST) on Second Generation Intel® Xeon® Scalable Processors

Intel® Speed Select Technology (Intel® SST) is a feature that provides flexibility and configurability of the desired base performance. It has the capability to configure the CPU to run at three distinct operating points:

- Each operating point defined by a combination of core count/base frequency/TDP/Tj

Static Boot Time Configuration:
- The BIOS discovers and configures the operating point at boot.

Key Value Prop:
- Multiple CPU personalities based on workload/VM needs
- Improved server utilization in data center
- Improved guaranteed performance SLAs

Figure 5-2. Intel® Speed Select Technology (Intel® ISS)

Note: Frequency and core count for illustration only.
5.2.2.1 Benefits of Flexible CPU Configuration - Example

- Cloud customer has three distinct products with different hardware configurations.
- Targets 50%+ utilization to accommodate fluctuations in demand/uncertainty on customer product choice.
- By consolidating three hardware configurations to single flexible SKU, the CSP can reduce the total number of system deployments and still meet the same demand/uncertainty profile.

\[
\delta Q = \sqrt{\delta a^2 + \delta b^2 + \delta c^2 + ... + \delta z^2}
\]

Propagation of Errors / Uncertainties

\(\delta x = \text{Spare Capacity (Uncertainty)}\)
5.2.2.2 Thermal and Fan Speed Control Considerations

DTS 2.0 is not available in Intel® Speed Select Technology configurations.

- DTS 2.0 thermal “Margin to Loadline” is available only for the base configuration.
- Same margin sensor reports “Margin to Tcontrol” for ISS configurations for fan speed control.

System power characterization must be done for all configurations as fan behavior might change among configurations.

“Margin to Throttle” is available on all configurations (Base and ISS configurations).

Figure 5-3. Examples of DTS 2.0 Based Thermal Margin on Base and ISS Configurations
Notes:
1. Used $T_{\text{CONTROL}}$ specification.
2. For these ISS SKUs, DTS 2.0 is supported only for the baseline configuration. For ISS and PBF configurations, DTS 2.0 is not supported. The sensor that reports margin to $DTS_{\text{2.0}}$ thermal profile will report margin to $T_{\text{CONTROL}}$ for fan speed control purposes.
3. Second Generation Intel® Xeon® Scalable Processors Gold –N and –S processors have been optimized for use in some networking and storage applications. The workload (TDP) assumed for maintaining the marked frequency (also called P1) is an average across the SPECint_rate2006 benchmark suite. Note that the SPECint_rate2006 benchmark is composed of 12 different sub-benchmarks. Second Generation Intel® Xeon® Scalable Processors Gold –N and –S processors assume a less intensive core workload for the TDP operating point.
   This new family of application optimized SKUs may not maintain their marked frequency while running some standard server workloads (SPECint*, SPECfp*, or POVRAY* for example). Throttling can occur even if there is thermal margin to $T_{\text{CASE, MAX}}$ as TDP is enforced by the Power Control Unit (PCU).
   Intel recommends potential customers do performance testing using existing platforms before committing to a design using these new processors and avoid relying on previous experience and frequency scaling projections to estimate expected performance.

Table 5-4. Second Generation Intel® Xeon® Scalable Processors - SP ISS Thermal Specifications

<table>
<thead>
<tr>
<th>Processor Number</th>
<th>Configuration</th>
<th>TDP (W)</th>
<th>Core Count</th>
<th>Frequency (GHz)</th>
<th>Die</th>
<th>Heatsink Form Factor</th>
<th>System Form Factor</th>
<th>C1E Offset Disable</th>
<th>T_{\text{CONTROL}} (OC)</th>
<th>Thermal Profiles</th>
<th>C1E Disable8</th>
<th>T_{\text{CASE, MAX}} (°C)</th>
<th>DTS_{\text{MAX}} (°C)</th>
<th>Smiling Pond Correction Factor (°C/W)</th>
<th>Stepping</th>
<th>Sample Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® Xeon® Gold</td>
<td>Baseline</td>
<td>150</td>
<td>18</td>
<td>2.6</td>
<td>XCC</td>
<td>2U</td>
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<td>5 [0.187*P]+46</td>
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<td>88</td>
<td>0.0026</td>
<td></td>
<td></td>
<td>B1</td>
<td>Revenue</td>
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<tr>
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<td>150</td>
<td>14</td>
<td>2.8</td>
<td>XCC</td>
<td>Spread Core</td>
<td>0</td>
<td>5 [0.187*P]+46</td>
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<tr>
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<td>150</td>
<td>8</td>
<td>3.1</td>
<td>XCC</td>
<td>Spread Core</td>
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<td>24</td>
<td>2.3</td>
<td>XCC</td>
<td>2U</td>
<td>Spread Core</td>
<td>0</td>
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<td>74</td>
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<td>16</td>
<td>2.1 [0.187*P]+46</td>
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<td>86</td>
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<td>2.3</td>
<td>XCC</td>
<td>1U</td>
<td>Spread Core</td>
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<td>89</td>
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<td>2.3</td>
<td>HCC</td>
<td>Shadowed</td>
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<td>8</td>
<td>2.4</td>
<td>HCC</td>
<td>Shadowed</td>
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<td>88</td>
<td>0.0291</td>
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<td>2.3</td>
<td>HCC</td>
<td>1U</td>
<td>Shadowed</td>
<td>0</td>
<td>10 [0.273*P]+53</td>
<td>83</td>
<td>94</td>
<td>0.018</td>
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<td>L1</td>
<td>Revenue</td>
</tr>
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<td>12</td>
<td>2.1 [0.273*P]+53</td>
<td>83</td>
<td>94</td>
<td>0.018</td>
<td></td>
<td></td>
<td>Note 1</td>
<td></td>
</tr>
</tbody>
</table>
5.2.2.3 **Non-MCP (10-Year Use + NEBS-Friendly) SKU Thermal Profiles**

Network Equipment Building System (NEBS) is the most common set of environmental design guidelines applied to telecommunications equipment. Non-MCP (10-year use + NEBS-friendly) SKU thermal profiles target operation at higher case temperatures and/or NEBS thermal profiles for embedded communications server and storage form factors. The term “embedded” is used to refer to those segments collectively. Thermal profiles in this section pertain only to those specific non-MCP (10-year use + NEBS-friendly) SKU thermal profiles.

The nominal thermal profile must be used for standard operating conditions or for products that do not require NEBS Level 3 compliance.

The short-term thermal profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 96 hours per instance, 360 hours per year, and a maximum of 15 instances per year, as intended by NEBS Level 3.

Operation at the short-term thermal profile for durations exceeding 360 hours per year violate the processor thermal specifications and may result in permanent damage to the processor.

Implementation of the defined thermal profile should result in virtually no TCC activation.

5.2.2.4 **NEBS T\text{CASE} Thermal Profile**

The NEBS thermal profiles help relieve thermal constraints for short-term NEBS conditions. To help with reliability, the processors must meet the nominal thermal profile under standard operating conditions and can only rise up to the short-term specification for the NEBS excursions. See the following thermal profile diagram.
Processor Thermal Management

5.2.2.5 NEBS T_{DTS} Thermal Profile

The thermal solution is expected to be developed in accordance with the T_{CASE} thermal profile. Operational compliance monitoring of thermal specifications and fan speed modulation may be done via the DTS based thermal profile.

These T_{DTS} profiles are fully defined by the simple linear equation: \( T_{DTS} = P S I_{PA} \times P + T_{LA} \)

Where:

- PSIPA is the processor-to-ambient thermal resistance of the processor thermal solution.
- TLA is the local ambient temperature for the nominal thermal profile.
- TLA-ST designates the local ambient temperature for short-term operation.
- P is the processor power dissipation.

Figure 5-5 illustrates the general form of the resulting linear graph resulting from \( T_{DTS} = P S I_{PA} \times P + T_{LA} \).

The slope of a DTS profile assumes full fan speed which is not required over much of the power range. \( T_{CONTROL} \) is the temperature above that fans must be at maximum speed to meet the thermal profile requirements. \( T_{CONTROL} \) is different for each SKU and
may be slightly above or below $T_{DTS-Max}$ of the DTS nominal thermal profile for a particular SKU. At many power levels on most non-MCP (10-year use + NEBS-friendly) SKU thermal profiles, temperatures of the nominal profile are less than $T_{CONTROL}$ as indicated by the blue shaded region in the DTS thermal profile in the following diagram. As a further simplification, operation at DTS temperatures up to $T_{CONTROL}$ is permitted at all power levels. Compliance to the DTS profile is required for any temperatures exceeding $T_{CONTROL}$.

Figure 5-5. NEBS DTS Thermal Profile
Table 5-5. Second Generation Intel® Xeon® Scalable Processors-SP_HT XCC Thermal Specs Update

<table>
<thead>
<tr>
<th>Processor number</th>
<th>TDP (W)</th>
<th>Die</th>
<th>Frequency (GHz)</th>
<th>Core Count</th>
<th>C1E Offset Disable</th>
<th>T_CONTROL</th>
<th>Nominal TCASE_MAX (°C)</th>
<th>Short Term TCASE_MAX (°C)</th>
<th>Nominal DTS_MAX (°C)</th>
<th>Short Term DTS_MAX (°C)</th>
<th>Correction Factor (°C/W)</th>
<th>Stepping</th>
<th>Sample Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® Xeon® Gold 6238T</td>
<td>125</td>
<td>XCC</td>
<td>1.9</td>
<td>22</td>
<td>0</td>
<td>20</td>
<td>0.208*P+52</td>
<td>0.208*P+67</td>
<td>0.296*P+52</td>
<td>0.296*P+67</td>
<td>93</td>
<td>104</td>
<td>78</td>
</tr>
<tr>
<td>Intel® Xeon® Gold 6230T</td>
<td>125</td>
<td>XCC</td>
<td>2.1</td>
<td>20</td>
<td>0</td>
<td>20</td>
<td>0.200*P+52</td>
<td>0.200*P+67</td>
<td>0.280*P+52</td>
<td>0.280*P+67</td>
<td>92</td>
<td>102</td>
<td>77</td>
</tr>
<tr>
<td>Intel® Xeon® Gold 5220T</td>
<td>105</td>
<td>XCC</td>
<td>1.9</td>
<td>18</td>
<td>0</td>
<td>20</td>
<td>0.248*P+52</td>
<td>0.248*P+67</td>
<td>0.333*P+52</td>
<td>0.333*P+67</td>
<td>93</td>
<td>102</td>
<td>78</td>
</tr>
<tr>
<td>Intel® Xeon® Gold 5218T</td>
<td>105</td>
<td>XCC</td>
<td>2.1</td>
<td>16</td>
<td>0</td>
<td>20</td>
<td>0.248*P+52</td>
<td>0.248*P+67</td>
<td>0.333*P+52</td>
<td>0.333*P+67</td>
<td>93</td>
<td>102</td>
<td>78</td>
</tr>
<tr>
<td>Intel® Xeon® Gold 4209T</td>
<td>70</td>
<td>LCC</td>
<td>2.2</td>
<td>8</td>
<td>0</td>
<td>20</td>
<td>0.343*P+52</td>
<td>0.343*P+67</td>
<td>0.500*P+52</td>
<td>0.500*P+67</td>
<td>91</td>
<td>102</td>
<td>76</td>
</tr>
</tbody>
</table>

Notes:
1. These values are specified at VccIN_MAX for all processor frequencies. Systems must be designed to ensure the processor is not subjected to any static Vcc and Icc combination wherein VccIN exceeds VccIN_MAX at a specified Icc. Refer to the electrical loadline specifications.
2. Thermal Design Power (TDP) should be used as a target for processor thermal solution design at maximum T_CASE. Processor power may exceed TDP for short durations.
3. These specifications are preliminary and will be updated as further characterization data becomes available.
4. Thermal specifications are based on a 12C rise above system ambient.
5. The nominal thermal profile must be used for all normal operating conditions or for products that do not require NEBS Level 3 compliance.
6. The short-term thermal profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 96 hours per instance, 360 hours per year, and a maximum of 15 instances per year, as compliant with NEBS Level 3. Operation at the short-term thermal profile for durations exceeding 360 hours per year violate the processor thermal specifications and may result in permanent damage to the processor.
7. The DTS2.0 does follow the nominal DTS thermal profile.
8. Disabling C1E will result in an automatic reduction of DTS_max so that the reliability is still protected. DTS_max will be reduced by the value shown "C1E Offset Disable". If thermal design has not been optimized to the reduced DTS_max value, throttling may occur. T_CONTROL is already an offset to DTS_max; therefore, the absolute temperature at which the T_CONTROL is reached will shift by the same amount. For example:

Thermtrip_abs C1E enabled = Thermtrip_abs C1E disabled

![Graph](image1)

![Graph](image2)
5.2.3 Thermal Metrology

5.2.3.1 Case Temperature Measurement

Processor die(s) may be off center under the Integrated Heat Spreader (IHS). The minimum and maximum case temperatures (TCASE) specified are measured on the topside of the IHS, where the center of the each die is located as shown in Figure 5-6. This figure also includes geometry guidance for modifying the IHS to accept a thermocouple probe.

Figure 5-6. Case Temperature (TCASE) Measurement Location

Note: Image shown here is for demonstration purposes and does not reflect final product. Refer to the mechanical drawings section for an accurate representation.

5.2.3.2 DTS 2.0 Based Thermal Margin

Processors covered in this document support DTS 2.0 based thermal margin. The intercept and slope terms from the DTS thermal profiles are stored in the processor. The processor calculates and reports the margin which may be read by PECI command RdPkgConfig(), Index 10; Or MSR 1A1h: PACKAGE_THERM_MARGIN[15:0]. Fan speed control algorithms simply read and react to the thermal margin register. The thermal margin offset may need to be used for real-time thermal specification compliance and power performance optimization during fan speed control. Larger thermal margin offset leads to more performance. Small thermal margin offset leads to lower fan speed and noise. The CPU package temperature is not allowed to exceed the DTS2.0 thermal specification all the time during fan speed control in normal system operating condition, which means thermal margin (MSR 1A1h) should maintain positive values all the time.

Note: The default value reported for DTS 2.0 thermal margin during bring up is 0, and this value may continue until the system is fully operational

Thermal Margin FSC = Thermal Margin (by PECI/MSR) – Thermal Margin Offset

Thermal Margin FSC < 0: Gap to thermal margin FSC specification, fan speed must increase
Thermal Margin FSC > 0: Margin to thermal margin FSC specification, fan speed may decrease
5.3 Processor Thermal Management Guidelines

5.3.1 Processor Thermal Solution Environmental Conditions

Processor heatsink design must comply with the $T_{\text{CASE}}$ based thermal profile. Systems that do not monitor the processor die temperature by monitoring the thermal sensor output must ensure processor cooling solution is capable of meeting the processor based $T_{\text{CASE}}$ specification. In some situations, implementation of DTS based thermal specification can reduce average fan power and improve acoustics as compared to the $T_{\text{CASE}}$ based thermal profile.

When all cores are active, a properly sized heatsink will be able to meet the processor thermal specification. When all cores are not active or when Intel® Turbo Boost Technology is active, attempting to comply with the DTS based thermal specification may drive system fans to increased speed. In such situations, the $T_{\text{CASE}}$ temperature will be below the $T_{\text{CASE}}$ based thermal profile by design.

Table 5-6 provides thermal boundary conditions and performance targets applied in defining the processor thermal specifications. These values serve as a guide for designing a process compatible thermal solution.
### Table 5-6. Thermal Boundary Conditions

<table>
<thead>
<tr>
<th>Heatsink Form Factor</th>
<th>Driving Form Factor</th>
<th>Thermal Specification Setting SKU Alignment</th>
<th>Airflow (CFM)</th>
<th>TLA for each TDP SKU (°C) (T_SYSTEM_AMBIENT = 35 °C)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Airflow (CFM)</td>
<td>45 (W)</td>
</tr>
<tr>
<td>1U High Performance</td>
<td>½ Width</td>
<td>SKUs ≤ 95W</td>
<td>11.6</td>
<td>47.1</td>
</tr>
<tr>
<td>1U High Performance</td>
<td>½ Width</td>
<td>95W ≤ SKUs ≤ 140W</td>
<td>11.6</td>
<td>--</td>
</tr>
<tr>
<td>1U Low Impedance</td>
<td>½ Width</td>
<td>SKUs ≤ 140W</td>
<td>11.6</td>
<td>40</td>
</tr>
<tr>
<td>1U High Performance</td>
<td>Spread-Core 1U Height</td>
<td>150W ≤ SKUs ≤ 165W</td>
<td>11.1</td>
<td>--</td>
</tr>
<tr>
<td>2U Passive High Performance</td>
<td>2U EEB or ½ Width 2U Height</td>
<td>150W ≤ SKUs ≤ 165W</td>
<td>21.5</td>
<td>--</td>
</tr>
<tr>
<td>1U High Performance</td>
<td>Spread-Core 1U Height</td>
<td>High Frequency SKUs ≤ 150W Only</td>
<td>11.1</td>
<td>43.2</td>
</tr>
<tr>
<td>2U Passive High Performance</td>
<td>Spread-Core 2U Height</td>
<td>High Frequency SKUs ≤ 165W Only</td>
<td>21.5</td>
<td>43.2</td>
</tr>
<tr>
<td>Workstation Tower Square Passive</td>
<td>Workstation</td>
<td>Workstation SKU Only</td>
<td>23.5</td>
<td>--</td>
</tr>
<tr>
<td>2U Passive High Performance</td>
<td>Spread-Core 2U Height</td>
<td>175W ≤ SKUs ≤ 205W</td>
<td>21.5</td>
<td>--</td>
</tr>
</tbody>
</table>

**Notes:**
1. Thermal Boundary Conditions (BC) based on test data
2. 1U narrow high performance HS is used for the rear CPU, and low impedance 1U narrow HS is used for the front CPU.
3. 1U low impedance heatsink intended to use for front processor of ½ width form factor
5.3.2 Fan Speed Control

Fan Speed Control (FSC) techniques to reduce system-level acoustic noise are a common practice in server designs. The fan speed is one of the parameters that determines the amount of airflow provided to the thermal solution. Additionally, airflow is proportional to a thermal solution’s performance, which consequently determines the $T_{\text{CASE}}$ of the processor at a given power level. Because the temperature of a processor is an important parameter in determining the long-term reliability of a processor, the FSC implemented in a system directly correlates to the processor’s ability to meet the thermal profile. For this purpose, the parameter called $T_{\text{CONTROL}}$, as explained in the EDS electrical specification, is to be used in FSC designs to ensure that the long-term reliability of the processor is met while keeping the system-level acoustic noise down.

When Digital Temperature Sensor (DTS) value is less than $T_{\text{CONTROL}}$, the thermal profile can be ignored. The DTS value is a relative temperature to PROCHOT which is the maximum allowable temperature before the thermal control circuit is activated. In this region, the DTS value can be utilized to not only ensure specification compliance but also to optimize fan speed control resulting in the lowest possible fan power and acoustics under any operating conditions. When DTS goes above $T_{\text{CONTROL}}$, fan speed must increase to bring the sensor temperature below $T_{\text{CONTROL}}$ or to ensure compliance with the thermal profile.

<table>
<thead>
<tr>
<th>Condition</th>
<th>FSC Scheme</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\text{DTS} \leq T_{\text{CONTROL}}$</td>
<td>FSC can adjust fan speed to maintain DTS $\leq T_{\text{CONTROL}}$ (low acoustic region).</td>
</tr>
<tr>
<td>$\text{DTS} &gt; T_{\text{CONTROL}}$</td>
<td>FSC should adjust fan speed to keep $T_{\text{CASE}}$ at or below the thermal profile specification (increased acoustic region).</td>
</tr>
</tbody>
</table>

The PECI temperature reading from the processor can be compared to this $T_{\text{CONTROL}}$ value. A fan speed control scheme can be implemented as described in the EDS electrical specification without compromising the long-term reliability of the processor.

The PECI command for DTS is GetTemp(). Though use of a sign bit, the value returned from PECI is negative.

The PECI command for $T_{\text{CONTROL}}$ is RdPkgConfig(), temperature target read, 15:8. The value returned from PECI is unsigned (positive); however, it is negative by definition.

There are many different ways of implementing fan speed control, including FSC based on processor ambient temperature, FSC based on processor Digital Thermal Sensor (DTS) temperature, or a combination of the two. If FSC is based only on the processor ambient temperature, low acoustic targets can be achieved under low ambient temperature conditions. However, the acoustics cannot be optimized based on the behavior of the processor temperature. If FSC is based only on the digital thermal sensor, sustained temperatures above $T_{\text{CONTROL}}$ drive fans to maximum RPM. If FSC is based both on the ambient and digital thermal sensor, ambient temperature can be used to scale the fan RPM controlled by the digital thermal sensor. This would result in an optimal acoustic performance. Regardless of which scheme is employed, system designers must ensure that the thermal profile specification is met.
5.3.3 Thermal Excursion Power

Under fan failure or other anomalous thermal excursions, processor temperature (either $T_{\text{CASE}}$ or DTS) may exceed the thermal profile for a duration totaling less than 360 hours per year without affecting long term reliability (life) of the processor. For more typical thermal excursions, the thermal monitor is expected to control the processor power level as long as conditions do not allow the processor to exceed the temperature at which Thermal Control Circuit (TCC) activation initially occurred.

Under more severe anomalous thermal excursions when the processor temperature cannot be controlled at or below thermal profile by TCC activation, then data integrity is not assured. At some higher thresholds, THERMTRIP_N will enable a shut down in an attempt to prevent permanent damage to the processor.
6 System Design Considerations

When designing a thermally capable system, all critical components must be simultaneously considered. The responsible engineer must determine how each component will affect another, while ensuring target performance for all components. The term “target performance” is used because some components (for example, LRDIMM) have better performance, depending on how well they are cooled. The system design team must set these target performance goals during the design phase so that they can be achieved with the selected component layout.

The location of components and their interaction must be considered during the layout phase. For example, memory that is heated by a processor will have worse performance than a layout that does not shadow memory behind a processor.

Although the memory components have fixed thermal specifications, the performance management of RDIMM will limit memory throughput to ensure that the temperature limits are met. Consequently, a poorly cooled memory subsystem will have worse performance. The processor is somewhat different in that it enables full performance at all times, as defined by its specifications. The thermal engineer’s responsibility is to ensure that each and every component meets its performance goals bounded by thermal and acoustic specifications but also computing performance such as memory throughput.

The thermal engineer directly influences the critical thermal parameters affecting processor cooling capability. For a given heatsink and retention solution, the layout and air-mover selection must ensure that all thermal specifications are met. It is desirable to drive chassis air temperature rise as low as reasonably possible while maximizing flow to each component. However, higher chassis temperature rise can be accommodated as long as the design implements a countering flow increase. These trade-offs are essential in designing a thermally capable system.

The number, size, and position of fans, vents, and other heat-generating components determine the component thermal performance and the resultant local ambient and airflow to the processor. The size and type (passive or active) of the thermal solution and the amount of system airflow can be traded off against each other to meet specific system design constraints.

In choosing the boundary conditions for a passive heatsink, the following methodology is recommended to ensure that a system can deliver the required boundary conditions. The Intel reference solution was developed by considering various system implementations to ensure that the boundary conditions were within reason.

- Conceptualize the layout with the system architect, including approximate volumetric constraints for the heatsink.
- Select air movers that will deliver airflow and local temperatures within reason to all system components (also account for $T_{RISE}$ across the air-movers).
- Create a Computational Fluid Dynamics (CFD) model of the system.
- Run the CFD model with varying flow resistance representing the finned section of the heatsink.
- Extract an effective air-mover curve from the CFD results.
- Optimize the heatsink (fin thickness, quantity, base thickness, and so on) based on the effective air-mover curve.
• Determine whether that optimized thermal solution can meet processor specifications.
• Iterate through the previous steps to find a solution that will meet thermal requirements.

To develop a reliable and cost-effective thermal solution, thermal characterization and simulation should be carried out at the entire system level, accounting for the thermal requirements of each component. In addition, acoustic noise constraints may limit the size, number, placement, and types of air-movers that can be used in a particular design. A number of collaterals, such as thermal and mechanical models, are made available to aid in performing system and component level thermal characterizations. See Table 1-1 for the listing of available collaterals.

6.1 PCB Design Consideration

6.1.1 Allowable Board Thickness

The components described in this document (namely retention mechanism, backplate and the heatsink) will support board thickness in the range of 1.6 - 2.36 mm (0.063"-0.093") and 2.36 - 3.3 mm (0.093" - 0.130"). The studs on the backplate will need to be changed for longer ones if using the thicker board range (2.36 - 3.3 mm). Boards (PCBs) not within this range may require modifications to the backplate and the bolster plate.

Note: The dimensions presented in here do not account for a +/- 10% tolerance in them. For the max./min. values, refer to the corresponding backplate drawings.

6.1.2 Board Layout

Intel processors are targeted for use in a variety of board layouts and system form factors. Included in the list of system form factors are 1U, 2U, and workstation systems. Board layout varies within each system. Typical board layouts included shadowed configuration by which processors are placed in line or staggered with respect to direction of air flow. As an alternative processors may be placed side by side on the board.

6.1.3 Board Keep-Outs

Each of the components described in this document require an area beyond its physical size to accommodate components movement for installation purposes as well as to address their movement during shock and vibration. In identifying the board keep-outs, consider also board and system assembly process and tools. As a reference, recommended board keep-outs drawings (PCB top and bottom side) for the LGA3647 socket, retention mechanism, and heatsink are made available and included in the components assembly drawing. PCB keep-outs includes retention mechanism attach hole locations and sizes, components height limits in vicinity of the socket, as well as recommended area to allow access to retention and socket for processor installation.

6.1.4 Silkscreen Marking Identifying Socket and Keep-Out Area

Intel is recommending the socket name be silk screened adjacent to the socket such that it is visible after the bolster plate is installed.
6.1.5 Board Deflection

Excessive board deflection may result in failure at socket solder joints. Keeping the board deflection under the socket to an acceptable level by adhering to the following conditions can reduce the risk of solder joint failure:

1. Using the Intel reference heatsink retention and backplate
2. Maintaining compliance to maximum load values

Placement of board-to-chassis mounting holes also impacts board deflection and resultant socket solder ball stress. Customers need to assess shock for their designs as their heatsink retention, heatsink mass and chassis mounting holes may vary.

Designs that do not meet the design objectives of the backplate or exceed the maximum heatsink static compressive load, should follow Board Deflection Measurement Methodology as outlined to assess risk to socket solder joint reliability.

6.1.6 Socket Land Pattern Guidance

The land pattern guidance provided in this section applies to printed circuit board design. The Recommendation for Printed Circuit Board (PCB) land patterns is to ensure solder joint reliability during dynamic stresses, often encountered during shipping and handling and hence to increase socket reliability.

The land pattern for the LGA3647-0 socket is a 39 mil hexagonal array. See Figure 6-1 for detailed location and land pattern type.

Table 6-1. LGA3647 Socket Land Pattern Guidance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component Size</td>
<td>76.12 mm x 60.5 mm</td>
</tr>
<tr>
<td>Pitch</td>
<td>0.859 mm in X, and 0.991 mm staggered in Y</td>
</tr>
<tr>
<td>Pkg SRO</td>
<td>0.56 mm in X, and 0.854 mm in Y</td>
</tr>
<tr>
<td>Stencil Opening</td>
<td>19 mil</td>
</tr>
<tr>
<td>Ball Count</td>
<td>3647</td>
</tr>
<tr>
<td>LPID</td>
<td>2725</td>
</tr>
</tbody>
</table>
Figure 6-1. LGA3647 Socket Land Pattern Guidance

![LGA3647 Socket Land Pattern Guidance](image)

<table>
<thead>
<tr>
<th>Legend</th>
<th>Color</th>
<th>Pad Size (mil/micron)</th>
<th>Type</th>
<th>Trace Requirements</th>
<th># of lands</th>
</tr>
</thead>
<tbody>
<tr>
<td>Black</td>
<td></td>
<td>17x20 mil (431.8umx508um) Oblong Pads (see definition below) with 17mil (431.8um) pad opening offset by 1.5 mil – offset direction is towards the inside of the socket. <strong>These should be partial (roughly half) SMDs (full SMD or full MD is NOT acceptable)</strong>. <strong>Preferred</strong>: Long axis of pad and traces connected to the pad should be pointing away from the center of the pin field (90° wrt socket edge). <strong>Alternate</strong>: Long axis of pad and traces connected to the pad pointing along the skt vertical or horizontal axis.</td>
<td>56</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Red</td>
<td></td>
<td>17x20 mil (431.8umx508um) Oblong Pads with 17mil (431.8um) pad opening. <strong>These should be partial (roughly half) SMDs (full SMD or full MD is NOT acceptable)</strong>. Long axis of pad and traces connected to the pad should be pointing away from the center of the pin field (90° wrt socket edge) – Vertical on North-South edges and Horizontal on East-West edges</td>
<td>176</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Green</td>
<td></td>
<td>Between 17mil (431.8um) to 20mil (508um) circular MD (see definition below). Larger pads are preferred</td>
<td>130</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Blue</td>
<td></td>
<td>Preferred 17mil (431.8um) circular MD (see definition below) OR Alternate: SMD with 17mil (431.8um) pad opening</td>
<td>3283</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Total** = 3647

**Pad Type Recommendation**

Intel defines two types of pad types based on how they are constructed. A Metal Defined (MD) pad is one where a pad is individually etched into the PCB with a minimum width trace exiting it. The solder mask defined (SMD) pad is typically a pad in a flood plane where the solder mask opening defines the pad size for soldering to the component.

In thermal cycling a MD pad has shown to be more robust than a SMD pad type. The solder mask that defines the SMD pad can create a sharp edge on the solder joint as the solder ball/paste conforms to the window created by the solder mask.
For certain failure modes, the MD pad may not be as robust in shock and vibration (S and V). During S and V, the predominant failure mode for a MD pad in the corner of the BGA layout is pad craters and solder joint cracks. A corner MD pad can be made more robust and behave like a SMD pad by having a wide trace enter the pad. This trace should be 10 mil minimum but not to exceed the pad diameter and exit the pad.

During board flexure that results from shock and vibration a SMD pad is less susceptible to a crack initiating due to the larger surface area. Intel has defined selected solder joints of the socket as Non-Critical To Function (NCTF) when evaluating package solder joints post environmental testing.

The signals at NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.

### 6.2 System Mechanical Design Consideration

#### 6.2.1 Processor and Socket Stack-up Height

**Figure 6-2. Processor/Socket Stack Height**

Overall processor and socket stack height is provided here as convenience and should be derived from (a) the height of the socket seating plane above the motherboard after reflow, (b) the height of the package from the package seating plane to the top of the IHS, and accounting for its nominal variation and tolerances.

#### 6.2.2 Components Volumetric

The baseboard keep-out zones on the primary and secondary sides and height restrictions under the enabling component region will be provided and included as a part of the components drawings. The overall volumetric keep in zone encapsulates the processor, socket, and the entire thermal/mechanical enabling assembly.

#### 6.2.3 Components Mass

The static compressive load should also be considered in dynamic assessments.

Direct contact between backplate and chassis pan will usually help minimize board deflection during shock.
6.3 System Thermal Design Considerations

6.3.1 Ambient Temperature (TLA)

The temperature of the inlet air entering the processor is referenced in this document as the ambient temperature (TLA). This is not a system requirement. It is measured from the air upstream and in close vicinity to the processor cooling device. For the cooling systems, the ambient temperature is measured from the inlet air to the cooling device.

6.3.2 Airflow

Airflow should be provided by a system fan or blower to cool the processor package. Available airflow at the component’s cooling solution, direction, and restrictions through the system should be considered in optimizing the components cooling solution design.

6.3.3 Pressure Drop (Delta P)

The allowable pressure drop in the airflow to ensure cooling requirements for the system components at downstream from the processor should be taken into account in designing the processor cooling requirements.

§
7 Thermal Design Guidelines

7.1 Heatsink Design Considerations

To remove the heat from the processor, basic thermal design considerations include:

- The area of the surface on which the heat transfer takes place - Without any enhancements, this is the surface of the processor package IHS. One method used to improve thermal performance is to attach a heatsink to the IHS. A heatsink can increase the effective heat transfer surface area by conducting heat out of the IHS and into the surrounding air through fins attached to the heatsink base.

- The conduction path from the heat source to the heatsink fins - Providing a direct conduction path from the heat source to the heatsink fins and selecting materials with higher thermal conductivity typically improves heatsink performance. The length, thickness, and conductivity of the conduction path from the heat source to the fins directly impacts the thermal performance of the heatsink. In particular, the quality of the contact between the package IHS and the heatsink base has a higher impact on the overall thermal solution performance. Thermal Interface Material (TIM) is used to fill in the gap between the IHS and the bottom surface of the heatsink, and thereby improves the overall performance of the thermal stack-up (IHS-TIM-Heatsink). With extremely poor heatsink interface flatness or roughness, TIM may not adequately fill the gap. The TIM thermal performance depends on its thermal conductivity as well as the pressure load applied to it.

- The heat transfer conditions on the surface upon which heat transfer takes place - Convective heat transfer occurs between the airflow and the surface exposed to the flow. It is characterized by the local ambient temperature of the air, $T_{LA}$, and the local air velocity over the surface. The higher the air velocity over the surface, the more efficient the resulting cooling. The nature of the airflow can also enhance heat transfer via convection. Turbulent flow can provide improvement over laminar flow. In the case of a heatsink, the surface exposed to the flow includes the fin faces and the heatsink base.

An active heatsink typically incorporates a fan that helps manage the airflow through the heatsink.

Passive heatsink solutions require in-depth knowledge of the airflow in the chassis. As the heatsink fin density (the number of fins in a given cross-section) increases, the resistance to the airflow increases; it is more likely that the air will travel around the heatsink instead of through it, unless air bypass is carefully managed. Using air-ducting techniques to manage bypass area is an effective method for maximizing airflow through the heatsink fins.

7.2 Thermal Interface Material (TIM) Considerations

Thermal interface material between the processor IHS and the heatsink base is necessary to improve thermal conduction from the IHS to the heatsink. Many thermal interface materials can be pre-applied to the heatsink base prior to shipment from the heatsink supplier without the need for a separate TIM dispense or attachment process in the final assembly factory.

All thermal interface materials should be sized and positioned on the heatsink base in a way that ensures that the entire area is covered. It is important to compensate for heatsink-to-processor positional alignment when selecting the proper TIM size.
When pre-applied material is used, it is recommended that it have a protective cover.

Thermal performance usually degrades over the life of the assembly and this degradation needs to be accounted for in the thermal performance. Degradation can be caused by shipping and handling, environmental temperature, humidity conditions, load relaxation over time, temperature cycling or material changes (most notably in the TIM) over time. For this reason, the measured $T_{\text{CASE}}$ value of a given processor may increase over time, depending on the type of TIM material.

### 7.3 Thermal Solution Performance Characterization

The case-to-local ambient Thermal Characterization Parameter ($\Psi_{CA}$) is defined by:

$$\Psi_{CA} = \frac{T_{\text{CASE}} - T_{LA}}{T_{\text{DP}}}$$

Where:

$T_{\text{CASE}}$ = Processor case temperature ($^\circ$C)

$T_{LA}$ = Local ambient temperature before the air enters the processor heatsink ($^\circ$C)

$T_{\text{DP}}$ = TDP (W) assumes all power dissipates through the integrated heat spreader. This inexact assumption is convenient for heatsink design.

$$\Psi_{CA} = \Psi_{CS} + \Psi_{SA}$$

Where:

$\Psi_{CS}$ = Thermal characterization parameter of the TIM ($^\circ$C/W) is dependent on the thermal conductivity and thickness of the TIM.

$\Psi_{SA}$ = Thermal characterization parameter from heatsink-to-local ambient ($^\circ$C/W) is dependent on the thermal conductivity and geometry of the heatsink and dependent on the air velocity through the heatsink fins.

Figure 7-1 illustrates the thermal characterization parameters.
Processor enabling components consist of a set of mechanical components that enable integration of the processor with the board and system. Unlike the previous generation of LGA sockets, the LGA3647-0 socket uses a spring-loading mechanism to maintain the interface between the processor and the socket. The socket loading spring is provided by the bolster plate and its design is defined to provide the socket static load. The heatsink retention mechanism provides the board with structural stiffness to secure and support the mass the heatsink. In preventing damage to the socket during the processor installation, the processor and heatsink are held together using a package carrier mechanism. The assembly of the processor and heatsink prior to socket installation is referred to as the Processor Heatsink Module (PHM).

The main components of the socket stack are:

- Backplate
- Bolster plate with spring
- Processor package carrier or carrier
- Heatsink

### 8.1 PHM Overview

The LGA3647-0 socket PHM design consists of a assembly of the processor, heatsink, and a package carrier. The PHM design enables ease of installation of the processor into the socket while utilizing the guide posts of the bolster plate to pre-align the PHM and socket in minimizing risk of the damaging the socket contacts.
Figure 8-1. LGA 3647-0 Enabling Components (ISO View)
8.2 PHM Mechanical Design Considerations and Recommendations

8.3 PHM Features

One of the key features of the PHM is enabling the integration of the processor and heatsink as a single module. As a module, the PHM assembly acts as the vehicle for installing the processor onto the socket; reducing the risk of damaging the socket contacts.

Bolster plate guide posts serve as the alignment feature between the PHM and socket. Dissimilar posts on the bolster plate are the keying feature between the socket and the PHM that prevents the PHM from engaging with the socket when incorrectly oriented.

Protrusions on four corners of the package on the package carrier provide secondary alignment between the PHM and the socket as they interface with the socket wall exterior. Primary alignment between processor and socket is achieved through socket wall interior by constraining the processor movement.
8.4 PHM Loading Mechanism (PHLM)

8.4.1 Retention Mechanism Design Overview

The LGA3647 socket retention mechanism design consists of a top (bolster) plate and a backplate.

Bolster Plate with Spring

The bolster plate is an integrated subassembly that includes two corner guiding posts placed at opposite corners, nuts to mate with the backplate, and two springs that attach to the heatsink via screws. The corner posts guide the Processor Heatsink Module (PHM) as it is lowered over the socket. The corner posts act as coarse position constraints in the X-Y direction to prevent the PHM from moving and potentially damaging the processor package or socket. The springs on either side of the bolster plate are mechanically attached via rivets. The PHM is secured to the bolster plate by the two screws located in mid section on either side of the heatsink. Doing so will exert force normal to the socket at the top of the package IHS. The resulting socket-to-processor contact force ensures maximum contact areas between socket pins and processor package lands, as well as thermal interface material bond between package and heatsink. The springs include stoppers on their outer edges, to prevent movement of the heatsink in the Z-direction due to forces parallel to the motherboard.

Backplate

The backplate provides structural rigidity to the motherboard supporting the PHM mass and reducing board deflection resulted form socket loading. Bolster plate cut-outs enables component placements on the backside of the motherboard. The backplate is secured to the bolster plate at its threaded PEM studs.

Note: The backplate is compatible only with the matching bolster plate.

Both bolster plate and the backplate are isolated from the routing and vias on the backside of the motherboard by an insulator covering entire surface interface between the plates and the motherboard.

Nut Durability Specification

The PHLM heatsink nuts and bolster plate studs are rated to a durability specification of 12 installation and removal cycles, when using the reference designs with lubrication. Lubrication is required on the bolster plate threaded studs and heatsink nut threads. This is based on the visual inspection criteria of no observed dust/shavings greater than 0.5 mm in length as seen from the naked eye from 24 inches away with direct overhead lighting under cool white fluorescent light conditions [60-120 Ft-Candle (645-1293 LUX)] or equivalent, and a viewing time of one visual pass of 5-7 seconds for each surface. Refer to Appendix D, “Retention Assembly Mechanical Drawings” for details on the hardware.
**Note:** Narrow fabric bolster plate design includes features required for retention of Intel fabric passive cable. Even though the Second Generation Intel® Xeon® Scalable Processors does not support the use of the Intel fabric passive cable, it is possible to use the narrow fabric bolster plate for the PHLM.

**Figure 8-3. Narrow Fabric Bolster Plate Assembly (ISO View)**

**Note:** Narrow non-fabric bolster plate design does not include the features required for retention of the Intel fabric passive cable.

**Figure 8-4. Narrow Non-Fabric Bolster Plate Assembly (ISO View)**
Figure 8-5. Narrow Backplate Assembly (ISO View)
8.4.2 PHLM Features

The bolster plate incorporates mechanical features specific to Second Generation Intel® Xeon® Scalable Processors PHM and PCB. The large and small guide posts provide both a keying mechanism and serve as a secondary alignment between the PHM and socket.

Figure 8-6. Narrow Bolster Plate Part Feature

Narrow Bolster Plate
1. PHM guide post (large)
2. Positioning tab (with respect to socket)
3. Attachment fasteners (7x)
4. PEM threaded studs (2x)
5. Load spring (heatsink attach spring)
6. Load screw (heatsink attach screw -2x)
7. Insulator
8. PHM guide post (small)
9. LEC54B connector latch (not supported in the Second Generation Intel® Xeon® Scalable Processors)
10. LEC54B connector opening (not supported in the Second Generation Intel® Xeon® Scalable Processors)
11. LEC54B guide pin (not supported in the Second Generation Intel® Xeon® Scalable Processors)
12. Pin one indicator

Note: The narrow Fabric bolster plate can be used with the Second Generation Intel® Xeon® Scalable Processors, although items 9, 10 and 11 will not have any added value as the...
LEC54B connector is not enabled in this generation. For a bolster plate without these features, refer to the Non-Fabric Narrow Bolster Plate.

**Figure 8-7. Narrow Backplate Part Feature**

![Narrow Backplate Diagram]

**Narrow Backplate**

1. Center cavity for PCB components
2. PEM studs (7x)
3. Insulator
4. Cavity for PCB components (small - 4x)
5. Cavity for PCB components (square - 4x)
6. Pin one indicator
8.4.3 **PHM Loading Mechanism Material Specifications**

PHM retention mechanism is defined to be installed onto the PCB post socket assembly process. There are no system attachment. However, additional support may be necessary depending on board and system configuration and the heatsink mass.

<table>
<thead>
<tr>
<th>Table 8-1. Bolster Plate Material Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>Material Thickness</td>
</tr>
<tr>
<td>Insulator Thickness</td>
</tr>
<tr>
<td>Material Strength</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Flatness</td>
</tr>
<tr>
<td>Spring Rivet Pullout Force</td>
</tr>
<tr>
<td>Nut/Collar Separation Force</td>
</tr>
</tbody>
</table>

*Note:* See bolster plate drawing for additional details.

<table>
<thead>
<tr>
<th>Table 8-2. Backplate Material Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>Material Thickness</td>
</tr>
<tr>
<td>Insulator Thickness</td>
</tr>
<tr>
<td>Material Strength</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Flatness</td>
</tr>
<tr>
<td>Studs pull-out Force</td>
</tr>
<tr>
<td>Studs Torque Out</td>
</tr>
</tbody>
</table>

*Note:* See backplate drawing for details.

8.4.4 **Bolster and Backplates Marking**

All markings required in this section must withstand a minimum temperature of 100 °C.

<table>
<thead>
<tr>
<th>Table 8-3. Bolster and Backplates Traceability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part Number</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Lot Traceability</td>
</tr>
</tbody>
</table>
8.5 Package Carrier Design

The processor package carrier or carrier is an integral part of the Processor Heatsink Module (PHM). It holds the package and heatsink together creating a single module for installation onto the socket. Matching the package carrier designated keying features to the processor package notches ensures the package is properly aligned to the package carrier. The PHM package carrier is designed to align the processor to the socket using socket walls as alignment features. Alignment between the package carrier and socket provides a secondary level of alignment in preventing damage to the socket during the processor installation sequence.

During the components subassembly, the processor package is first aligned and latched onto the package carrier. The pre-assembled processor and package carrier is then attached and held to the processor heatsink. Thermal Interface Material (TIM2) is expected to be pre-applied to the heatsink prior to the package carrier plus processor subassembly installation.
8.5.1 Package Carrier Mechanical Features

Key features of the PHM package carrier are identified in the following illustrations.

Note: The narrow non-fabric package carrier is not compatible with the processor SKUs with fabric feature.

Narrow Non-Fabric Package Carrier Mechanical Features (Top View)

1. Crossbar
2. Side walls limiting package movement
3. Heatsink alignment partial-post
4. Surface interface with the heatsink base
5. Heatsink latch (4x)
6. Package carrier to bolster plate small post alignment hole
7. Stiffening crossbar
8. Opening for the tool access (to break the TIM bonding between the processor and heatsink)
9. Pin one indicator
10. Carrier to heatsink orientation indicator
11. Package carrier to bolster plate large post alignment hole
Figure 8-9. Narrow Non-Fabric Package Carrier Mechanical Features (Bottom View)

Narrow Non-Fabric Package Carrier (Bottom View)

1. Package IHS interface
2. Package carrier to socket body alignment features
3. Package carrier to socket body alignment features
4. Package carrier latch
5. Stiffening crossbar
6. Package carrier latch at the processor tab
7. Prevention pillars to avoid the TIM breaker to enter a forbidden area (3x)
8.5.2 Package carrier Marking

All markings required in this section must withstand a minimum temperature of 100°C

Table 8-4. Package carrier Marking

| Part Number | • Manufacturer's insignia (font size at supplier’s discretion).  
|            | • This mark will be molded or laser-marked into the top side of the socket housing.  
|            | • Both part number and manufacturer’s insignia will be visible when assembled with the processor and the heatsink. |
| Lot Traceability | • Package carrier shall be marked with a lot identification code to allow traceability of all components, date of manufacture (year and week), and assembly location. The mark must be placed on a surface that is visible after assembled with the processor and heatsink. In addition, this identification code must be marked on the exterior of the box in which the unit is shipped. |

8.5.3 Package Carrier Material Specifications

Table 8-5. Package Carrier Material Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>PC-ABS</td>
<td>Recommended</td>
</tr>
<tr>
<td>Flammability</td>
<td>UL Flammability rating 94-V0</td>
<td>Required</td>
</tr>
<tr>
<td>Withstand Temperature</td>
<td>120 °C min.</td>
<td>Required</td>
</tr>
</tbody>
</table>

8.5.4 Package Carrier Durability

The package carrier must withstand 10 numbers of attachment/removal cycles. An attachment cycle is defined as a one time attachment of the carrier to the processor package and heatsink. Removal cycle is defined as separating the carrier from the processor and heatsink one time.

The package carrier must also withstand 10 numbers of socket installation/removal cycles. The Installation and removal cycle is defined as installing the PHM onto the socket, securing it, un-securing the PHM, and disengaging the PHM from the socket.
8.6 PHM Heatsink

The processor requires a heatsink to remove the heat dissipated at the processor package IHS and to maintain the processor die temperature within its operating temperature. The PHM heatsink design serves a dual purpose. One is to remove the heat from the processor. The other is to apply the required loading to actuate the LGA3647 socket and to apply a sufficient amount of pressure to maintain the bond between the TIM2, the heatsink pedestal, and the processor IHS.

Processor heatsink performance is dependent on the thermal environment it is in, such as inlet air temperature and flow rate and applied heatsink design technology. The heatsink thermal characteristics within a defined set of thermal boundary conditions must meet the processor thermal specifications for the processor to achieve its optimum performance.

The processor heatsink is designed to interface with the PHM package carrier and the socket retention mechanism. Mechanical features at the base of the heatsink enable the PHM to latch on and hold together the processor and the heatsink. Retention mechanism standoffs provide alignment and orientation with respect to the socket.

**Figure 8-10. PHM Assembly (Bottom View)**

Two fasteners on the sides of the heatsink secures the heatsink to the retention mechanism. When fasteners are tightened to the specified torque limit, the heatsink induces force normal to the socket through the processor package IHS. Not adhering to the package and the socket load specification can result in damaging the processor and/or the socket as well as the retention mechanism.
8.6.1 Heatsink Mechanical Interfaces

Figure 8-11. Heatsink Base Mechanical Features

Heatsink Mechanical Features
1. Bolster plate spring load fastener (left side)
2. Heatsink retention fastener
3. Heatsink to bolster plate post alignment hole
4. Bolster plate spring load fastener (right side)
5. Cut-out for package carrier to heatsink latching feature
6. Heatsink to bolster plate post alignment hole

8.6.2 Heatsink Mechanical Requirements

Mechanical features of the heatsink are defined such that they enable integration of the processor and the package carrier to establish a processor heatsink module. Hence, it is critical that the initial position of the processor with respect to the heatsink base is well controlled. This is established through the package carrier and through the carrier to heatsink latching positions.

The heatsink is also used to establish the preliminary alignment between the processor and the socket. Processor to socket preliminary alignment is established through bolster plate alignment posts which also act as a keying feature ensuring the PHM is properly orientated with respect to the socket.

The four fasteners on the heatsink are used to secure the PHM to the bolster plate. Two of the fasteners in the corners of the heatsink, diagonal to each other, are used to secure the heatsink to the bolster plate. These fasteners must be tightened first to ensure the heatsink has touched-down on the bolster plate, and it is leveled to the bolster plate. This will 1) reduce the risk of damaging contacts during the installation, and 2) ensures heatsink and bolster plate load fasteners are close to engage. Properly
torquing the two middle fasteners will provide the loading necessary to actuate the socket while complying with both the socket and processor mechanical loading specifications.

Heatsink base cutouts for the package carrier latching features and for the fasteners are defined to address the heatsink mechanical and integration requirements. Refer to the heatsink mechanical drawing for details.

Table 8-6. Heatsink Mechanical Requirement

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Values</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heatsink Base Thickness</td>
<td>4.5 ±0.12 mm</td>
<td>See heatsink mechanical drawings.</td>
</tr>
<tr>
<td>Heatsink Base Flatness</td>
<td>0.24 mm</td>
<td></td>
</tr>
<tr>
<td>Heatsink base holes dimensions for the bolster plate retention fasteners</td>
<td>See heatsink mechanical drawings.</td>
<td></td>
</tr>
<tr>
<td>Bolster plate small hole dimensions for the bolster plate alignment post</td>
<td>See heatsink mechanical drawings.</td>
<td></td>
</tr>
<tr>
<td>Bolster plate large hole dimensions for the bolster plate alignment post</td>
<td>See heatsink mechanical drawings.</td>
<td></td>
</tr>
<tr>
<td>Heatsink base holes dimensions for the bolster plate spring fasteners</td>
<td>See heatsink mechanical drawings.</td>
<td></td>
</tr>
<tr>
<td>Heatsink Installation Torque</td>
<td>12.0 in-Lb</td>
<td></td>
</tr>
<tr>
<td>Maximum Allowable Heatsink Mass</td>
<td>600 g.</td>
<td></td>
</tr>
</tbody>
</table>

Note: This stiffness guidance is related to socket reliability, not thermal performance. Any potential thermal impact due to heatsink base deflection at lower stiffness levels needs to be determined separately.

§
9 Component Assembly Instructions

Reference enabling components are designed for compatibility with the Second Generation Intel® Xeon® Scalable Processors package and to ease board and system assembly. The processor enabling solution is illustrated in Figure 9-1, "Processor and Enabling Components Mechanical Assembly" on page 83. The method of installing the processor onto the motherboard is to assemble the processor and its enabling solution prior to installation onto a board. This will allow the processor and its cooling solution to be assembled offline and delivered to the board or the system assembly site. This method is commonly referred to as the pre-attach method. In this section pre-assembling the processor and the heatsink as a module (PHM) and its installation onto the motherboard will be described. It should be noted that without the processor package carrier, there is no control mechanism to secure the processor to the heatsink or align the module to the socket.

The processor and its enabling components assembly are divided into three areas. First is the top and bottom plate installation onto the motherboard. Second is the processor, and its cooling solution assembly. Last is the processor installation onto the socket and securing the assembly to the board.

Instructions provided from here on are an overview of the components assembly and installation onto a board or a system.

9.1 Processor Enabling Components

Processor enabling components consist of a set of components that enable integration of the processor with the board and system. Processor enabling components are listed in Table 9-1, “LGA3647-0 Components Listing and Compatibility” and are illustrated in Figure 9-1, "Processor and Enabling Components Mechanical Assembly".
### Table 9-1. LGA3647-0 Components Listing and Compatibility

<table>
<thead>
<tr>
<th>Enabling Component</th>
<th>Narrow Non-Fabric PHM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor Package</td>
<td>Non-fabric</td>
</tr>
<tr>
<td>LGA3647-0 LGA socket (Socket P0)</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Narrow Fabric PHLM</strong></td>
<td></td>
</tr>
<tr>
<td>Narrow Backplate*</td>
<td>Yes</td>
</tr>
<tr>
<td>Narrow Fabric Bolster Plate</td>
<td>Yes</td>
</tr>
<tr>
<td>Narrow Fabric Socket Dust Cover</td>
<td>Yes</td>
</tr>
<tr>
<td>Narrow Fabric Bolster and Socket Dust Cover</td>
<td>Yes</td>
</tr>
<tr>
<td>Narrow Fabric Package Carrier</td>
<td>No</td>
</tr>
<tr>
<td><strong>Narrow Non-Fabric PHLM</strong></td>
<td></td>
</tr>
<tr>
<td>Narrow Backplate*</td>
<td>Yes</td>
</tr>
<tr>
<td>Narrow non-fabric Bolster Plate</td>
<td>Yes</td>
</tr>
<tr>
<td>Narrow non-Fabric Socket Dust Cover</td>
<td>Yes</td>
</tr>
<tr>
<td>Narrow non-Fabric Bolster Socket Dust Cover</td>
<td>Yes</td>
</tr>
<tr>
<td>Narrow non-Fabric Package Carrier</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Square PHLM</strong></td>
<td></td>
</tr>
<tr>
<td>Square Bolster Plate*</td>
<td>No</td>
</tr>
<tr>
<td>Square Socket Dust Cover</td>
<td>No</td>
</tr>
<tr>
<td>Square Bolster Socket Dust Cover</td>
<td>No</td>
</tr>
<tr>
<td>Square Backplate</td>
<td>No</td>
</tr>
<tr>
<td>Square Package Carrier</td>
<td>No</td>
</tr>
<tr>
<td><strong>Heatsinks</strong></td>
<td></td>
</tr>
<tr>
<td>1U Heatsink High Performance</td>
<td>Yes</td>
</tr>
<tr>
<td>1U Low Impedance Heatsink</td>
<td>Yes</td>
</tr>
<tr>
<td>2U Narrow Heatsink</td>
<td>Yes</td>
</tr>
<tr>
<td>Tower Square Heatsink</td>
<td>No</td>
</tr>
<tr>
<td>Non-MCP (10-Year Use + NEBS-Friendly) Profile</td>
<td>Yes</td>
</tr>
</tbody>
</table>

**Notes:**
1. The components marked with an * support board thickness of 1.6 - 2.36 mm (0.063" - 0.093").
2. Refer to Table 11-1, "Second Generation Intel® Xeon® Scalable Processors Based Platform LGA3647-0 Socket Enabling Components" for Intel and suppliers’ part numbers.
3. PHM is Processor Heatsink Module.
Note: The processor thermal mechanical solution assembly begins with surface mounting the LGA3647-0 socket onto the baseboard. The remaining steps presumed that the socket(s) have already been surface-mounted onto the board.
9.2 Top and Bolster Plate Installation

The first step in board or system assembly is to attach the LGA3647-0 socket and bottom plate to the motherboard. For the processor and components assembly, it is presumed that the socket(s) have already been surface-mounted onto the board. As for the bolster plate, customers may require double-sided Kapton* tape to hold the back in place for the duration of the assembly. While installing the bolster plate or placing the motherboard on the bolster plate, care should be taken to visually align them to prevent damaging the motherboard.

**Note:**

The bolster plate must be properly oriented with respect to the motherboard. Otherwise, the processor and the top assembly will not engage properly with the motherboard and the socket.

The next step is installing the top plate with its Kapton tape pre-applied. The top plate should be placed on the motherboard while ensuring that it is properly oriented. The indicator on the top plate, as well as its holes pattern, provide clues as to its orientation. The top plate is then secured to the motherboard by attaching the large and small posts.

**Warning:**

The large and small posts must be tightened to a maximum torque value of 0.8 N-m (7 lbf-in.). Damage to the processor and its enabling components may result if the posts are not tightened properly.

After the bolster plate is installed, the socket PNP capacitors should be carefully removed. This capacitors do prevent dust or small foreign material enter socket contact area. Hence, they should be replaced by a socket dust cover after the bolster is installed. Be sure the socket duct cover is of the correct part number for use with the installed bolster plate.

---

Figure 9-2. LGA3647-0 Post SMT with PNP Cover
Figure 9-3. LGA3647-0 Backplate (Installed Position)

Figure 9-4. LGA3647-0 Bolster Plate in Installed Position with the Socket Dust Cover
9.3 Processor Heatsink Subassembly

Offline assembly of the processor and heatsink is done using the processor shipping tray. Assembly begins with the appropriate processor clip: orient the clip and snap it onto the processor in the tray.

Verify that the clip is fully attached to the processor before proceeding. The heatsink is next: it is assumed that the thermal interface material is already applied and remove any protective film or cover before proceeding.

Next, properly orient the heatsink if necessary and lower it onto the processor and clip assembly from the previous step. Make sure the thermal interface material does not come in contact with any surface until it rests on the processor.

At this point, the processor clip can be snapped onto the heatsink base at the top and bottom edges and within both the oblong holes. It may be necessary to push at the top until those snap features are engaged and then at the bottom until those snap features are engaged.

Verify that all snap features of the processor clip are fully engaged before removing the PHM assembly from the tray.

**Caution:** If the board or the system assembly site is at a different site, then the above assembly should be properly packed to prevent any damage to the processor or the components while in transit.

Figure 9-5. Processor Heatsink Module in Installed Position
9.4 Processor Installation

Inspect the processor and heatsink assembly if they are assembled offline. The next steps assume that the board is ready for the processor installation. That is, Section 9.2 is completed.

Gently remove the socket dust cover and inspect the socket for damage or defects.

**Warning:** Do not install the processor if the socket contains defects.

Orient the processor assembly over the large and small posts. Gently lower the assembly, while making sure that the posts protrude through the heatsink holes.

**Warning:** If the processor has reached its stop but the posts are not protruded, inspect the setup to ensure processor is properly seated. This may require removing the assembly, inspecting it and the board, and reinstalling the processor assembly.

Once the processor is properly seated on the socket, tighten the corner fasteners and then tighten the spring fasteners to load the entire assembly. Be sure that all of the fasteners are tightened and inspect the assembly to ensure that it is properly installed.

![LGA3647-0 Processor Heatsink Module (PHM) Ready for Installation](image)
This section describes the Intel reference heatsink design and performance specifications in accordance with the processor thermal and mechanical specifications. System form factor compatibility and thermal boundary conditions were applied in designing the heatsinks.

10.1 Reference Heatsink Design

Intel has several reference heat sinks for the Second Generation Intel® Xeon® Scalable Processors based platform. This section details the design targets and performance of each heatsink design within a set of environmental boundary conditions.

Table 10-1. 1U Narrow Low Impedance Heatsink

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volumetric</td>
<td>78 x 108 x 25.5 mm³</td>
</tr>
<tr>
<td>Base Thickness</td>
<td>4.5 mm</td>
</tr>
<tr>
<td>Fin Height</td>
<td>21 mm</td>
</tr>
<tr>
<td>Ambient Temperature (Tla)</td>
<td>Refer to Table 5-6, &quot;Thermal Boundary Conditions&quot; to obtain these values.</td>
</tr>
<tr>
<td>Air Flow Rate (Q)</td>
<td></td>
</tr>
</tbody>
</table>

Figure 10-1. 1U Narrow Low Impedance Heatsink

The next chart illustrates the heatsink performance and pressure drop as a function of the air flow rate.
The next chart illustrates the heatsink performance and pressure drop as a function of the air flow rate.
Table 10-4. 1U Narrow High Performance Heatsink

<table>
<thead>
<tr>
<th>Heatsink Performance Variables</th>
<th>Heatsink Performance Chart</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \Psi_{CA,TTV} = \alpha + \beta \cdot (Q)^\gamma )</td>
<td><img src="image" alt="Heatsink Performance Chart" /></td>
</tr>
<tr>
<td>( \alpha = 0.122, \beta = 1.528, \gamma = 0.967 )</td>
<td></td>
</tr>
<tr>
<td>( Q = 11.6 \text{ CFM} )</td>
<td></td>
</tr>
<tr>
<td>Mean ( \Psi_{CA,TTV} = 0.265 ^\circ \text{C/W} )</td>
<td></td>
</tr>
<tr>
<td>( \sigma = 0.0025 )</td>
<td></td>
</tr>
<tr>
<td>( \Delta P = 5.52E-04 \cdot Q^2 + 1.76E-02 \cdot Q )</td>
<td></td>
</tr>
</tbody>
</table>

Table 10-5. 2U Narrow High Performance Heat Pipe Heatsink

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volumetric</td>
<td>78 x 108 x 64 mm³</td>
</tr>
<tr>
<td>Base Thickness</td>
<td>4.5 mm</td>
</tr>
<tr>
<td>Fin Height</td>
<td>59.5 mm</td>
</tr>
<tr>
<td>Heatpipe</td>
<td>4x with dia: 6 mm</td>
</tr>
<tr>
<td>Ambient Temperature (TUA)</td>
<td>Refer to Table 5-6, &quot;Thermal Boundary Conditions&quot; to obtain these values.</td>
</tr>
<tr>
<td>Air Flow Rate (Q)</td>
<td></td>
</tr>
</tbody>
</table>
The next chart illustrates the heatsink performance and pressure drop as a function of the air flow rate.

**Table 10-6. 2U Narrow High Performance Heatpipe Heatsink**

<table>
<thead>
<tr>
<th>Heatsink Performance Variables</th>
<th>Heatsink Performance Chart</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Psi_{CA,TTV} = \alpha + \beta \times (Q)^\gamma$</td>
<td>$\Delta P = 9.88E-05 \times Q^2 + 3.59E-03 \times Q$</td>
</tr>
<tr>
<td>$\alpha = 0.106$, $\beta = 1.385$, $\gamma = 0.938$</td>
<td>$Q = 21.5$ CFM</td>
</tr>
<tr>
<td>Mean $\Psi_{CA,TTV} = 0.179$ °C/W</td>
<td>$\sigma = 0.003$</td>
</tr>
<tr>
<td>$\Delta P$</td>
<td>$Q$</td>
</tr>
</tbody>
</table>

**Figure 10-3. 2U Narrow High Performance Heat Pipe Heatsink**
Table 10-7. Workstation Passive Square Heatpipe Heatsink

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volumetric</td>
<td>92 x 92 x 125mm³</td>
</tr>
<tr>
<td>Base Thickness</td>
<td>4.5 mm</td>
</tr>
<tr>
<td>Fin Height</td>
<td>59.5 mm</td>
</tr>
<tr>
<td>Heatpipe</td>
<td>4x U shape with dia: 6 mm</td>
</tr>
<tr>
<td>Ambient Temperature (T_{L,A})</td>
<td>Refer to Table 5-6, &quot;Thermal Boundary Conditions&quot; to obtain these values.</td>
</tr>
<tr>
<td>Air Flow Rate (Q)</td>
<td></td>
</tr>
</tbody>
</table>

Figure 10-4. Workstation Passive Square Heat Pipe Heatsink

The next chart illustrates the heatsink performance and pressure drop as a function of the air flow rate.
Table 10-8. Workstation Passive Square Heatpipe Heatsink

<table>
<thead>
<tr>
<th>Heatsink Performance Variables</th>
<th>Heatsink Performance Chart</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Psi_{CA,TTV} = \alpha + \beta \cdot (Q)^{1.064}$</td>
<td><img src="image" alt="Heatsink Performance Chart" /></td>
</tr>
<tr>
<td>$\alpha = 0.111, \beta = 1.847$</td>
<td></td>
</tr>
<tr>
<td>$Q = 23.2$ CFM</td>
<td></td>
</tr>
<tr>
<td>Mean $\Psi_{CA,TTV} = 0.176$ °C/W</td>
<td></td>
</tr>
<tr>
<td>$\sigma = 0.007$</td>
<td></td>
</tr>
<tr>
<td>$\Delta P = 2.93E-05 \cdot Q^2 + 3.47E-03 \cdot Q$</td>
<td></td>
</tr>
</tbody>
</table>

Table 10-9. Non-MCP (10-Year Use + NEBS-Friendly) Low Profile Heatsink

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volumetric</td>
<td>$12.4 \times 78 \times 108 \text{ mm}^3$</td>
</tr>
<tr>
<td>Base Thickness</td>
<td>4.5 mm</td>
</tr>
<tr>
<td>Fin Height</td>
<td>7.9 mm</td>
</tr>
</tbody>
</table>

Figure 10-5. Non-MCP (10-Year Use + NEBS-Friendly) Low Profile Heatsink
The next figure illustrates the heatsink performance as a function of the air speed.

Figure 10-6. Non-MCP (10-Year Use + NEBS-Friendly) Low Profile Heatsink Performance Chart

<table>
<thead>
<tr>
<th>Heatsink Performance Chart</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Heatsink Performance Chart" /></td>
</tr>
</tbody>
</table>

10.1.1 **Thermal Interface Material (TIM)**

Honeywell* PCM45F pad material was chosen as the interface material for analyzing boundary conditions and processor specifications. The recommended minimum activation load for PCM45F is ~15 PSI [103 kPA]. Meeting the minimum heatsink load targets described in Table 4-1 ensures that requirement is met.

§
11 Supplier Listing

Third-party suppliers are enabled to ensure that the reference thermal and mechanical components are available.

**Intel Enabled Supplier Information**

**Notes:**

1. Supplier listing is provided by Intel as a convenience to its customers. Intel does not make any representations or warranties whatsoever regarding the quality, reliability, functionality, or compatibility of these devices.
2. All part numbers listed are in prototype phase and have not been verified to meet performance targets or quality and reliability requirements and are subject to change.
3. Supplier information provided in the table was deemed accurate when this document was released.
4. Customers must evaluate performance against their own product requirements.
### Table 11-1. Second Generation Intel® Xeon® Scalable Processors Based Platform LGA3647-0 Socket Enabling Components

<table>
<thead>
<tr>
<th>Component</th>
<th>Intel P/N</th>
<th>Supplier 1</th>
<th>Supplier 1 P/N</th>
<th>Supplier 2</th>
<th>Supplier 2 P/N</th>
<th>Supplier 3</th>
<th>Supplier 3 P/N</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>LGA3647-0 Socket 30 μ-inch Gold Contacts (Socket P0)</td>
<td>J34320 - 001 Right Side Key Yellow</td>
<td>Tyco Electronics Connectivity* (TE)</td>
<td>2-2129710-6</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>J34320 - 002 Left Side Key Black</td>
<td>Tyco Electronics Connectivity (TE)</td>
<td>2-2129710-5</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>J34318 - 001 Right Side Key Yellow</td>
<td>NA</td>
<td>NA</td>
<td>Foxconn Interconnect Technology*</td>
<td>PE36473-01NK3-1H</td>
<td>NA</td>
<td>NA</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>J34318 - 002 Left Side Key Black</td>
<td>NA</td>
<td>NA</td>
<td>Foxconn Interconnect Technology</td>
<td>PE36473-01NK4-1H</td>
<td>NA</td>
<td>NA</td>
<td>3</td>
</tr>
<tr>
<td>LGA3647-0 Socket 15 μ-inch Gold Contacts (Socket P0)</td>
<td>J65187 - 001 Right Side Key Yellow</td>
<td>Tyco Electronics Connectivity (TE)</td>
<td>2-2129710-2</td>
<td>NA</td>
<td>NA</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>J65187 - 002 Left Side Key Black</td>
<td>Tyco Electronics Connectivity (TE)</td>
<td>2-2129710-1</td>
<td>NA</td>
<td>NA</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>H37603 - 202 Right Side Key Yellow</td>
<td>NA</td>
<td>NA</td>
<td>Foxconn Interconnect Technology*</td>
<td>PE36477-01NK1-1H</td>
<td>3</td>
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</tr>
<tr>
<td></td>
<td>H37603 - 203 Left Side Key Black</td>
<td>NA</td>
<td>NA</td>
<td>Foxconn Interconnect Technology</td>
<td>PE36477-01NK2-1H</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Socket-P Heatsink Nut Collar</td>
<td>H94875-004</td>
<td>KYZ</td>
<td>A10360H</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>3</td>
</tr>
<tr>
<td>Socket-P Delrin® Heatsink Washer</td>
<td>H37265-004</td>
<td>KYZ</td>
<td>A10247H</td>
<td>ITW</td>
<td>FT1604-A</td>
<td>NA</td>
<td>NA</td>
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<tr>
<td>Socket-P Intel® Xeon® Processor Scalable Processors Heatsink Nut</td>
<td>H98449-003</td>
<td>ITW</td>
<td>FT1614-A</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
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<td>Thermal Interface Material PCM45F 70X47X0.25 mm</td>
<td>H38442-001</td>
<td>Honeywell International, Inc.*</td>
<td>099079</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>3</td>
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<td>Component</td>
<td>Intel P/N</td>
<td>Supplier 1</td>
<td>Supplier 1 P/N</td>
<td>Supplier 2</td>
<td>Supplier 2 P/N</td>
<td>Supplier 3</td>
<td>Supplier 3 P/N</td>
<td>Note</td>
</tr>
<tr>
<td>------------------------------------------------</td>
<td>-------------------</td>
<td>---------------------</td>
<td>----------------</td>
<td>---------------------</td>
<td>----------------</td>
<td>--------------------</td>
<td>----------------</td>
<td>------</td>
</tr>
<tr>
<td>Narrow Fabric PHLM</td>
<td></td>
<td>LOTES CO LTD*</td>
<td>AZIF0087-P002C*</td>
<td>Foxconn Interconnect Technology</td>
<td>WNMEL60-80N04-EH</td>
<td>Tyco Electronics Connectivity (TE)</td>
<td>2310924-3</td>
<td>3</td>
</tr>
<tr>
<td>Narrow Fabric Bolster Plate</td>
<td>H95384-004</td>
<td>LOTES CO LTD*</td>
<td>AZIF0087-P002C*</td>
<td>Foxconn Interconnect Technology</td>
<td>WNMEL60-80N04-EH</td>
<td>Tyco Electronics Connectivity (TE)</td>
<td>2310924-3</td>
<td>3</td>
</tr>
<tr>
<td>Narrow Socket Dust Cover</td>
<td>H77975-005</td>
<td>LOTES CO LTD</td>
<td>AZIF0084-P002C*</td>
<td>Foxconn Interconnect Technology</td>
<td>WNMEL00-81N00-EH</td>
<td>Tyco Electronics Connectivity (TE)</td>
<td>2305234-1</td>
<td>3</td>
</tr>
<tr>
<td>Narrow Fabric Bolster and Socket Dust Cover</td>
<td>NA</td>
<td>LOTES CO LTD</td>
<td>AZIF0088-P002C*</td>
<td>Foxconn Interconnect Technology</td>
<td>PT44L11-4811</td>
<td>Tyco Electronics Connectivity (TE)</td>
<td>2310924-1</td>
<td>3</td>
</tr>
<tr>
<td>Narrow Fabric Bolster with Dust Cover and Backplate</td>
<td>NA</td>
<td>LOTES CO LTD</td>
<td>AZIF0112-P002C*</td>
<td>Foxconn Interconnect Technology</td>
<td>WNMEA66-81N01-EH</td>
<td>Tyco Electronics Connectivity (TE)</td>
<td>2314678-3</td>
<td>3</td>
</tr>
<tr>
<td>Narrow Non-Fabric PHLM</td>
<td></td>
<td>LOTES CO LTD*</td>
<td>AZIF0089-P002C*</td>
<td>Foxconn Interconnect Technology</td>
<td>WNMEL60-80N03-EH</td>
<td>Tyco Electronics Connectivity (TE)</td>
<td>2299805-1</td>
<td>3</td>
</tr>
<tr>
<td>Narrow Backplate (board thickness 1.6 - 2.36 mm (0.063&quot; - 0.093&quot;)</td>
<td>H77928-002</td>
<td>LOTES CO LTD</td>
<td>AHSK0010-P003C*</td>
<td>Foxconn Interconnect Technology</td>
<td>PT44P11-4801</td>
<td>Tyco Electronics Connectivity (TE)</td>
<td>2299805-1</td>
<td>3</td>
</tr>
<tr>
<td>Narrow Backplate (board thickness 2.36 - 3.3 mm (0.093&quot; - 0.130&quot;)</td>
<td>J36227-001</td>
<td>LOTES CO LTD</td>
<td>AHSK0013-P003C*</td>
<td>Foxconn Interconnect Technology</td>
<td>WNMEP06-80600-EH</td>
<td>Tyco Electronics Connectivity (TE)</td>
<td>2299805-3</td>
<td>3</td>
</tr>
<tr>
<td>Narrow non-fabric Bolster Plate</td>
<td>H95385-004</td>
<td>LOTES CO LTD</td>
<td>AZIF0089-P002C*</td>
<td>Foxconn Interconnect Technology</td>
<td>WNMEL60-80N03-EH</td>
<td>Tyco Electronics Connectivity (TE)</td>
<td>2299804-3</td>
<td>3</td>
</tr>
<tr>
<td>Narrow Socket Dust Cover</td>
<td>H77975-005</td>
<td>LOTES CO LTD</td>
<td>AZIF0084-P002C*</td>
<td>Foxconn Interconnect Technology</td>
<td>WNMEL00-81N00-EH</td>
<td>Tyco Electronics Connectivity (TE)</td>
<td>2305234-1</td>
<td>3</td>
</tr>
<tr>
<td>Narrow non-Fabric Bolster and Socket Dust Cover</td>
<td>NA</td>
<td>LOTES CO LTD</td>
<td>AZIF0090-P002C*</td>
<td>Foxconn Interconnect Technology</td>
<td>WNMEL60-80N00-EH</td>
<td>Tyco Electronics Connectivity (TE)</td>
<td>2299804-1</td>
<td>3</td>
</tr>
<tr>
<td>Narrow non-Fabric Package Carrier</td>
<td>H72851-002</td>
<td>LOTES CO LTD</td>
<td>AZIF0081-P002C*</td>
<td>Foxconn Interconnect Technology</td>
<td>WNMEL00-82N00-EH</td>
<td>Tyco Electronics Connectivity (TE)</td>
<td>2299806-1</td>
<td>3</td>
</tr>
</tbody>
</table>
### Table 11-1. Second Generation Intel® Xeon® Scalable Processors Based Platform LGA3647-0 Socket Enabling Components

<table>
<thead>
<tr>
<th>Component</th>
<th>Intel P/N</th>
<th>Supplier 1 P/N</th>
<th>Supplier 1</th>
<th>Supplier 2 P/N</th>
<th>Supplier 2</th>
<th>Supplier 3 P/N</th>
<th>Supplier 3</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Narrow non-Fabric Bolster with Dust Cover and Backplate</td>
<td>NA</td>
<td>LOTES CO LTD</td>
<td>AZIF0113- P002C*</td>
<td>Foxconn Interconnect Technology</td>
<td>WNMEA66-81N00-EH</td>
<td>Tyco Electronics Connectivity (TE)</td>
<td>2314678-1</td>
<td>3</td>
</tr>
<tr>
<td><strong>Heatsinks</strong></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1U High Performance Heatsink</td>
<td>H38569-008</td>
<td>Foxconn Technology Co. Ltd</td>
<td>1A21BJ900-RPC</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>3</td>
</tr>
<tr>
<td>1U Low Impedance Heatsink</td>
<td>H45651-006</td>
<td>CCI</td>
<td>0A14092601</td>
<td>Foxconn Technology Co. Ltd</td>
<td>1A21MPL00</td>
<td>NA</td>
<td>NA</td>
<td>3</td>
</tr>
<tr>
<td>2U Narrow Heatsink (Compatible with 2U and 4U system form factors)</td>
<td>H36976-007</td>
<td>Foxconn Technology Co. Ltd</td>
<td>1A21BMU00-RPC</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>3</td>
</tr>
<tr>
<td>Non-MCP (10-Year Use + NEBS-Friendly) Low Profile Heatsink</td>
<td>J12672-003</td>
<td>CCI</td>
<td>0A15386301</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>3</td>
</tr>
</tbody>
</table>

**Notes:**
1. See the component specifications for detail and ordering information.
2. Contact the local Intel representative for sample availability.
3. Components part numbers are subject to change. Contact your Intel representative and the suppliers for the latest revisions, compatibility between revisions, and availability schedule.
### Table 11-2. Components Supplier Contact Listing

<table>
<thead>
<tr>
<th>ID</th>
<th>Supplier</th>
<th>Contact</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Lotes Co LTD*</td>
<td>Cathy Yang Tel. +1-86-20-8468 6519 email: <a href="mailto:Cathy@lotes.com.cn">Cathy@lotes.com.cn</a></td>
</tr>
<tr>
<td>2</td>
<td>Foxconn Technology Co LTD*</td>
<td>Ray Wang Tel. +1 512 351-1493 x273 email: <a href="mailto:ray.wang@foxconn.com">ray.wang@foxconn.com</a></td>
</tr>
<tr>
<td>3</td>
<td>Molex Inc*</td>
<td>Joe Dambach Tel. +1 630-527-4546 email: <a href="mailto:Joe.Dambach@molex.com">Joe.Dambach@molex.com</a></td>
</tr>
<tr>
<td>4</td>
<td>Tyco Electronics Corporation (TE)*</td>
<td>Ellen Liang Tel. +886 2 2171 5261 email: <a href="mailto:ellen.yh.liang@te.com">ellen.yh.liang@te.com</a></td>
</tr>
<tr>
<td>5</td>
<td>Foxconn Interconnect Technology (FIT)*</td>
<td>Eric Ling Tel. +1 971-506-6441 +1 503-327-8346 email: <a href="mailto:eric.ling@fit-foxconn.com">eric.ling@fit-foxconn.com</a></td>
</tr>
<tr>
<td>6</td>
<td>CCI (Chaun-Choung) Technology Corp.*</td>
<td>12F,No 123-1, Hsing-De Rd., Sanchung, Taipei, Taiwan, R.O.C. Tel. +886 (2) 2995-2666 x1131 Fax: +886 (2) 2995-8258 Monica Chih <a href="mailto:Monica_chih@ccic.com.tw">Monica_chih@ccic.com.tw</a> Sean Wu <a href="mailto:sean_wu@ccic.com.tw">sean_wu@ccic.com.tw</a> (408)429-4670</td>
</tr>
<tr>
<td>7</td>
<td>Honeywell International, Inc.*</td>
<td>430 Li Bing Rd., Zhangjiang Hi-Tech Park, Pudong, Shanghai, China. Connije Smiriglio (Account Manager) Tel. +1 845-627-2750 email: <a href="mailto:Connie.smiriglio@honeywell.com">Connie.smiriglio@honeywell.com</a> Hyo Xi (Technical) Tel. 8621-28943106</td>
</tr>
<tr>
<td>8</td>
<td>KYZ</td>
<td>No.8, Xinhe Rd., Zhang Pu Town, Kunshan City, Jiangsu Province, China TW Tel: 02-82005703 CH Tel: 051257293826 Gary Yuan Tel. + 886 987237801 email: <a href="mailto:gary_yuan@kyz.com.tw">gary_yuan@kyz.com.tw</a> Anna Luo Tel. +886 981006216 email: <a href="mailto:anna_luo@kyz.com.tw">anna_luo@kyz.com.tw</a></td>
</tr>
<tr>
<td>9</td>
<td>ITW EBA</td>
<td>Chak Chakir Tel. 512.989.7771 email: <a href="mailto:chak.chakir@itweba.com">chak.chakir@itweba.com</a></td>
</tr>
</tbody>
</table>
A Quality and Reliability Requirements

A.1 Thermal/Mechanical Solution Stress Test

Intel evaluates reliability performance based on the use conditions (operating environment) of the end product by using acceleration models.

The use condition environment definitions provided in the next tables are based on speculative use condition assumptions, and are provided as examples only.

Based on the system enabling boundary condition, the solder ball temperature can vary and needs to be comprehended for reliability assessment.

Table A-1. Thermal Stress Test Examples

<table>
<thead>
<tr>
<th>Use Environment</th>
<th>Speculative Stress Condition</th>
<th>Example Use Condition</th>
<th>Example 7 yr. Stress Equivalent</th>
<th>Example 10 yr. Stress Equivalent</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slow small internal gradient changes due to external ambient (temperature cycle or externally heated) Fast, large gradient on/off to max operating temp. (power cycle or internally heated including power save features)</td>
<td>Temperature Cycle</td>
<td>D T = 35 - 44 °C (solder joint)</td>
<td>550-930 cycles Temp Cycle (-25 °C to 100 °C)</td>
<td>780-1345 cycles Temp Cycle (-25 °C to 100 °C)</td>
</tr>
<tr>
<td>High ambient moisture during low-power state (operating voltage)</td>
<td>THB/HAST</td>
<td>T = 25 -30 °C 85%RH(ambient)</td>
<td>110-220 hrs at 110 °C 85% RH</td>
<td>145-240 hrs at 110 °C 85% RH</td>
</tr>
<tr>
<td>High operating temperature and short duration high temperature exposures</td>
<td>Bake</td>
<td>T = 95 - 105 °C (contact)</td>
<td>700 - 2500 hrs at 125 °C</td>
<td>800 - 3300 hrs at 125 °C</td>
</tr>
</tbody>
</table>
A.2 Intel Reference Component Validation

Intel tests reference components individually and as an assembly on mechanical test boards and assesses performance to the envelopes specified in previous sections by varying boundary conditions.

While component validation shows a reference design is tenable for a limited range of conditions, customers need to assess their specific boundary conditions and perform reliability testing based on their use conditions.

Intel reference components are also used in board functional tests to assess performance for specific conditions.

A.3 Ecological Requirement

Material should be resistant to fungal growth. Examples of non-resistant materials include cellulose materials, animal and vegetable based adhesives, grease, oils, and many hydrocarbons. Synthetic materials such as PVC formulations, certain polyurethane compositions (for example, polyester and some polyethers), plastics which contain organic fillers of laminating materials, paints, and varnishes also are susceptible to fungal growth. If materials are not fungal growth resistant, then MIL-STD-810E, Method 508.4 must be performed to determine material performance.

Cadmium should not be used in the painting or plating of the socket. CFCs and HFCs should not be used in manufacturing the socket.
Any plastic component exceeding 25 gm should be recyclable per the European Blue Angel recycling standards.

Supplier is responsible for complying with industry standards regarding environmental care as well as with the specific standards required per the supplier’s region. More specifically, the supplier is responsible for compliance with the European regulations related to restrictions on the use of lead and bromine containing flame-retardants.

Legislation varies by geography, European Union (RoHS/WEEE), China, California, and so forth.

The following definitions apply to the use of the terms lead-free, Pb-free, and RoHS compliant.

**Halogen flame retardant free (HFR-Free) PCB:** Current guidance for the socket pad layout supports FR4 and HFR-free designs. In future revisions of this document, Intel will be providing guidance on the mechanical impact to using a HFR-free laminate in the PCB. This will be limited to workstations.

**Lead-free and Pb-free:** Lead has not been intentionally added, but lead may still exist as an impurity below 1000 ppm.

**RoHS compliant:** Lead and other materials banned in the RoHS directive are either (1) below all applicable substance thresholds as proposed by the EU or (2) an approved/pending exemption applies.

**Note:** RoHS implementation details are not fully defined and may change.
# Processor Package Mechanical Drawings

Table B-1 lists the processor Package Mechanical Drawings (PMD) included in this chapter.

<table>
<thead>
<tr>
<th>Drawing Description</th>
<th>Figure Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMD XCC: Non-Fabric Form Factor</td>
<td>Figure B-1</td>
</tr>
<tr>
<td>PMD HCC Form Factor</td>
<td>Figure B-2</td>
</tr>
<tr>
<td>PMD LCC Form Factor</td>
<td>Figure B-3</td>
</tr>
</tbody>
</table>
Figure B-2. PMD HCC Form Factor (Sheet 1 of 3)
Figure B-2. PMD HCC Form Factor (Sheet 2 of 3)
Figure B-2. PMD HCC Form Factor (Sheet 3 of 3)
Figure B-3. PMD LCC Form Factor (Sheet 1 of 3)
Figure B-3. PMD LCC Form Factor (Sheet 2 of 3)
Figure B-3. PMD LCC Form Factor (Sheet 3 of 3)

<table>
<thead>
<tr>
<th>Change</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>09/02/19</td>
<td>REVISED HOLE LOCATION A5.0</td>
</tr>
<tr>
<td></td>
<td>01/16/19</td>
<td>REVISED HOLE LOCATION A4.5</td>
</tr>
<tr>
<td></td>
<td>12/20/18</td>
<td>REVISED AS PER INCOGRAPHER</td>
</tr>
<tr>
<td></td>
<td>02/28/19</td>
<td>REVISED PACKAGING LAYOUT</td>
</tr>
<tr>
<td></td>
<td>02/28/19</td>
<td>REVIEW PACKAGING LAYOUT</td>
</tr>
<tr>
<td></td>
<td>03/15/19</td>
<td>REVISED AS PER INCOGRAPHER</td>
</tr>
<tr>
<td></td>
<td>03/25/19</td>
<td>REVISED PACKAGING LAYOUT</td>
</tr>
<tr>
<td></td>
<td>03/25/19</td>
<td>REVIEW PACKAGING LAYOUT</td>
</tr>
</tbody>
</table>

[Diagram of PMD LCC Form Factor]

Second Generation Intel® Xeon® Scalable Processors
Thermal/Mechanical Specifications and Design Guide, August 2019
Table C-1 lists the socket drawings included in this chapter.

Table C-1. Socket Drawing List

<table>
<thead>
<tr>
<th>Drawing Description</th>
<th>Figure Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Socket Mechanical Drawing</td>
<td>Figure C-1</td>
</tr>
</tbody>
</table>
Figure C-1. Socket Mechanical Drawing (Sheet 1 of 4)

NOTES:
1. THE PURPOSE OF THIS DRAWING IS TO ESTABLISH THE MECHANICAL FORM FACTOR OF THE SOCKET.
   THE DRAWING IS NOT INTENDED TO SHOW INTERNAL DETAIL OF THE SOCKET WHICH MAY VARY
   FROM SUPPLIER.
2. MATERIAL:
   DIA, ENG. CAP, AND PAINT SPECIFICATIONS MAY VARY.
   KEY: BARREL - HIGH TEMPERATURE NICKEL 300.
3. FINISH: HOE.
4. FIN AT CHAMFER.

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN MILLIMETERS.
INCHES ARE EQUAL TO MILLIMETERS.

INTERNATIONAL UNITS INTERPRETED AND USED FOR ACME TITANS ONLY.
Figure C-1. Socket Mechanical Drawing (Sheet 2 of 4)
Figure C-1. Socket Mechanical Drawing (Sheet 3 of 4)
Figure C-1. Socket Mechanical Drawing (Sheet 4 of 4)
## D Retention Assembly Mechanical Drawings

### D.1 Processor Heatsink Loading Mechanism (PHLM) Drawings

Table D-1 lists the mechanical drawings that are used in the loading mechanism of the Second Generation Intel® Xeon® Scalable Processors based platform.

<table>
<thead>
<tr>
<th>Description</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bolster Guide Post - Small</td>
<td>Figure D-1</td>
</tr>
<tr>
<td>Bolster Guide Post - Large</td>
<td>Figure D-2</td>
</tr>
<tr>
<td>Backplate Stud</td>
<td>Figure D-3</td>
</tr>
<tr>
<td>Spring Rivet</td>
<td>Figure D-4</td>
</tr>
<tr>
<td>Bolster Captive Nut</td>
<td>Figure D-5</td>
</tr>
<tr>
<td>Bolster Captive Nut Collar</td>
<td>Figure D-6</td>
</tr>
<tr>
<td>Narrow Backplate</td>
<td>Figure D-7</td>
</tr>
<tr>
<td>Narrow Backplate Insulator</td>
<td>Figure D-8</td>
</tr>
<tr>
<td>Narrow-Fabric Bolster Plate</td>
<td>Figure D-9</td>
</tr>
<tr>
<td>Narrow Bolster Plate</td>
<td>Figure D-10</td>
</tr>
<tr>
<td>Narrow Bolster Insulator</td>
<td>Figure D-11</td>
</tr>
<tr>
<td>Narrow CPU Carrier</td>
<td>Figure D-12</td>
</tr>
<tr>
<td>Narrow Backplate Assembly</td>
<td>Figure D-13</td>
</tr>
<tr>
<td>Narrow Dust Cover</td>
<td>Figure D-14</td>
</tr>
<tr>
<td>Narrow Spring Assembly</td>
<td>Figure D-15</td>
</tr>
<tr>
<td>Narrow Spring</td>
<td>Figure D-16</td>
</tr>
<tr>
<td>Narrow - Fabric Bolster Plate Assembly</td>
<td>Figure D-17</td>
</tr>
<tr>
<td>Narrow Bolster Plate Assembly</td>
<td>Figure D-18</td>
</tr>
<tr>
<td>Bolster Corner Standoff</td>
<td>Figure D-19</td>
</tr>
<tr>
<td>Narrow Spring Stud</td>
<td>Figure D-20</td>
</tr>
<tr>
<td>Backplate Stud: Long</td>
<td>Figure D-21</td>
</tr>
<tr>
<td>Narrow Backplate Long Stud Assembly</td>
<td>Figure D-22</td>
</tr>
</tbody>
</table>
## D.2 PHLM Narrow (NRW) Drawings

Table D-2 lists the mechanical drawings included in the NRW processor heatsink loading mechanism configuration.

### Table D-2. NRW Mechanical Drawing List

<table>
<thead>
<tr>
<th>Description</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Narrow Bolster Plate Assembly</td>
<td>Figure D-18</td>
</tr>
<tr>
<td>• Bolster Guide Post - Small</td>
<td>Figure D-1</td>
</tr>
<tr>
<td>• Bolster Guide Post - Large</td>
<td>Figure D-2</td>
</tr>
<tr>
<td>• Spring Rivet</td>
<td>Figure D-4</td>
</tr>
<tr>
<td>• Bolster Captive Nut</td>
<td>Figure D-5</td>
</tr>
<tr>
<td>• Bolster Captive Nut Collar</td>
<td>Figure D-6</td>
</tr>
<tr>
<td>• Narrow Bolster Plate</td>
<td>Figure D-10</td>
</tr>
<tr>
<td>• Narrow Bolster Insulator</td>
<td>Figure D-11</td>
</tr>
<tr>
<td>• Narrow Spring Assembly</td>
<td>Figure D-15</td>
</tr>
<tr>
<td></td>
<td>Narrow Spring Stud</td>
</tr>
<tr>
<td></td>
<td>Narrow Spring</td>
</tr>
<tr>
<td>• Bolster Corner Standoff</td>
<td>Figure D-19</td>
</tr>
<tr>
<td>Narrow Backplate Assembly</td>
<td>Figure D-13</td>
</tr>
<tr>
<td>• Backplate Stud</td>
<td>Figure D-3</td>
</tr>
<tr>
<td>• Narrow Backplate</td>
<td>Figure D-7</td>
</tr>
<tr>
<td>• Narrow Backplate Insulator</td>
<td>Figure D-8</td>
</tr>
<tr>
<td>Narrow Backplate Long Stud Assembly</td>
<td>Figure D-22</td>
</tr>
<tr>
<td>• Backplate Stud: Long</td>
<td>Figure D-21</td>
</tr>
<tr>
<td>• Narrow Backplate</td>
<td>Figure D-7</td>
</tr>
<tr>
<td>• Narrow Backplate Insulator</td>
<td>Figure D-8</td>
</tr>
<tr>
<td>Narrow Dust Cover</td>
<td>Figure D-14</td>
</tr>
<tr>
<td>Narrow CPU Carrier</td>
<td>Figure D-12</td>
</tr>
</tbody>
</table>
Figure D-1. Bolster Guide Post - Small

NOTES: UNLESS OTHERWISE SPECIFIED:
1. REFERENCE DOCUMENTS
   ASME Y14.5M-2009 - STANDARD DIMENSION AND TOLERANCES
2. FEATURES NOT SPECIFIED ON DRAWING AND FEATURES WITHOUT SPECIFIED TOLERANCE
   SHALL BE CONTROLLED BY 3D CAD DATABASE. FOR FEATURES NOT EXPLICITLY TOLERANCED:
   (BASIC DIMENSIONS FROM THE 3D CAD MODEL.)
3. DIMENSIONS ARE IN MILLIMETERS
4. MATERIAL: 18-8 STAINLESS STEEL; AISI 301, 304, 305; JIS SUS304; OR EQUIVALENT
5. PROCESS TEST: 168 HRS 85° C / 85% HUMIDITY WITH NO VISIBLE CORROSION.
6. DIMENSIONS MARKED △ ARE CRITICAL TO FUNCTION DIMENSIONS (CTF).
△ SUPPLIER DEFINED DIAMETER TO MEET PRESS FIT SEPARATION FORCE REQUIREMENT.
△ APPLICABLE BOLSTER PLATE ASSEMBLY DRAWING.
 pushout force > 89N (20lbf)
- CHAMFER TO CORNER BASE 12 DEGREES OR 1.5MM
- FOR STRUCTURAL INTEGRITY DURING ASSEMBLY
- PUSHOUT FORCE > 89N (20LBF)

PARTS LIST

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>PART NUMBER</th>
<th>ITEM NO</th>
<th>QTY</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOLSTER SMALL GUIDE POST</td>
<td>G93935-003</td>
<td>TOP</td>
<td>1</td>
</tr>
</tbody>
</table>

Dimensions:
- Ø3.5 ±0.1
- 20±0.25
Figure D-2. Bolster Guide Post - Large

NOTES: UNLESS OTHERWISE SPECIFIED:

1. REFERENCE DOCUMENTS
   ASME Y14.5M-2009 - STANDARD DIMENSION AND TOLERANCES

2. FEATURES NOT SPECIFIED ON DRAWING AND FEATURES WITHOUT SPECIFIED TOLERANCE
   SHALL BE CONTROLLED BY 3D CAD DATABASE. FOR FEATURES NOT EXPLICITLY TOLERANCED:
   (BASIC DIMENSIONS FROM THE 3D CAD MODEL).

3. DIMENSIONS ARE IN MILLIMETERS

4. MATERIAL: 18-8 STAINLESS STEEL; AISI 303, 304, 305; JIS SUS304; OR EQUIVALENT

5. PROCESS TEST: 168 HOURS 85°C 85% HUMIDITY WITH NO VISIBLE CORROSION.

6. DIMENSIONS MARKED □ ARE CRITICAL TO FUNCTION DIMENSIONS (CTF).

SUPPLIER DEFINED DIAMETER TO MEET PRESS FIT SEPARATION FORCE REQUIREMENT.
SEE APPLICABLE BOLSTER PLATE ASSEMBLY DRAWING.

- PUSHOUT FORCE > 89N (20LBF)

Chamfer to corner (max 1.0 height) or 1.0mm radius max can be added as an option for structural integrity during assembly.

PARTS LIST

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>PART NUMBER</th>
<th>ITEM NO</th>
<th>QTY</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOLSTER LARGE GUIDE POST</td>
<td>G94443-003</td>
<td>TOP</td>
<td>1</td>
</tr>
</tbody>
</table>
Figure D-3. Backplate Stud

**Notes:**
1. Reference Documents:
   - ASME Y14.5-2009: Standard Dimension and Tolerances
   - UL 1439: UL Sharp Edge Testing
2. Features not specified on drawing without specified tolerance shall be controlled by 3D CAD database. For features not explicitly tolerated, (basic dimensions from the 3D CAD model).
3. Material:
   - SUS 416
   - Critical Mechanical Properties: 400 MPa min
   - Process Test: 188 hours 85°C/85% Humidity with no visible corrosion
4. Dimensions marked * are critical to function and
   - Dimensions (CTF)
   - Feature detail per vendor specification
5. Must meet durability specifications defined in the assembly drawing.
6. Reference and non-dimensional features may be modified per Intel Approval.

**M3 x 0.5 Class 6g External "Rolled" Thread**

**Chamfer 0.31 x 45° All Around**

**Feature Defined by Press Fit in Assembly.**

**Parts List**

<table>
<thead>
<tr>
<th>Description</th>
<th>Part Number</th>
<th>Item No</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>SKT P M3 Backplate Stud, Short</td>
<td>H12853-004</td>
<td>TOP</td>
<td>1</td>
</tr>
</tbody>
</table>

**Design Notes:**
- Dimensions are in millimeters.
- Third angle projection.

**Revision History**
- 01 Tooling Release 08/20/14
- 02 1. Increase stud length to 7mm. 2. Added CTF for threads to be rolled not cut. 12/1/14
- 03 1. Decreased stud length from 7mm to 6.334mm. 2. Updated notes. 3/26/15
- 04 1. Changed note 4 critical to function symbol. 4/23/15
- 05 1. Updated notes. 9/11/15
- 06 1. Changed the height from 6.334 to 6.72. 2. Part number rolled from H12853-003 to H12853-004. 2/11/16
- 07 1. Removed CTF dimensions. 7/11/16
Figure D-4. Spring Rivet

NOTES:
1. REFERENCE DOCUMENTS
   ASME Y14.5M-2009 - STANDARD DIMENSION AND TOLERANCES
   UL1439 - UL SHARP EDGE TESTING
2. FEATURES NOT SPECIFIED ON DRAWING SHALL BE CONTROLLED BY
   3D CAD DATABASE. FOR FEATURES NOT EXPLICITLY TOLERANCED:
   (BASIC DIMENSIONS FROM THE 3D CAD DATABASE)
3. CRITICAL MATERIAL PROPERTIES:
   - RIVET FAILURE LOAD > 500N (112LB)
   - RIVET MUST NOT SHEAR, DEFORM, OR CRACK BELOW LOAD LIMIT.
   - SEE ASSEMBLY DRAWING H77470/H77929/H78203/H78902 FOR DETAILS
   Finish:
   - PROCESS TEST: 168 HRS 85°C / 85% HUMIDITY WITH NO
   VISIBLE CORROSION
4. RIVET LENGTH DETERMINED BY ASSEMBLY DRAWING H77470/H77929/H78203/H78902
5. REFERENCE AND NON-DIMENSIONED FEATURES MAY BE MODIFIED
   PER INTEL APPROVAL

FINISH:
- PROCESS TEST: 168 HRS 85°C / 85% HUMIDITY WITH NO
  VISIBLE CORROSION

4. RIVET LENGTH DETERMINED BY ASSEMBLY DRAWING H77470/H77929/H78203/H78902
5. REFERENCE AND NON-DIMENSIONED FEATURES MAY BE MODIFIED
   PER INTEL APPROVAL

REFERENCES:
- ASME Y14.5M-2009 - STANDARD DIMENSION AND TOLERANCES
- UL1439 - UL SHARP EDGE TESTING
- UL1439 - UL SHARP EDGE TESTING

SPECIFICATIONS:
- MATERIAL:
- PROCESS TEST:
  - 168 HRS 85°C / 85% HUMIDITY WITH NO VISIBLE CORROSION

DIMENSIONS ARE IN MILLIMETERS.
THIRD ANGLE PROJECTION
Figure D-5. Bolster Captive Nut

NOTES UNLESS OTHERWISE SPECIFIED
1. REFERENCE DOCUMENTS
   ASME Y14.5M - 2009 - STANDARD DIMENSION AND TOLERANCES
   UL 1439 - UL SHARP EDGE TESTING
2. FEATURES NOT SPECIFIED ON DRAWING SHALL BE CONTROLLED BY
   3D CAD DATABASE. FOR FEATURES NOT EXPLICITLY TOLERANCED:
   (BASIC DIMENSIONS FROM THE 3D CAD MODEL).
3. MATERIAL:
   - LOW CARBON STEEL 1144, HARDEN AND TEMPER
   - CRITICAL MECHANICAL PROPERTIES: 345 MPa MIN YIELD STRENGTH
   - MAY USE INTEL ENGINEERING APPROVED EQUIVALENT
4. FINISH:
   - 2 MICROMETER MIN ELECTROLYTIC NICKEL PLATING
   - PROCESS TEST 168 HRS 85 DEGREE C / 85% HUMIDITY WITH NO
     VISIBLE CORROSION
   - INTERFERENCE FIT WITH PART H19329-003
   - MINIMUM 0.1LBF SEPARATION FORCE WITH PRESS FIT COLLAR
5. SHARP CORNERS MUST BE CHAMFERED, OR ROUNDED TO 0.1MM
   RADIUS MAX
6. DRILL CLEARANCE HOLE TO CLEAN UP CHIP/PLUS FROM TAPPING
   FORMING OPERATIONS. SHOULD ALLOW M3 STUD TO PASS THROUGH
   WITHOUT INTERFERENCE
7. DIMENSIONS MARKED ARE CRITICAL TO FUNCTION
   DIMENSIONS (CTF).

M3 X 0.5 CLASS 6H
INTERNAL THREAD THRU ALL

SECTION A-A

6 Point T-20 Drive Feature T 1.5 ± 0.25

CLEARANCE HOLE Ø5.1
Ø4.32±0.25 X120°
Figure D-6. Bolster Captive Nut Collar

NOTES UNLESS OTHERWISE SPECIFIED

1. REFERENCE DOCUMENTS
   ASME Y14.5M - 2009 - STANDARD DIMENSION AND TOLERANCES
   UL1439 - UL SHARP EDGE TESTING

2. FEATURES NOT SPECIFIED ON DRAWING SHALL BE CONTROLLED BY 3D CAD DATABASE.
   FOR FEATURES NOT EXPLICITLY TOLERANCED:
   (BASIC DIMENSIONS FROM THE 3D CAD MODEL)

3. MATERIAL:
   - ANSI 1215 CARBON STEEL OR EQUIVALENT
   - CRITICAL MECHANICAL PROPERTIES: 415 MPa MIN YIELD STRENGTH
   - MAY USE INTEL ENGINEERING APPROVED EQUIVALENT

4. FINISH:
   - 2 MICRONETER MIN ELECTROLYTIC NICKEL PLATING
   - PROCESS TEST 168 HRS 95 DEGREES C / 95% HUMIDITY WITH NO VISIBLE CORROSION, AFTER MATING WITH PRESS FIT NUT INTERFACE

   FEATURE DEFINED BY VENDOR - FOR INTERFERENCE FIT WITH PART H19328-002
   FEATURE MAY BE MODIFIED WITH INTEL ENGINEERING APPROVAL, IN ORDER TO MEET MINIMUM 50LBF SEPARATION FORCE FOR NUT/COLLAR PRESS FIT INTERFACE

6. SHARP CORNERS MUST BE CHAMFERED, OR ROUNDED TO 0.1MM RADIUS MAX.

7. DIMENSIONS MARKED ∆ ARE CRITICAL TO FUNCTION DIMENSIONS (CTF)

DIMENSIONS ARE IN MILLIMETERS

SECTION A-A
Figure D-7. Narrow Backplate

Notes:
- Reference documents:
  1. ASME Y14.5M-2009 - Standard Dimension and Tolerance
  2. UL1439 - UL Sharp Edge Testing
  3. INTEL MARKING STANDARD
  4. A29419 - Intel Tolerance Standard for Sheet Metal
  5. C25432 - Intel Cosmetic Spec for Sheet Metal

- Features not specified on drawing and features without specified tolerances shall be controlled by 3D CAD database, and shall conform to sheet metal tolerance standard (A29419).
- For features not explicitly toleranced:
  - (Basic dimensions from the 3D model)

- Material:
  - A) Type: Sheet Steel, SK7, 1065, S50C, or CHSP60PC - 2.2 MM +/− 0.05 THK
  - Critical Mechanical Properties:
    - Heat treated to 250 MPa minimum yield
    - Tensile Yield Strength (ASTM D638) ≥ 250 MPa
    - Ultimate Tensile Strength (ASTM D638) ≥ 300 MPa

- Plating:
  - 2 Micron Minimum Electrolytic Nickel Plating

- Final location and orientation of press fit stud in Assy DRAWING H77928 must be met and takes precedence over this drawing.

- Part shall be free of oil and debris.

- Burr heights shall not exceed 0.10 MM.

- Sharp corners must be chamfered or rounded to 0.25 MM max.

- Dimensions marked with "C" are critical to function.

- Flatness to be controlled on the backplate assembly drawing H77928.

- Dimensions (CTF) without specification.

- All dimensions are in mm.

- Third Angle Projection.
Figure D-8. Narrow Backplate Insulator
Figure D-9. Narrow-Fabric Bolster Plate (Sheet 1 of 3)
Figure D-9. Narrow-Fabric Bolster Plate (Sheet 2 of 3)
SUPPLEMENTAL OPTIONS TO IMPROVE DESIGN FOR MANUFACTURING

2X DIAMETER CAN VARY WITH MATING OBJECT AS SHOWN IN ASSEMBLY H95384-004

SEE DETAIL B

SCALE 1:10

DETAIL B

SCALE 1:10
Figure D-10. Narrow Bolster Plate (Sheet 1 of 3)
SUPPLEMENTAL OPTIONS TO IMPROVE DESIGN FOR MANUFACTURING

12X 0.2  -0.2

2X DIAMETER CAN VARY WITH MATING OBJECT AS SHOWN IN ASSEMBLY H95385-004
Figure D-11. Narrow Bolster Insulator

DIMENSIONS ARE IN MILLIMETERS
THIRD ANGLE PROJECTION

NOTES
1. REFER TO DOCUMENTS:
   a) ASME Y14.5M-2009 - STANDARD DIMENSION AND TOLERANCE
   b) G14599 - INTEL MARKING STANDARD
2. FEATURES NOT SPECIFIED ON DRAWING ARE CONTROLLED BY 3D CAD DATABASE.
   FOR FEATURES NOT EXPLICITLY TOLERANCED:
   BASIC DIMENSIONS FROM 3D CAD DATABASE
3. MATERIAL:
   a) PC-1860B (CHENGDU KANGLONGXIN PLASTICS CO., LTD)
   0.127MM NOMINAL THICKNESS, ONE SIDE ADHESIVE APPLIED.
   TOTAL THICKNESS = 0.18MM.
   b) FLAMMABILITY: UL 94-V0 OR VTM-0 RATING.
4. APPLY ADHESIVE TO THE TOP SIDE.
5. DIMENSIONS MARKED WITH \( \bigtriangleup \) ARE CRITICAL TO FUNCTION DIMENSIONS (CTF).

PARTS LIST

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>QTY</th>
</tr>
</thead>
<tbody>
<tr>
<td>H64296-002</td>
<td>TOP BOLSTER INSULATOR</td>
<td>1</td>
</tr>
<tr>
<td>H64296-002</td>
<td>NON FABRIC BOLSTER INSULATOR</td>
<td>1</td>
</tr>
</tbody>
</table>

REFERENCE DOCUMENTS
a) ASME Y14.5M-2009 - STANDARD DIMENSION AND TOLERANCE
b) G14599 - INTEL MARKING STANDARD

APPLICATIONS
- INTERFACE TO INTEL'S MOTHERBOARD, SET TOP COVER, TOP COVER INNER, TOP COVER OUTER.
- PLACE ADHESIVE ON THE TOP SIDE.
- MATERIAL MAY BE ELECTROMAGNETICALLY SCREENED.

NOTES
1. DEFLECTED DIMENSIONS
2. MATERIAL: MAY USE INTEL ENGINEERING APPROVED EQUIVALENT.
3. ALL SUBSTANCES IN THIS PART MUST CONFORM TO INTEL ENVIRONMENTAL PRODUCT SPECIFICATION (BS-MTN-0001).
Figure D-12. Narrow CPU Carrier (Sheet 2 of 2)
Figure D-13. Narrow Backplate Assembly (Sheet 1 of 2)
Figure D-14. Narrow Dust Cover (Sheet 1 of 2)

NOTES: UNLESS OTHERWISE SPECIFIED

1. REFERENCE DOCUMENTS:
   ASME Y14.5M-2009 - STANDARD DIMENSION AND TOLERANCES
   SB-007-045 - INTEL WORKMANSHIP STANDARD - SYSTEMS MANUFACTURING
   19-8401 - INTEL ENVIRONMENTAL PRODUCT SPECIFICATION FOR
   SUPPLIERS & OUTSOURCED MANUFACTURERS
   WEBSITE: https://supplier.intel.com/wmvs/

2. FEATURES NOT SPECIFIED ON DRAWING AND FEATURES WITHOUT
   SPECIFIED TOLERANCE SHALL BE CONTROLLED BY 3D CAD DATABASE

3. MATERIAL MAY USE INTEL ENGINEERING APPROVED EQUIVALENT.
   ALL SUBSTANCES IN THIS PART MUST CONFORM TO INTEL ENVIRONMENTAL
   PRODUCT SPECIFICATION (AS XTN-807):
   A) PC-ABS (V0 FLAME RATING AND MUST PASS 105°C BAKE TEST)
   B) COLOR: BLACK

4. FINISH: UNSPECIFIED SURFACES MUST CONFORM WITH CLASS C
   REQUIREMENTS.
   PARTS MUST BE FREE OF OIL AND DEBRIS.
   DEBURR ALL SHARP EDGES.

   USE "LGA Socket X Retention Plate Marking Guideline"
   INTEL DOCUMENT NUMBER G14577 TO MARK PART IN AREA SHOWN.

5. DIMENSIONS MARKED are CRITICAL TO FUNCTION Dimensions (CTF).

6. DIMENSIONS MARKED are CRITICAL TO FUNCTION Dimensions (CTF).
Figure D-15. Narrow Spring Assembly
Figure D-16. Narrow Spring

NOTE
1. REFERENCE DOCUMENTS
   - ASME Y14.5M-2009 - STANDARD DIMENSION AND TOLERANCES
   - UL1439 - UL SHARP EDGE TESTING
   - A29419 - INTEL STANDARD FOR SHEETMETAL
2. FEATURES NOT SPECIFIED ON DRAWING AND FEATURES WITHOUT SPECIFIED TOLERANCES SHALL BE CONTROLLED BY 3D CAD DATABASE, AND SHALL CONFORM TO INTEL SHEETMETAL TOLERANCE STANDARD (A29419) FOR FEATURES NOT EXPLICITLY TOLERANCED: (BASIC DIMENSIONS FROM THE 3D CAD MODEL).
3. MATERIAL: MAY USE INTEL ENGINEERING APPROVED EQUIVALENT. ALL SUBSTANCES IN THIS PART MUST CONFORM TO INTEL ENVIRONMENTAL PRODUCT SPECIFICATION (BS-MTN-0001).
   A) TYPE SUS301, 1.2MM .05 THK.
   B) CRITICAL MECHANICAL PROPERTIES:
      - YIELD STRENGTH (ASTM D638) MINIMUM = 965 MPa.
   C) PLATING: NONE.
   D) HEAT TREATING: AS REQUIRED

4. BURR HEIGHTS SHALL NOT EXCEED 0.15MM.
5. SHARP CORNERS MUST BE CHAMFERED OR ROUNDED TO 0.25MM RADIUS MAX.
6. SEE BOLSTER... H95384-001 OR H95385-001 FOR FIT REQUIREMENTS.
7. DIMENSIONS MARKED WITH * ARE CRITICAL TO FUNCTION.
8. OPTIONAL STRESS RELIEF ALLOWED IF MINIMUM LOAD REQUIREMENT IS NOT MET. SEE LOAD TEST PROCEDURE, DOCUMENT # H95020. LOAD VALUE WILL NEED TO BE CHECKED FOR EVERY NEW MATERIAL LOT.

RETENTION ASSEMBLY MECHANICAL DRAWINGS

SECOND GENERATION INTEL® XEON® SCALABLE PROCESSORS
THERMAL/MECHANICAL SPECIFICATIONS AND DESIGN GUIDE, AUGUST 2019
Figure D-17. Narrow - Fabric Bolster Plate Assembly (Sheet 1 of 2)
Figure D-17. Narrow - Fabric Bolster Plate Assembly (Sheet 2 of 2)
Figure D-18. Narrow Bolster Plate Assembly (Sheet 2 of 2)

- 4X BOLSTER INSTALLATION HOLES.
- LOCATION MUST ALLOW T-20 DRIVER TO TIGHTEN H19328 NUTS IN ASSEMBLED STATE.
- ADJUST HOLE LOCATIONS IN H95196 AS NEEDED.
- NO METAL CAN BE EXPOSED.
- OVERHANG OF INSULATOR ON INNER EDGES OF THE BOLSTER-PLATE IS ACCEPTABLE.
- PRE-CONDITION THE SPRING BY EITHER PULLING UP (ON THE SPRING STUD) OR PUSHING UP (ON THE BOTTOM CENTER OF THE STUD HEAD) IN THE DIRECTION OF THE ARROW TO 3.1MM.
- OVERHANG OF INSULATOR ON INNER AND OUTER EDGES OF THE BOLSTER-PLATE IS ACCEPTABLE.
- 4X BULGING OF RIVET HEAD ON THIS SIDE IS ACCEPTABLE, NOT TO EXCEED 2.5MM.
- 2X LASER WELD OR RIVET POST ONTO BOLSTER PLATE, NO MATERIAL TO PROTRUDE BEYOND BOTTOM SURFACE.
- SPRING STUD TO BOLSTER FRAME GAP (BEFORE PRE CONDITIONING)
- 2X (5.5) M4 MAJOR DIAMETER
- POST PRE CONDITIONING
- 2X (3.5) M4 MAJOR DIAMETER
- NUT ASSEMBLY SEQUENCE FOR 6 CYCLES.
- ASSEMBLE THEN REMAINING NUTS IN ANY ORDER.
- DISASSEMBLE IN REVERSE ORDER OF ASSEMBLY.
- NUT ASSEMBLY SEQUENCE FOR 6 CYCLES.
NOTES: UNLESS OTHERWISE SPECIFIED:
1. REFERENCE DOCUMENTS:
   ASME Y14.5M-2009 - STANDARD DIMENSION AND TOLERANCES
2. FEATURES NOT SPECIFIED ON DRAWING AND FEATURES WITHOUT SPECIFIED TOLERANCES SHALL BE
   CONTROLLED BY 3D CAD MODELS. (DIMENSIONS FROM 3D CAD MODEL)
3. DIMENSIONS ARE IN MILLIMETERS
4. MATERIAL: SUS 416. ALL STUD THREADS REQUIRE APPROVED LUBRICANTS BY INTEL. CONTACT INTEL FOR THE LIST OF APPROVED LUBRICANTS.
5. PROCESS TEST: 168 HRS 85°C 85% HUMIDITY WITHOUT VISIBLE CORROSION.
   MINIMUM RADIUS FOR DUST COVER INTERFACE.
6. ROLLED THREADS.
   (SUPPLIED DEFINED DIA TO MEET PRESS FIT SEPARATION FORCE REQUIREMENT
   PLUS HIPS TO ENSURE ELECTROPLATED PLATE ASSEMBLY DRAWING.
   - PULLOUT FORCE = 445N (100LBF).
   - TORQUE OUT = 2.25 N-m (20 IN-LBF).
7. DIMENSIONS MARKED WITH ** CRITICAL TO FUNCTION DIMENSIONS (CTF)

PARTS LIST

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>PART NUMBER</th>
<th>ITEM NO</th>
<th>QTY</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOLSTER CORNER STANDOFF</td>
<td>H96570-002</td>
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</tbody>
</table>

DETAIL A

SCALE: 16:1
Figure D-20. Narrow Spring Stud

NOTES:
1. REFERENCE DOCUMENTS
   ASME Y14.5M-2009 - STANDARD DIMENSION AND TOLERANCES
   UL1439 - UL SHARP EDGE TESTING
2. FEATURES NOT SPECIFIED ON DRAWING SHALL BE CONTROLLED BY
   3D CAD DATABASE. FOR FEATURES NOT EXPLICITLY TOLERANCED:
   (BASIC DIMENSIONS FROM THE 3D CAD MODEL)
3. MATERIAL: SUS416
   -MINIMUM SURFACE HARDNESS EQUIVALENT TO BRINELL HARDNESS (HB) 342 OR
   VICKERS HARDNESS (HV) 360.
   -CRITICAL MATERIAL PROPERTIES: 400 MPA MIN YIELD STRENGTH
   - PROCESS TEST: 168 HRS 85º C / 85% HUMIDITY WITH NO
   VISIBLE CORROSION
   -REFERENCE AND NON-DIMENSIONED FEATURES MAY BE MODIFIED
   △ PER INTEL APPROVAL
   5 ROLLED THREADS
   △ NOT USED.
   6 DIMENSIONS MARKED WITH △ CRITICAL TO FUNCTION DIMENSIONS (CTF).
   8 GEOMETRY ON VENDOR DISCRETION, UPON INTEL APPROVAL.

 Dimensions marked with △ are critical to function dimensions (CTF).
Figure D-21. Backplate Stud: Long

NOTES:
1. REFERENCE DOCUMENTS
   ASME Y14.5-2009-STANDARD DIMENSION AND TOLERANCES
   UL 1439 - UL SHARP EDGE TESTING
2. FEATURES NOT SPECIFIED ON DRAWING WITHOUT SPECIFIED
   TOLERANCE SHALL BE CONTROLLED BY 3D CAD DATABASE. FOR
   FEATURES NOT EXPLICITLY TOLERANCED: (BASIC DIMENSIONS
   FROM THE 3D CAD MODEL):
3. MATERIAL:
   - SUS 416 - MECHANICAL PROPERTIES: 400 MPa MIN
   - PROCESS TEST: 168 HRS 85°C / 85% HUMIDITY WITH NO
     MOBILE CORROSION
4. DIMENSIONS MARKED ** ARE CRITICAL TO FUNCTION
5. FEATURE DETAIL PER VENDOR SPECIFICATION
   MUST MEET DURABILITY SPECIFICATIONS DEFINED IN
   ASSEMBLY DRAWING
6. REFERENCE AND NON-DIMENSIONED FEATURES MAY BE MODIFIED
   PER INTEL APPROVAL

7. DIMENSIONS MARKED * ARE CRITICAL TO FUNCTION
   DIMENSIONS (CTF).
8. FEATURE DEFINED BY PRESS FIT IN ASSEMBLY.

DIMENSIONS ARE IN MILLIMETERS
THIRD ANGLE PROJECTION

PARTS LIST

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>PART NUMBER</th>
<th>ITEM NO</th>
<th>QTY</th>
</tr>
</thead>
<tbody>
<tr>
<td>SKT P M3 BACKPLATE STUD, LONG</td>
<td>J20889</td>
<td>001</td>
<td>TOP</td>
</tr>
</tbody>
</table>

M3x0.5 CLASS 6g EXTERNAL "ROLLED" THREAD
CHAMFER 0.31 x 45° ALL AROUND
Figure D-22. Narrow Backplate Long Stud Assembly (Sheet 1 of 2)
Figure D-22. Narrow Backplate Long Stud Assembly (Sheet 2 of 2)
## Heatsink Mechanical Drawings

### E.1 Heatsink Drawings

Table E-1 lists the reference heatsink mechanical drawings that are used in the Second Generation Intel® Xeon® Scalable Processors based platform.

<table>
<thead>
<tr>
<th>Description</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>2U Heatsink Assembly</td>
<td>Figure E-1</td>
</tr>
<tr>
<td>2U Heatsink Heatpipe: Small</td>
<td>Figure E-2</td>
</tr>
<tr>
<td>2U Heatsink Heatpipe: Large</td>
<td>Figure E-3</td>
</tr>
<tr>
<td>2U Heatsink Copper Slug</td>
<td>Figure E-4</td>
</tr>
<tr>
<td>2U Heatsink Aluminum Base</td>
<td>Figure E-5</td>
</tr>
<tr>
<td>2U Heatsink Fin Assembly</td>
<td>Figure E-6</td>
</tr>
<tr>
<td>Delrin Heatsink Washer</td>
<td>Figure E-7</td>
</tr>
<tr>
<td>TIM PCM45F</td>
<td>Figure E-8</td>
</tr>
<tr>
<td>1U Heatsink Assembly</td>
<td>Figure E-9</td>
</tr>
<tr>
<td>1U Heatsink</td>
<td>Figure E-10</td>
</tr>
<tr>
<td>1U Extruded Heatsink Assembly</td>
<td>Figure E-11</td>
</tr>
<tr>
<td>1U Extruded Heatsink</td>
<td>Figure E-12</td>
</tr>
<tr>
<td>Heatsink Label</td>
<td>Figure E-13</td>
</tr>
<tr>
<td>Heatsink Collar</td>
<td>Figure E-14</td>
</tr>
<tr>
<td>Heatsink Nut</td>
<td>Figure E-15</td>
</tr>
<tr>
<td>Extruded Aluminum Heatsink Label</td>
<td>Figure E-16</td>
</tr>
</tbody>
</table>
E.2 1U Copper Base Heatsink Drawings

Table E-2 lists the mechanical drawings that compose the 1U Copper Base heatsink configuration.

Table E-2. 1U Copper Base Heatsink Drawing List

<table>
<thead>
<tr>
<th>Description</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>1U Heatsink Assembly</td>
<td>Figure E-9</td>
</tr>
<tr>
<td>• Delrin Heatsink Washer</td>
<td>Figure E-7</td>
</tr>
<tr>
<td>• TIM PCM45F</td>
<td>Figure E-8</td>
</tr>
<tr>
<td>• 1U Heatsink</td>
<td>Figure E-10</td>
</tr>
<tr>
<td>• Heatsink Label</td>
<td>Figure E-13</td>
</tr>
<tr>
<td>• Heatsink Collar</td>
<td>Figure E-14</td>
</tr>
<tr>
<td>• Heatsink Nut</td>
<td>Figure E-15</td>
</tr>
</tbody>
</table>

E.3 1U Extruded Aluminum Heatsink Drawings

Table E-3 lists the mechanical drawings that compose the 1U Extruded Aluminum heatsink configuration.

Table E-3. 1U Extruded Aluminum Heatsink Drawing List

<table>
<thead>
<tr>
<th>Description</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>1U Extruded Heatsink Assembly</td>
<td>Figure E-11</td>
</tr>
<tr>
<td>• Delrin Heatsink Washer</td>
<td>Figure E-7</td>
</tr>
<tr>
<td>• TIM PCM45F</td>
<td>Figure E-8</td>
</tr>
<tr>
<td>• 1U Extruded Heatsink</td>
<td>Figure E-12</td>
</tr>
<tr>
<td>• Heatsink Collar</td>
<td>Figure E-14</td>
</tr>
<tr>
<td>• Heatsink Nut</td>
<td>Figure E-15</td>
</tr>
<tr>
<td>• Extruded Aluminum Heatsink Label</td>
<td>Figure E-16</td>
</tr>
</tbody>
</table>

E.4 2U Passive Heatsink Drawing

Table E-4 lists the mechanical drawings that compose the 2U Passive heatsink configuration.

Table E-4. 2U Passive Heatsink Drawing List (Sheet 1 of 2)

<table>
<thead>
<tr>
<th>Description</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>2U Heatsink Assembly</td>
<td>Figure E-1</td>
</tr>
<tr>
<td>• 2U Heatsink Heatpipe: Small</td>
<td>Figure E-2</td>
</tr>
<tr>
<td>• 2U Heatsink Heatpipe: Large</td>
<td>Figure E-3</td>
</tr>
<tr>
<td>• 2U Heatsink Copper Slug</td>
<td>Figure E-4</td>
</tr>
<tr>
<td>• 2U Heatsink Aluminum Base</td>
<td>Figure E-5</td>
</tr>
<tr>
<td>• 2U Heatsink Fin Assembly</td>
<td>Figure E-6</td>
</tr>
<tr>
<td>• Delrin Heatsink Washer</td>
<td>Figure E-7</td>
</tr>
<tr>
<td>• TIM PCM45F</td>
<td>Figure E-8</td>
</tr>
</tbody>
</table>
### Table E-4. 2U Passive Heatsink Drawing List (Sheet 2 of 2)

<table>
<thead>
<tr>
<th>Description</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heatsink Label</td>
<td>Figure E-13</td>
</tr>
<tr>
<td>Heatsink Collar</td>
<td>Figure E-14</td>
</tr>
<tr>
<td>Heatsink Nut</td>
<td>Figure E-15</td>
</tr>
</tbody>
</table>
Figure E-2. 2U Heatsink Heatpipe: Small
Figure E-4. 2U Heatsink Copper Slug

NOTES: UNLESS OTHERWISE SPECIFIED  
1. ITEM IDENTIFICATION 6, 607, 1000, 3703  
2. FEATURES NOT SPECIFIED ON THE DRAWING SHALL BE CONTROLLED BY THE 3D DATABASE, FOR FEATURES NOT EXPLICITLY TOLERANCED.  
(BASIC DIMENSION FROM 3D CAD MODEL)  
3. REFERENCE DOCUMENTS  
ASME Y14.5M-2009, STANDARD DIMENSION AND TOLERANCES  
ASME Y14.37M-2013, TOLERANCE FOR ASSEMBLY AND STOCK  
4. MATERIAL: COPPER, K=380 W/MK, MIN  
5. REMOVE ALL BURRS, SHARP EDGES, GREASES, AND/OR SOLVENTS AFTER MACHINING.  
6. CRITICAL TO FUNCTION DIMENSION

NAMES OF DRAWING  
2U HEATSINK COPPER SLUG  
DESIGNED BY  
NAME: [REDACTED]  
DATE: 09/25/2014  
REVISED BY  
NAME: [REDACTED]  
DATE: 03/04/2014  
PRINTED BY  
NAME: [REDACTED]  
DATE: 05/06/2015  
INSTRUMENT NUMBER: 12579  
DRAWING NUMBER: 12579  
SHEET 1 OF 1
Figure E-6. 2U Heatsink Fin Assembly

NOTES: UNLESS OTHERWISE SPECIFIED:
1. ITEM IDENTIFICATION IS HP707-001, XF03
2. THE DRAWING TO BE USED IN CONSTRUCTION WITH SUPPLIED 3D DATABASE FILE
3. FEATURES NOT SPECIFIED ON DRAWING SHALL BE CONTROLLED BY THE 3D DATABASE.
4. REFERENCE DOCUMENT: ASME Y14.3A-2009 - STANDARD DIMENSION AND TOLERANCES
5. MATERIAL: ALUMINUM. QTY (40) ALUMINUM, K=220 W/M-K MIN.
6. FINISH: NICKEL
7. REMOVE ALL BURRS, SHARP EDGES, OILS, AND/or SOLVENTS AFTER MACHINING AND FIN ASSEMBLY.
8. MECHANICAL STITCHING OR CONNECTION ALLOWED ON TOP SURFACE OF HEATSINK TO INCREASE FIN ARRAY STRUCTURAL STABILITY, OVERALL FIN HEIGHT MUST BE MAINTAINED.
9. CRITICAL TO FUNCTION DIMENSION.
Figure E-9. 1U Heatsink Assembly (Sheet 1 of 2)
Figure E-9. 1U Heatsink Assembly (Sheet 2 of 2)
Heatsink Mechanical Drawings

Figure E-11. 1U Extruded Heatsink Assembly (Sheet 1 of 2)

NOTES:
1. THIS DRAWING TO BE USED IN CORRELATION WITH SUPPLIED 3D DATABASE FILE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED FILE.

2. FEATURES NOT SPECIFIED ON DRAWING AND FEATURES WITHOUT SPECIFIED TOLERANCES SHALL BE CONTROLLED BY 3D CAD DATABASE. FOR FEATURES NOT EXPLICITLY TOLERANCED:
   BASIC DIMENSIONS FROM THE 3D CAD MODEL

3. REMOVE ALL BURRS, SHARP EDGES, GREASES, AND/OR SOLVENTS AFTER FINAL ASSEMBLY.

4. DIMENSIONS MARKED are critical to function dimensions (CTF)

5. MINIMUM PUSH OUT FORCE = 1 LB PER COLLAR/NUT.

PLACE PART NUMBER, DATE CODE, AND DISPLAYED TEXT IN ALLOWABLE AREA OTHER SIDE OF PART WHERE DRIVEN. THE MARK CAN BE AN INK MARK, LASER MARK, PUNCH MARK OR ANY OTHER PERMANENT MARK THAT IS READABLE AT 1.0X MAGNIFICATION.

PARTS LIST

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
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<tbody>
<tr>
<td>1U EXTRUDED HEATSINK ASMH45651-006</td>
<td>TOP</td>
</tr>
<tr>
<td>SKT-P DELRIN HEATSINK WASHERH37265-004</td>
<td>14</td>
</tr>
<tr>
<td>TIM PCM45F, 47X70MMH38442-001</td>
<td>21</td>
</tr>
<tr>
<td>1U EXTRUDED HEATSINKH45653-002</td>
<td>31</td>
</tr>
<tr>
<td>SKT -P HEATSINK COLLARH94875-004</td>
<td>44</td>
</tr>
<tr>
<td>SKT-P, HEATSINK NUT, M4H98449-003</td>
<td>54</td>
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<tr>
<td>J45423-001</td>
<td>61</td>
</tr>
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</table>

REV. HISTORY

ZONE REVISION DESCRIPTION DATE APPR
- A PRELIMINARY RELEASE 4/28/14
- B UPDATED H45653 11/4/14
- C UPDATED PARTS H19326 AND H45653 12/11/14
- D UPDATED: NOTES, ASSEMBLY NUMBER TO -002, PART H45653-002 ADDED LABEL AND HARDWARE, CHANGED NUT TO H78579-001 04/07/15
- E REMOVED DRAWING REVISION FROM PART MARKING.
- F UPDATED NOTE 2 TO 2009 STANDARD WITH PROFILE TOLERANCE, NOTE 4 WITH NEW CTF SYMBOL, NOTE 5 AND 6 TO TRIANGLE CALLOUTS.
- G H45653-002 REVISED TO REV E. 05/05/15
- H REPLACED H78579-001 NUT TO A NEW T-30 TORX NUT H98449-002. CHANGED HEATSINK DELRIN WASHER INNER DIAMETER, DASH CHANGE TO H37265-004. REPLACED HS COLLAR H19327-001 WITH NEW DELRIN COLLAR H94875-001. ROLLED H45651-002 TO H45651-003. 10/11/15
- I REPLACED DELRIN HS COLLAR H94875-001 WITH NYLON HS COLLAR H94875-002. ROLLED H45651-003 TO H45651-004. 12/21/15
- J ITEM 5 HEATSINK NUT IS NOW -003. ITEM 6 HEATSINK LABEL IS NOW J45423-001. TOP ASSEMBLY NOW H45651-005. PRE PRODUCTION REMOVED FROM PN. NOTE 6 UPDATED, TORQUE SPEC REMOVED. H45653-002 REVISION CHANGE TO -F. 10/26/16
- K ITEM INDENTIFICATION UPDATED TO H45651-006
- L COLLAR DESIGN UPDATED TO H94875-004. 3/9/17
Figure E-12. 1U Extruded Heatsink (Sheet 1 of 2)
Figure E-12. 1U Extruded Heatsink (Sheet 2 of 2)
Figure E-13. Heatsink Label

NOTES, UNLESS OTHERWISE SPECIFIED:

1. REFERENCE DOCUMENTS
   ASME Y14.5M-2009 - STANDARD DIMENSION AND TOLERANCES
   UL1439 - UL SHARP EDGE TESTING

2. FEATURES NOT SPECIFIED ON DRAWING SHALL BE CONTROLLED BY 3D CAD DATABASE.

3. LABEL MATERIAL: PET, APPROXIMATELY 0.15MM THICK, WHITE.

4. LABEL CONTENT: BLACK

5. ADHESIVE: PERMANENT ACRYLIC ADHESIVE, 20 +/-4 GM2

6. RELIABILITY REQUIREMENTS:
   PRINT RESISTIVITY: MUST SUPPORT THERMAL TRANSFER PRINT DURABILITY/RESISTIVITY AGAINST CHEMICAL DEGRADATION. ALL TESTING IN ACCORDANCE WITH MIL STD 883/2015.13
   DURABILITY: MUST DEMONSTRATE DURABILITY IN PRESENCE OF ENVIRONMENTAL CONDITIONS. HUMIDITY (32°C/90%RH FOR 7 DAYS), TEMP CYCLE (-7°C TO 50°C FOR 7 DAYS)
   SHELF LIFE: 1 YEAR (BEFORE APPLICATION) WITHOUT DETRIMENT TO ADHESION OR CONSTRUCTION. IF STORED IN PROPER ENVIRONMENT: 10°C - 25°C, 40%-60% RH, NO SUN EXPOSURE.

7. QUALITY REQUIREMENTS:
   IMAGE FLOAT: 0.75MM IN ANY DIMENSION (X OR Y)
   LABEL ALIGNMENT: DEFINED IN APPLICABLE HEATSINK DRAWING
   LABEL PEELING: LESS THAN OR EQUAL TO 1MM
   SCRATCHES: SCRATCHES/SCUFFING MUST BE LESS THAN OR EQUAL TO 0.03MM ALONG DEPTH AND WIDTH, AND LESS THAN OR EQUAL TO 1.27MM ALONG THE LENGTH.
Figure E-14. Heatsink Collar

NOTES: UNLESS OTHERWISE SPECIFIED:

1. REFERENCE DOCUMENTS
   98-0007-001 - INTEL WORKMANSHIP STANDARD - SYSTEMS MANUFACTURING
   98-14-1201 - INTEL ENVIRONMENTAL PRODUCT CONTENT SPECIFICATION FOR SUPPLIERS & OUTSOURCED MANUFACTURERS (FOUND ON EHS WEBSITE - https://supplier.intel.com/static/EHS/)
   ASME Y14.5-2009 - STANDARD DIMENSION AND TOLERANCES

2. FEATURES NOT SPECIFIED ON DRAWING SHALL BE CONTROLLED BY 3D CAD DATABASE. FOR FEATURES NOT EXPLICITLY TOLERANCED: (BASIC DIMENSIONS FROM THE 3D CAD MODEL):

3. MATERIAL: MAY USE INTEL ENGINEERING APPROVED EQUIVALENT. ALL SUBSTANCES IN THIS PART MUST CONFORM TO INTEL ENVIRONMENTAL PRODUCT SPECIFICATION (BS-MTN-001):
   A) NY66 A205F
   B) PIGMENT: N/A
   C) COLOR: NOT SPECIFIED, HOWEVER BLACK NOT SUGGESTED

4. CRITICAL TO FUNCTION DIMENSION (CTF).

5. PART MUST COMPLY WITH INTEL WORKMANSHIP STANDARD (98-0007-001). PART SHALL BE FREE OF OIL AND DEBRIS. FINISH: UNSPECIFIED SURFACES MUST CONFORM WITH CLASS C REQUIREMENTS.

6. NO GATING ALLOWED ON THIS COMPONENT MATING SURFACE.
Supplemental design that is an alternative
Figure E-16. Extruded Aluminum Heatsink Label

NOTES: UNLESS OTHERWISE SPECIFIED:

1. REFERENCE DOCUMENTS
   ASME Y14.5M-2009 - STANDARD DIMENSION AND TOLERANCES
   UL1439 - UL SHARP EDGE TESTING

2. FEATURES NOT SPECIFIED ON DRAWING SHALL BE CONTROLLED BY 3D CAD DATABASE.

3. LABEL MATERIAL: PET, APPROXIMATELY 0.15MM THICK, WHITE.

4. LABEL CONTENT: BLACK

5. ADHESIVE: PERMANENT ACRYLIC ADHESIVE, 20 ±1 GM2

6. RELIABILITY REQUIREMENTS:
   PRINT RESISTIVITY: MUST SUPPORT THERMAL TRANSFER PRINT DURABILITY/RESISTIVITY AGAINST CHEMICAL DEGRADATION - ALL TESTING IN ACCORDANCE WITH MIL-STD-883/2015.13 DURABILITY MUST DEMONSTRATE DURABILITY IN PRESENCE OF ENVIRONMENTAL CONDITIONS: HUMIDITY 93% RH/48H(7 DAYS), TEMP CYCLE (-70°C TO 50°C FOR 7 DAYS) SHELF LIFE 1 YEAR (BEFORE APPLICATION) WITHOUT DETRIMENT TO ADHESION OR CONSTRUCTION, IF STORED IN PROPER ENVIRONMENT: 10°C-25°C, 40%-60% RH, NO SUN EXPOSURE.

7. QUALITY REQUIREMENTS:
   IMAGE FLOAT - 0.75MM IN ANY DIMENSION (X OR Y)
   LABEL ALIGNMENT - DEFINED IN APPLICABLE HEATSINK DRAWING
   LABEL PEELING - LESS THAN OR EQUAL TO 0.03MM ALONG DEPTH AND WIDTH, AND LESS THAN OR EQUAL TO 1.27MM ALONG THE LENGTH.

<table>
<thead>
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<th>DESCRIPTION</th>
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<th>APPLICABLE</th>
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<tbody>
<tr>
<td>A</td>
<td>TOOLING RELEASE</td>
<td>10/24/16</td>
<td></td>
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</tbody>
</table>

UNLESS OTHERWISE SPECIFIED:

- REFERENCE DOCUMENTS
  - ASME Y14.5M-2009 - STANDARD DIMENSION AND TOLERANCES
  - UL1439 - UL SHARP EDGE TESTING

- FEATURES NOT SPECIFIED ON DRAWING SHALL BE CONTROLLED BY 3D CAD DATABASE.

- LABEL MATERIAL: PET, APPROXIMATELY 0.15MM THICK, WHITE.

- LABEL CONTENT: BLACK

- ADHESIVE: PERMANENT ACRYLIC ADHESIVE, 20 ±1 GM2

- RELIABILITY REQUIREMENTS:
  PRINT RESISTIVITY: MUST SUPPORT THERMAL TRANSFER PRINT DURABILITY/RESISTIVITY AGAINST CHEMICAL DEGRADATION - ALL TESTING IN ACCORDANCE WITH MIL-STD-883/2015.13 DURABILITY MUST DEMONSTRATE DURABILITY IN PRESENCE OF ENVIRONMENTAL CONDITIONS: HUMIDITY 93% RH/48H(7 DAYS), TEMP CYCLE (-70°C TO 50°C FOR 7 DAYS) SHELF LIFE 1 YEAR (BEFORE APPLICATION) WITHOUT DETRIMENT TO ADHESION OR CONSTRUCTION, IF STORED IN PROPER ENVIRONMENT: 10°C-25°C, 40%-60% RH, NO SUN EXPOSURE.

- QUALITY REQUIREMENTS:
  IMAGE FLOAT - 0.75MM IN ANY DIMENSION (X OR Y)
  LABEL ALIGNMENT - DEFINED IN APPLICABLE HEATSINK DRAWING
  LABEL PEELING - LESS THAN OR EQUAL TO 0.03MM ALONG DEPTH AND WIDTH, AND LESS THAN OR EQUAL TO 1.27MM ALONG THE LENGTH.
F  Mechanical Keep-Out Zones (KOZs) Drawings

F.1  Main Board Mechanical KOZs

Processor Heatsink Module (PHM) keep-out zones are included in this chapter. Table F-1 lists the mechanical drawings included in this chapter.

Table F-1.  Mechanical Keep-Out Zone Drawing List

<table>
<thead>
<tr>
<th>Description</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>KOZ: PHM 6 Holes</td>
<td>Figure F-1</td>
</tr>
<tr>
<td>KOZ: PHM Narrow Backplate</td>
<td>Figure F-2</td>
</tr>
<tr>
<td>KOZ: PHM Narrow Master (Sheet 1 of 6)</td>
<td>Figure F-3</td>
</tr>
<tr>
<td>KOZ: PHM 7 Holes</td>
<td>Figure F-9</td>
</tr>
</tbody>
</table>
Figure F-1. KOZ: PHM 6 Holes

NOTES:
1. THIS DRAWING TO BE USED IN CORRELATION WITH SUPPLIED 3D DATABASE FILE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED FILE.
2. CENTERLINE OF SOCKET MUST BE PLACED SYMMETRIC TO THE PHM HOLE PATTERN FOR PROPER FUNCTION.
3. WEIGHT RESTRICTION ZONE IS DEFINED AS ONE WHERE ALL COMPONENTS PLACED ON THE SURFACE OF THE MOTHERBOARD MUST HAVE A MAXIMUM WEIGHT NO GREATER THAN THE WEIGHT DEFINED BY THE ZONE.
4. WEIGHT RESTRICTION OF 0.0 MM REPRESENTS THE TOP (OR BOTTOM) SURFACE OF THE MOTHERBOARD AS THE MAXIMUM HEIGHT. THIS IS A NO COMPONENT PLACEMENT ZONE INCLUDING SOLDER BUMPS.

SCALE  1:15

6X TOP SIDE HOLE DETAIL  A
SCALE  1:15

JOHN S. MILLER
CUSTOMER SERVICE MANAGER  INTEL CORPORATION
2200 MISSION COLLEGE BLVD.
P.O. BOX 58119
SANTA CLARA, CA 95052-8119

KOZ LEGEND

ROUTE ZONE, THROUGH ALL LAYERS
ROUTE ZONE, TOP LAYER

PARTS LIST
DESCRIPTION
LGA-3647 KOZ, PHM 6 HOLE

NOTE: UNLESS OTHERWISE SPECIFIED INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH ASME Y14.5M-1994 DIMENSIONS ARE IN INCHES [MM] THIRD ANGLE PROJECTION

REV. DATE DESCRIPTION
A PRELIMINARY RELEASE 7/25/13
D5 B UPDATED SOCKET OUTLINE NOTE 10/2/13
D5 C UPDATED SOCKET OUTLINE NOTE AND FILE NAME 2/7/14
B6 D MODIFIED HOLE PATTERN TO MAKE ASYMETRIC FOR BOLSTER ORIENTATION 8/22/14
B4 E TOP LAYER RKO REDUCED TO 0.200" FROM 0.276" 11/13/14

NOTES:
1. THIS DRAWING TO BE USED IN CORRELATION WITH SUPPLIED 3D DATABASE FILE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED FILE.
2. CENTERLINE OF SOCKET MUST BE PLACED SYMMETRIC TO THE PHM HOLE PATTERN FOR PROPER FUNCTION.
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Mechanical Keep-Out Zones (KOZs) Drawings

Figure F-2. KOZ: PHM Narrow Backplate

SECONDARY SIDE OF MOTHERBOARD
AS VIEWED FROM THE SECONDARY SIDE

NOTES:
1. THIS DRAWING TO BE USED IN CORRELATION WITH SUPPLIED 3D DATABASE FILE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED FILE.
2. CENTERLINE OF SOCKET MUST BE PLACED SYMMETRIC TO THE PHM HOLE PATTERN FOR PROPER FUNCTION OF SOCKET.
3. A HEIGHT RESTRICTION ZONE IS DEFINED AS ONE WHERE ALL COMPONENTS PLACED ON THE SURFACE OF THE MOTHERBOARD MUST HAVE A MAXIMUM HEIGHT NO GREATER THAN THE HEIGHT DEFINED BY THAT ZONE AFTER REFLOW.
4. UNLESS OTHERWISE NOTED ALL VIEW DIMENSIONS ARE NOMINAL. ALL HEIGHT RESTRICTIONS ARE MAXIMUMS. ZONES ARE NOT DRIVEN BY SPECIFIC OR IMPLIED TOLERANCES.
5. A HEIGHT RESTRICTION OF 0.0 MM REPRESENTS THE TOP (OR BOTTOM) SURFACE OF THE MOTHERBOARD AS THE MAXIMUM HEIGHT. THIS IS A NO COMPONENT PLACEMENT ZONE INCLUDING SOLDER BUMPS.

SECONDARY SIDE OF MOTHERBOARD
AS VIEWED FROM THE SECONDARY SIDE

SCALE 5:1

DETAIL A

SEEM DETAIL A

SEE DETAIL A

NOTES:
1. THIS DRAWING TO BE USED IN CORRELATION WITH SUPPLIED 3D DATABASE FILE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED FILE.
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SECONDARY SIDE OF MOTHERBOARD
AS VIEWED FROM THE SECONDARY SIDE

SCALE 5:1

DETAIL A

SEEM DETAIL A

SEE DETAIL A

NOTES:
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SECONDARY SIDE OF MOTHERBOARD
AS VIEWED FROM THE SECONDARY SIDE

SCALE 5:1

DETAIL A

SEEM DETAIL A

SEE DETAIL A

NOTES:
1. THIS DRAWING TO BE USED IN CORRELATION WITH SUPPLIED 3D DATABASE FILE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED FILE.
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SECONDARY SIDE OF MOTHERBOARD
AS VIEWED FROM THE SECONDARY SIDE

SCALE 5:1

DETAIL A

SEEM DETAIL A

SEE DETAIL A

NOTES:
1. THIS DRAWING TO BE USED IN CORRELATION WITH SUPPLIED 3D DATABASE FILE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED FILE.
2. CENTERLINE OF SOCKET MUST BE PLACED SYMMETRIC TO THE PHM HOLE PATTERN FOR PROPER FUNCTION OF SOCKET.
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4. UNLESS OTHERWISE NOTED ALL VIEW DIMENSIONS ARE NOMINAL. ALL HEIGHT RESTRICTIONS ARE MAXIMUMS. ZONES ARE NOT DRIVEN BY SPECIFIC OR IMPLIED TOLERANCES.
5. A HEIGHT RESTRICTION OF 0.0 MM REPRESENTS THE TOP (OR BOTTOM) SURFACE OF THE MOTHERBOARD AS THE MAXIMUM HEIGHT. THIS IS A NO COMPONENT PLACEMENT ZONE INCLUDING SOLDER BUMPS.
Figure F-3. KOZ: PHM Narrow Master (Sheet 1 of 6)

This drawing contains all PHM narrow top KOZs.

SKX HFI PHM KOZ
-KOZ_H18200_SKG-PHM-NRW
-TO BE USED WITH BOLSTER ASSEMBLY H77929

SKX HFI PHM KOZ
-KOZ_H18200_SKG-PHM-NRW-HFI
-TO BE USED WITH ONE OF THE SKX LEC BELOW
-SEE SHEETS 4-6
-TO BE USED WITH BOLSTER ASSEMBLY H78902 OR H77929

SKX LEC LEFT EGRESS KOZ
-KOZ_H18200_SKG-LEC-LEFT
-TO BE USED WITH KOZ_H18200_SKG-PHM-TOP-HFI
-SEE SHEET 4

SKX LEC STRAIGHT EGRESS KOZ
-KOZ_H18200_SKG-LEC-STRAIGHT
-TO BE USED WITH KOZ_H18200_SKG-PHM-TOP-HFI
-SEE SHEET 5

SKX LEC RIGHT EGRESS KOZ
-KOZ_H18200_SKG-LEC-RIGHT
-TO BE USED WITH KOZ_H18200_SKG-PHM-TOP-HFI
-SEE SHEET 6

NOTES:
1. THIS DRAWING IS TO BE USED IN CONJUNCTION WITH THE SUPPLIED 3D DATABASE FILE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED FILE.
2. UNLESS OTHERWISE NOTED ALL VIEW DIMENSIONS ARE NOMINAL. ALL HEIGHT RESTRICTIONS ARE MAXIMUMS. ZONES ARE NOT DRIVEN BY SPECIFIC OR IMPLIED TOLERANCES.
3. ALL WEIGHT RESTRICTIONS ARE MAXIMUM. ZONES ARE NOT DRIVEN BY SPECIFIC OR IMPLIED TOLERANCES.
4. ASSUMING A GENERIC MAXIMUM COMPONENT HEIGHT ZONE.

Component Placement in this Zone must include:

- Component Tolerances
- Component Weight

DO NOT PLACE COMPONENTS IN THIS ZONE THAT WILL EXCEED THE SPECIFIED MAXIMUM HEIGHT.
Figure F-4. KOZ: PHM Narrow Master (Sheet 2 of 6)
Figure F-5. KOZ: PHM Narrow Master (Sheet 3 of 6)
Figure F-6. KOZ: PHM Narrow Master (Sheet 4 of 6)

KOZ NAME: KOZ_H18200_SKX-LEC-LEFT

KOZ MUST CONTINUE, AND ALLOW CABLE ROUTING FOR SPECIFIC CHASSIS LAYOUT

CABLE OVERMOLD PLUS TRAVEL DURING INSTALLATION / REMOVAL

PIN-1 LOCATION FOR REFERENCE ONLY

TX MOTHERBOARD THROUGH HOLES FOR REFERENCE ONLY FOR DETAILS SEE DOCUMENT KOZ_H18201_SKX-PHM-7-HOLE

FOR REFERENCE ONLY, FOR DETAILS SEE DOCUMENT KOZ_H18200_SKX-PHM-7-HOLE

KOZ LEGEND

HFI CONNECTOR AND CABLE ROUTING ZONE
0.0 MM HEIGHT RESTRICTION
LEC STRAIGHT EGRESS KOZ
KOZ NAME: KOZ_H18200_SKX-LEC-STRAIGHT
KOZ MUST CONTINUE, AND ALLOW CABLE ROUTING FOR SPECIFIC CHASSIS LAYOUT

TX MOTHERBOARD THROUGH HOLES FOR REFERENCE ONLY. FOR DETAILS SEE DOCUMENT KOZ_H18201_SKX-PHM-7-HOLE

PIN-1 LOCATION FOR REFERENCE ONLY

HFI CONNECTOR AND CABLE ROUTING ZONE
0.0 MM HEIGHT RESTRICTION
CABLE EGRESS ZONE, 1 MM HEIGHT RESTRICTION
**KOZ LEGEND**

- HFI CONNECTOR AND CABLE ROUTING ZONE
- 0.0 MM HEIGHT RESTRICTION

**KOZ MUST CONTINUE, AND ALLOW CABLE ROUTING FOR SPECIFIC CHASSIS LAYOUT**

**CABLE PLUS TRAVEL DURING INSTALLATION / REMOVAL**

**PIN 1 LOCATION FOR REFERENCE ONLY**

**MOTHERBOARD THROUGH HOLES FOR REFERENCE ONLY**

**REFERENCE**

**KOZ NAME: KOZ_H18200_SKX-LEC-RIGHT**

**90° LEČ RIGHT EGRESS KOZ**

**KOZ_H18200_SKX-PHM-NRW-MASTER 6F**

**Dwg. No Sht. Rev**

**Sheet 6 of 6**

**DO NOT SCALE DRAWING**

**SCALE: 3:1**

**Figure F-8. KOZ: PHM Narrow Master (Sheet 6 of 6)**
Second Generation Intel® Xeon® Scalable Processors
Thermal/Mechanical Specifications and Design Guide, August 2019

**Mechanical Keep-Out Zones (KOZs) Drawings**

### Figure F-9. KOZ: PHM 7 Holes

#### Notes:
1. This drawing is to be used in correlation with supplied 3D database files. All dimensions and tolerances on this drawing take precedence over supplied file.
2. Centerline of socket must be placed symmetric to the PHM hole pattern for proper function.
3. Height restriction zone is defined as one where all components placed on the surface of the mother board must have a maximum height no greater than the height defined by that zone after reflow.
4. Height restriction of 0.0 mm represents the top (or bottom) surface of the motherboard as the maximum height. This is a no component placement zone including solder bumps.

#### Parts List

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<th>Description</th>
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#### Revision History

- A PRELIMINARY RELEASE 7/25/13
- UPDATED SOCKET OUTLINE NOTE 10/2/13
- UPDATED SOCKET REFERENCE NOTE AND FILE NAME 2/7/14
- TOP LAYER RKO REDUCED TO 0.200" FROM 0.276" 11/13/14

#### Interpreting Dimensions and Tolerances

Dimensions are in inches [mm]. Third angle projection.
G  Board Flexure Initiative

Figure G-1. LGA3647 Socket BFI (Sheet 1 of 2)

| Scope | The strain values provided in this document apply only to transient bend conditions seen in board manufacturing assembly environment with no PHM and does not apply once PHM is installed. |
|-------|
| Gage Location | Strain gages must be placed at 4 locations on the board at 12.0 mm from corner solder joint, measured along the diagonal, with e1 and e3 parallel to the edges. Alternatively, the gage can be located with reference to socket housing. Please refer to figures 2 through 5 for locating strain gage on all four corners. Accurate positioning of the strain gages is necessary to compare strain data to Intel's BFI strain guidance. Strain gage location accuracy should be +/-0.5 mm and +/-5°. |

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<td>Pin Count</td>
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Figure 1 Gage placement at all four corners
**Test Requirements:** The Maximum Diagonal Strain for all (4) corners, is not to exceed the values listed in the table. The Diagonal Strain formula is defined as:

Max Diagonal Strain = \( \text{MAX} (|e_2|, |e_1+e_3-e_2|) \)

Where \( e_1, e_2, \) & \( e_3 \) are the raw strain readings from the three gages in the rosette, and the numbers inside the vertical bars are absolute values.

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<tr>
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<td>10 mm</td>
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**Reference Documents**
- Intel Board Flexure MAS rev 5.0 (or later) “Manufacturing with Intel Components: Strain measurement for Circuit Board Assembly”
- Module 1 Overview
- Module 2 Test Board Preparation
- Module 3 Assembly line measurement procedure
- Module 4 Reporting Procedure
- Module 5 Reducing Board Flexure in ICT
- Module 6 Troubleshooting

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May 2015