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# GALILEO GEN2

## INTEL QUARK X1000

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### FAB H

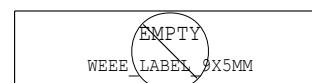
PB: H48142-207

PBA: H48125-800

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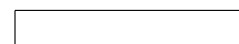
LB1



WEEE

LB6V1

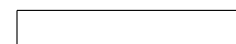
LABEL



1500X500\_TARGET  
SERIAL NUMBER

LB3

LABEL



1375X250\_TARGET  
MAC ADDRESS LABEL

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Wed May 21 10:12:25 2014

<b>INTEL CORPORATION</b> 2111 NE 25TH AVENUE HILLSBORO OR 97124		
TITLE	GALILEO Gen2	DOCUMENT NUMBER
	DESIGN TITLE PAGE	H38681
		REV
		2.0
SHEET 1 OF 28		

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6

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# TABLE OF CONTENTS

SHEET NUMBER	SHEET NAME	SHEET NUMBER	SHEET NAME
1	DESIGN TITLE PAGE		
2	TABLE OF CONTENTS		
3	DISCLAIMER		
4	SYSTEM BLOCK DIAGRAM		
5	QUARK DDR3 & PCIE		
6	QUARK GPIO		
7	QUARK MISC		
8	QUARK POWER		
9	QUARK DECOUPLING		
10	SDRAM 1		
11	SDRAM 2		
12	SDRAM TERMINATION		
13	MINI PCIE CONNECTOR		
14	MICRO SD CONNECTOR		
15	USB CONNECTORS		
16	UART 1 & JTAG		
17	LAN		
18	SPI: ADC&FLASH		
19	QUARK STRAPS		
20	EXTERNAL IO MUXING 1		
21	EXTERNAL IO MUXING 2		
22	LVL B BUFFER		
23	LVL C BUFFER		
24	AMUX & EXTERNAL IO		
25	VOLTAGE REGULATORS		
26	VOLTAGE REGULATORS		
27	VOLTAGE REGULATORS		
28	POWER BUTTONS & MISC		

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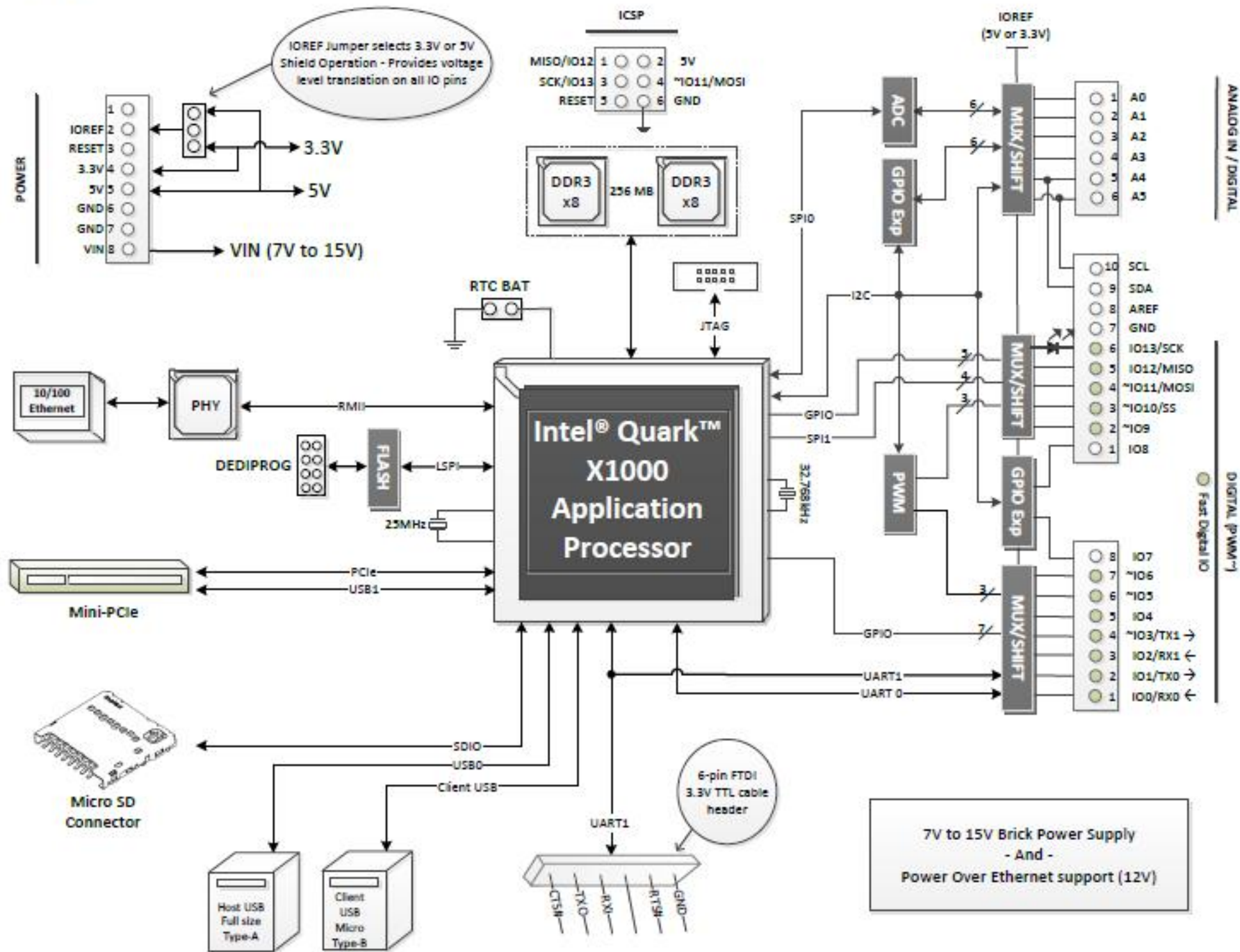
## Intel® Galileo Design Document

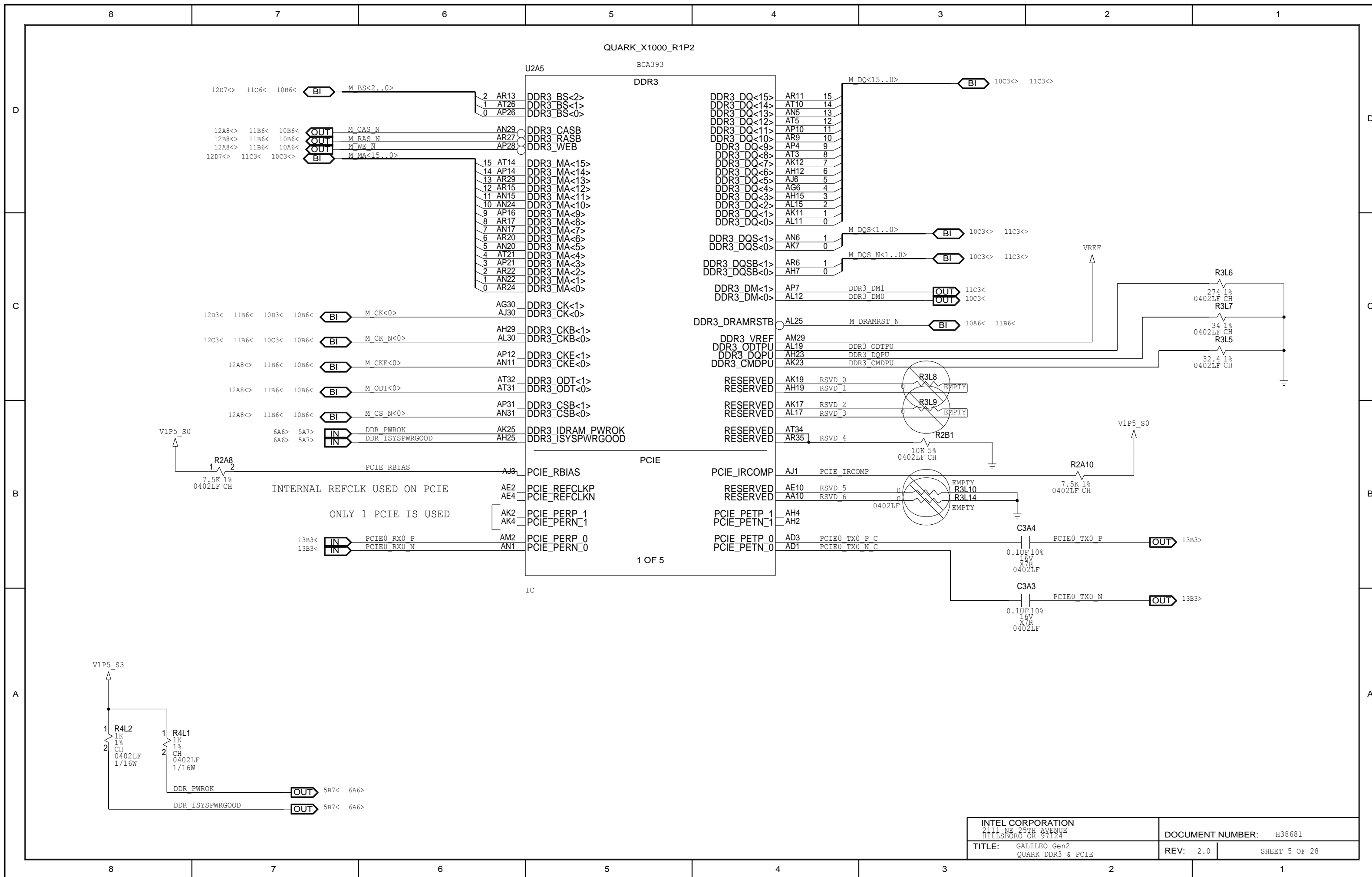
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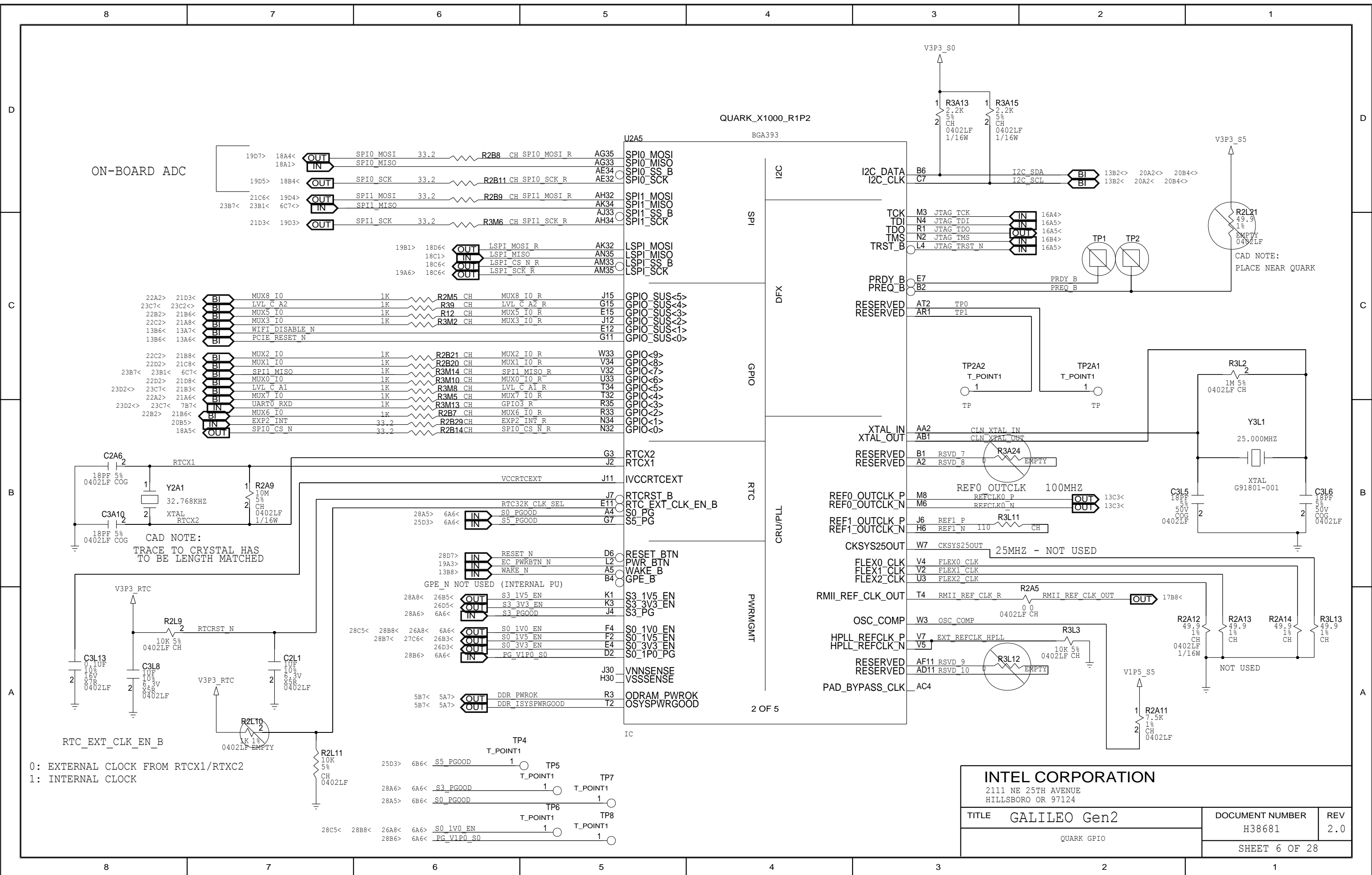
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INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 DISCLAIMER		REV: 2.0	SHEET 3 OF 28

Intel® Galileo™ Board Fab H (PVT)  
May/2014







ON-BOARD ADC

19D7>	18A4<	OUT	SPI0_MOSI	33.2	R2B8	CH	SPI0_MOSI_R	AG35	SPI0_MOSI
	18A1>	IN	SPI0_MISO					AG33	SPI0_MISO
19D5>	18B4<	OUT	SPI0_SCK	33.2	R2B11	CH	SPI0_SCK_R	AE34	SPI0_SCK
	23B1<	IN	SPI1_MISO					AE32	SPI0_SCK
21C6<	19D4>	OUT	SPI1_MOSI	33.2	R2B9	CH	SPI1_MOSI_R	AH32	SPI1_MOSI
23B7<	6C7<	IN	SPI1_MISO					AH34	SPI1_MISO
21D3<	19D3>	OUT	SPI1_SCK	33.2	R3M6	CH	SPI1_SCK_R	AJ33	SPI1_SCK
		IN						AH34	SPI1_SCK

19B1>	18D6<	OUT	LSPI_MOSI_R					AK32	LSPI_MOSI
	18C1>	IN	LSPI_MISO					AN35	LSPI_MISO
	18C6<	OUT	LSPI_CS_N_R					AM33	LSPI_CS_N
19A6>	18C6<	OUT	LSPI_SCK_R					AM35	LSPI_SCK

22A2>	21D3<	BI	MUX8_I0	1K	R2M5	CH	MUX8_I0_R	J15	GPIO_SUS<5>
23C7<	23C2<	BI	LVL_C_A2	1K	R39	CH	LVL_C_A2_R	G15	GPIO_SUS<4>
22B2>	21B6<	BI	MUX5_I0	1K	R12	CH	MUX5_I0_R	E15	GPIO_SUS<3>
22C2>	21A8<	BI	MUX3_I0	1K	R3M2	CH	MUX3_I0_R	J12	GPIO_SUS<2>
13B6<	13A7<	BI	WIFI_DISABLE_N					E12	GPIO_SUS<1>
13B6<	13A6<	BI	PCIE_RESET_N					G11	GPIO_SUS<0>

22C2>	21B8<	BI	MUX2_I0	1K	R2B21	CH	MUX2_I0_R	W33	GPIO<9>
22D2>	21C8<	BI	MUX1_I0	1K	R2B20	CH	MUX1_I0_R	V34	GPIO<8>
23B7<	23B1<	BI	SPI1_MISO	1K	R3M14	CH	SPI1_MISO_R	V32	GPIO<7>
22D2>	21D8<	BI	MUX0_I0	1K	R3M10	CH	MUX0_I0_R	U33	GPIO<6>
23D2<	23C7<	BI	LVL_C_A1	1K	R3M8	CH	LVL_C_A1_R	T34	GPIO<5>
22A2>	21A6<	BI	MUX7_I0	1K	R3M5	CH	MUX7_I0_R	T32	GPIO<4>
23D2<	23C7<	BI	UART0_RXD	1K	R3M13	CH	GPIO3_R	R35	GPIO<3>
22B2>	21B6<	BI	MUX6_I0	1K	R2B7	CH	MUX6_I0_R	R33	GPIO<2>
	20B5>	IN	EXP2_INT	33.2	R2B29	CH	EXP2_INT_R	N34	GPIO<1>
	18A5<	OUT	SPI0_CS_N	33.2	R2B14	CH	SPI0_CS_N_R	N32	GPIO<0>

28A5>	6A6<	IN	S0_PGOOD					A4	S0_PG
25D3>	6A6<	IN	S5_PGOOD					G7	S5_PG

28D7>		IN	RESET_N					D6	RESET_BTN
19A3>		IN	EC_PWRBTN_N					L2	PWR_BTN
13B8>		IN	WAKE_N					A5	WAKE_B
		IN	GPE_N NOT USED (INTERNAL PU)					B4	GPE_B

28A8<	26B5<	OUT	S3_1V5_EN					K1	S3_1V5_EN
26D5<	26D5<	OUT	S3_3V3_EN					K3	S3_3V3_EN
28A6>	6A6<	OUT	S3_PGOOD					J4	S3_PG

28C5<	28B8<	OUT	S0_1V0_EN					F4	S0_1V0_EN
	27C6<	OUT	S0_1V5_EN					F2	S0_1V5_EN
	26D3<	OUT	S0_3V3_EN					E4	S0_3V3_EN
28B6>	6A6<	IN	PG_V1P0_S0					D2	S0_1P0_PG

**INTEL CORPORATION**  
 2111 NE 25TH AVENUE  
 HILLSBORO OR 97124

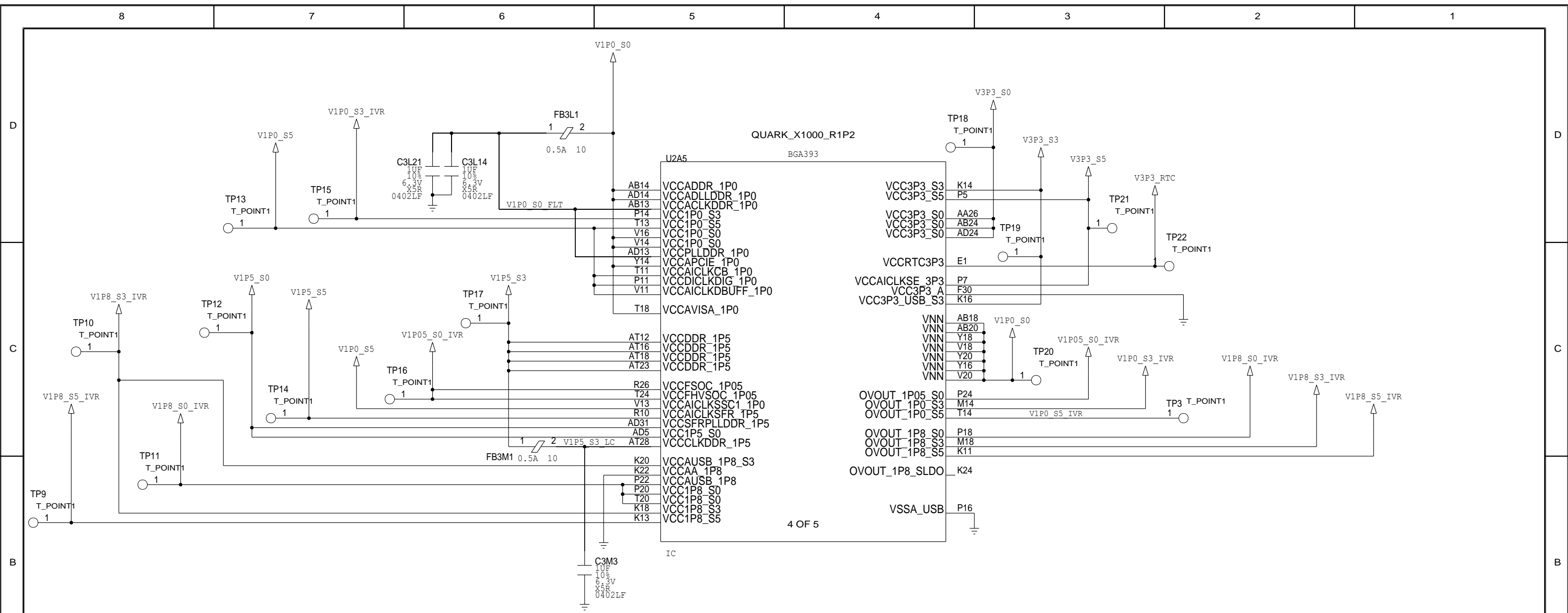
TITLE	GALILEO Gen2	DOCUMENT NUMBER	H38681	REV	2.0
QUARK GPIO			SHEET 6 OF 28		

0: EXTERNAL CLOCK FROM RTCX1/RTXC2  
 1: INTERNAL CLOCK

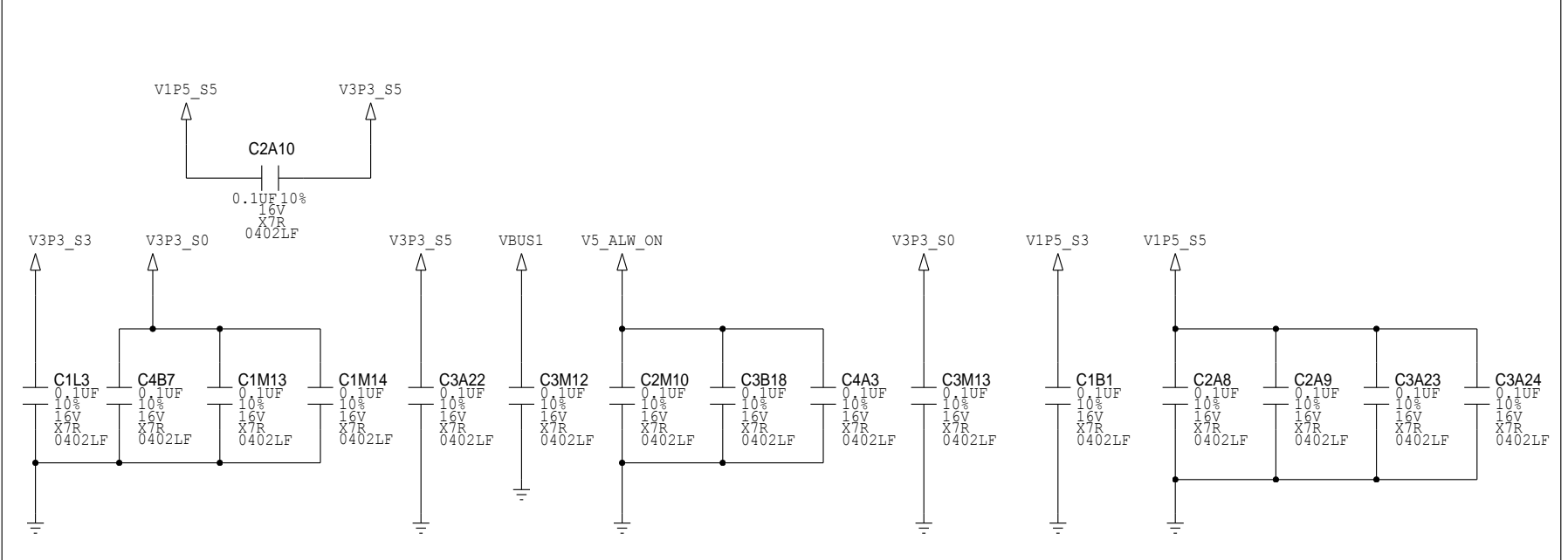
CAD NOTE:  
 TRACE TO CRYSTAL HAS  
 TO BE LENGTH MATCHED

CAD NOTE:  
 PLACE NEAR QUARK



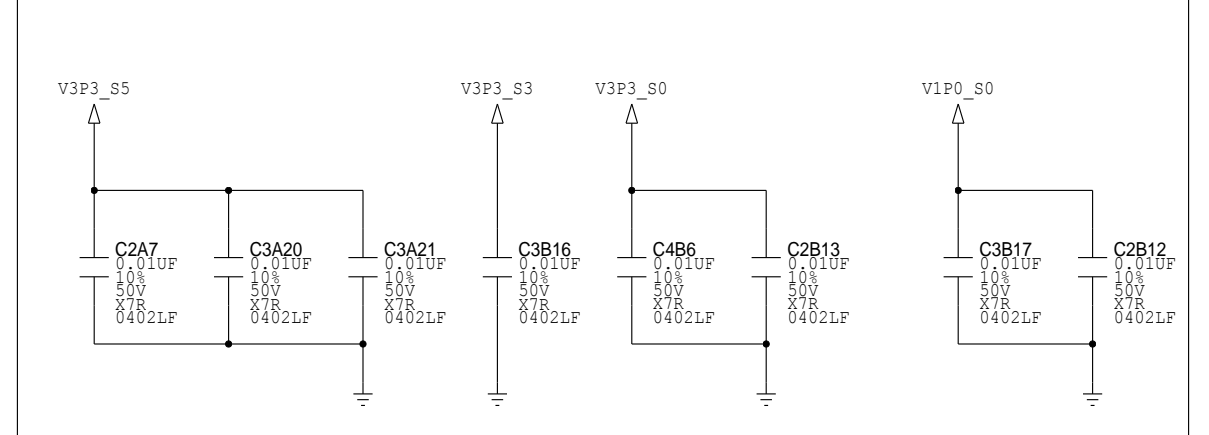


STITCHING CAPS FOR SPLIT PLANES



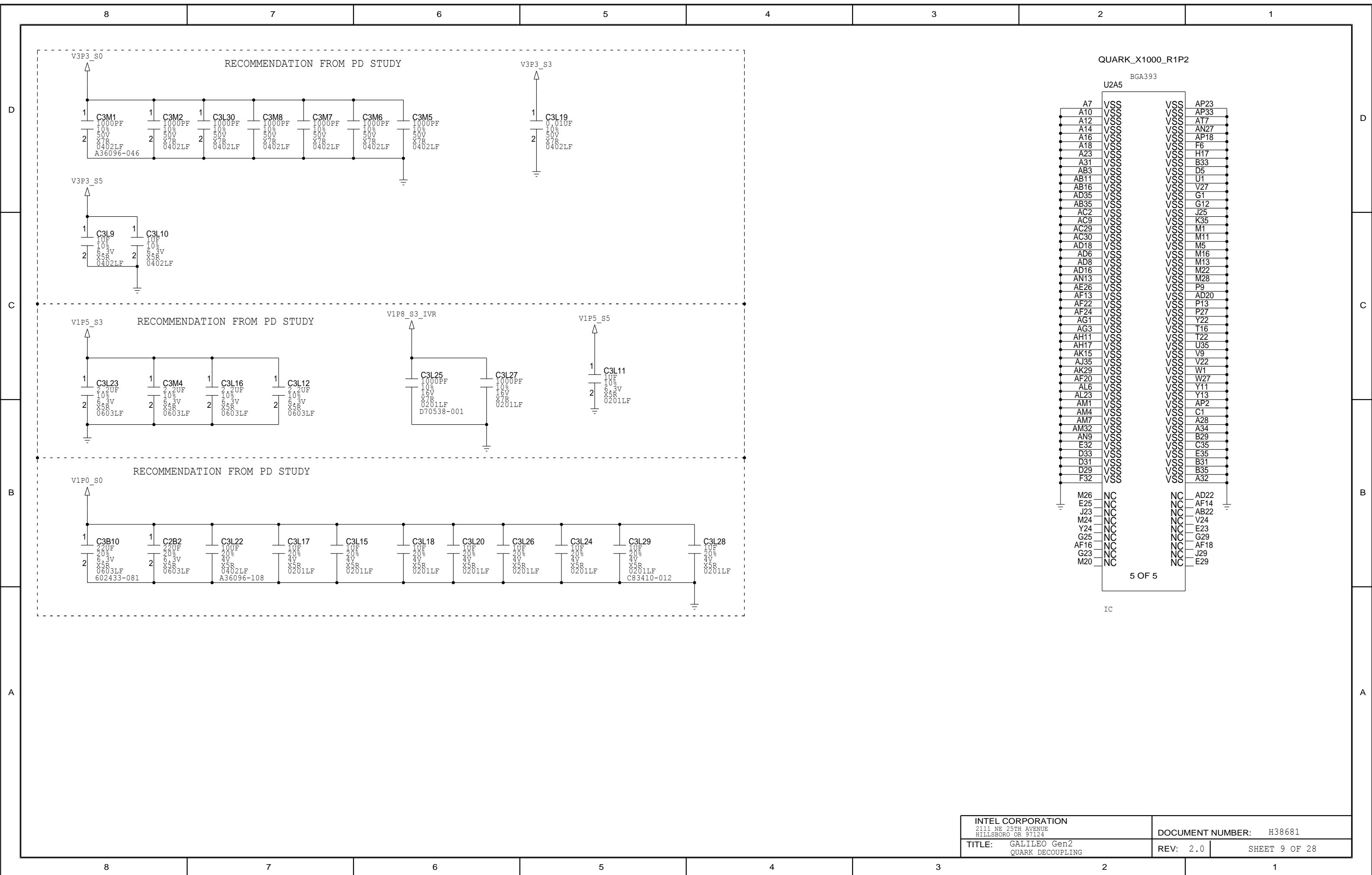
CAD NOTE  
PLACE AS CLOSE AS POSSIBLE TO SIGNAL VIAS

STITCHING CAPS FOR SIGNAL REFERENCE TRANSITION



INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 QUARK POWER		REV: 2.0	SHEET 8 OF 28

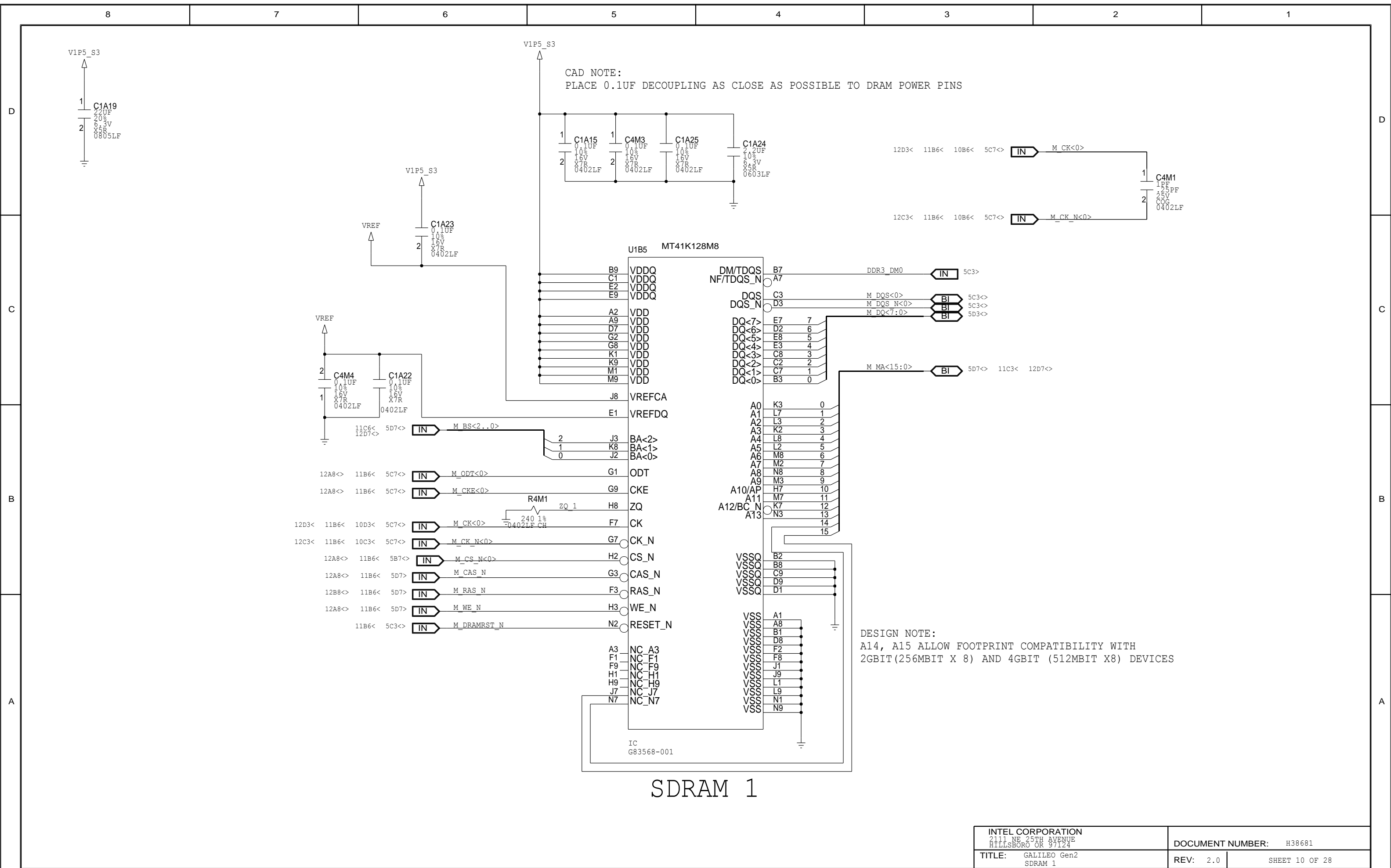




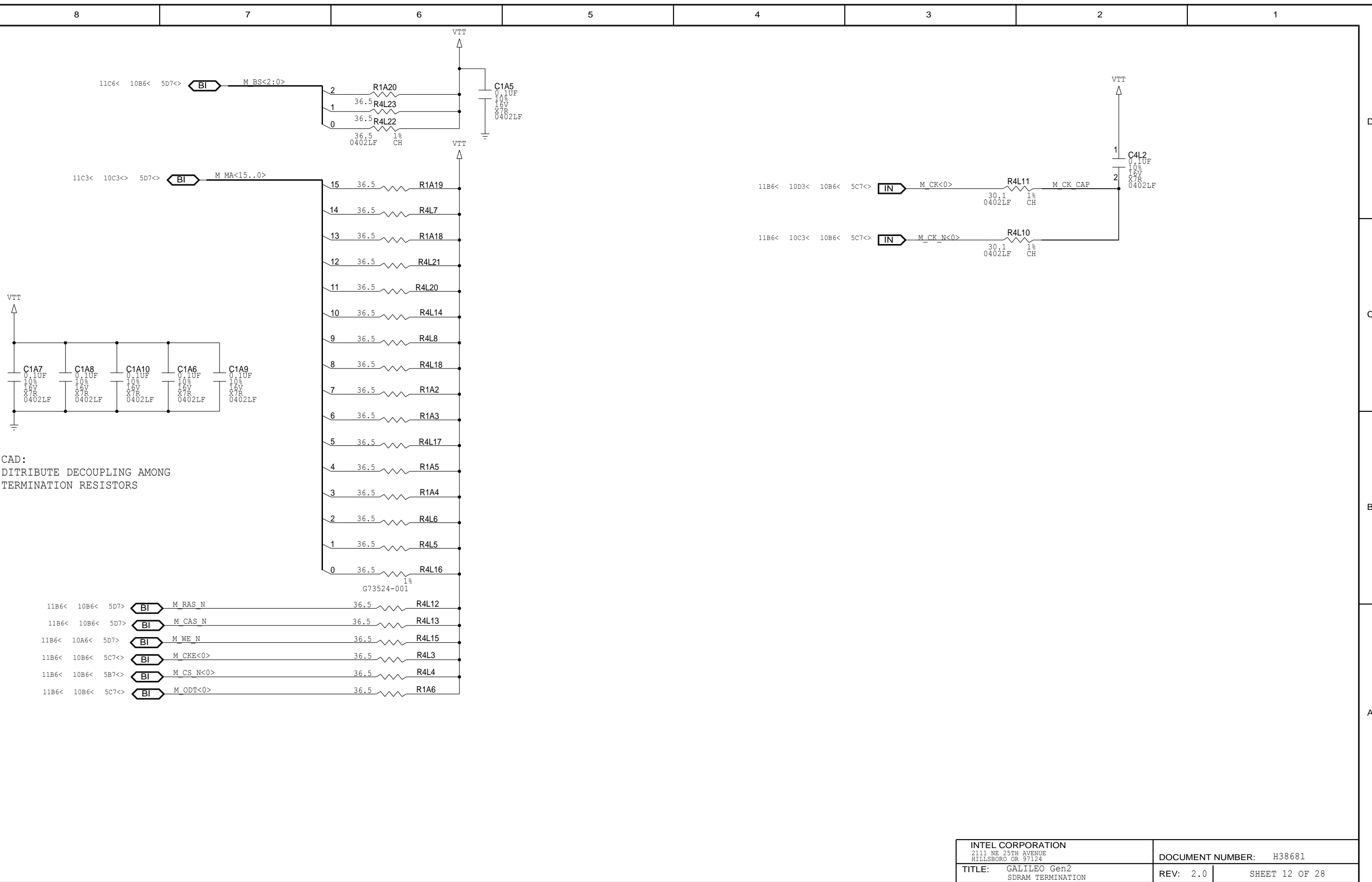
QUARK\_X1000\_R1P2  
BGA393

U2A5	A7	VSS	VSS	AP23
	A10	VSS	VSS	AP33
	A12	VSS	VSS	AT7
	A14	VSS	VSS	AN27
	A16	VSS	VSS	AP18
	A18	VSS	VSS	F6
	A23	VSS	VSS	H17
	A31	VSS	VSS	B33
	AB3	VSS	VSS	D5
	AB11	VSS	VSS	U1
	AB16	VSS	VSS	V27
	AD35	VSS	VSS	G1
	AB35	VSS	VSS	G12
	AC2	VSS	VSS	J25
	AC9	VSS	VSS	K35
	AC29	VSS	VSS	M1
	AC30	VSS	VSS	M11
	AD18	VSS	VSS	M5
	AD6	VSS	VSS	M16
	AD8	VSS	VSS	M13
	AD16	VSS	VSS	M22
	AN13	VSS	VSS	M28
	AE26	VSS	VSS	P9
	AF13	VSS	VSS	AD20
	AF22	VSS	VSS	P13
	AF24	VSS	VSS	P27
	AG1	VSS	VSS	Y22
	AG3	VSS	VSS	T16
	AH11	VSS	VSS	T22
	AH17	VSS	VSS	U35
	AK15	VSS	VSS	V9
	AJ35	VSS	VSS	V22
	AK29	VSS	VSS	W1
	AF20	VSS	VSS	W27
	AL6	VSS	VSS	Y11
	AL23	VSS	VSS	Y13
	AM1	VSS	VSS	AP2
	AM4	VSS	VSS	C1
	AM7	VSS	VSS	A28
	AM32	VSS	VSS	A34
	AN9	VSS	VSS	B29
	E32	VSS	VSS	C35
	D33	VSS	VSS	E35
	D31	VSS	VSS	B31
	D29	VSS	VSS	B35
	F32	VSS	VSS	A32
	M26	NC	NC	AD22
	E25	NC	NC	AF14
	J23	NC	NC	AB22
	M24	NC	NC	V24
	Y24	NC	NC	E23
	G25	NC	NC	G29
	AF16	NC	NC	AF18
	G23	NC	NC	J29
	M20	NC	NC	E29

5 OF 5

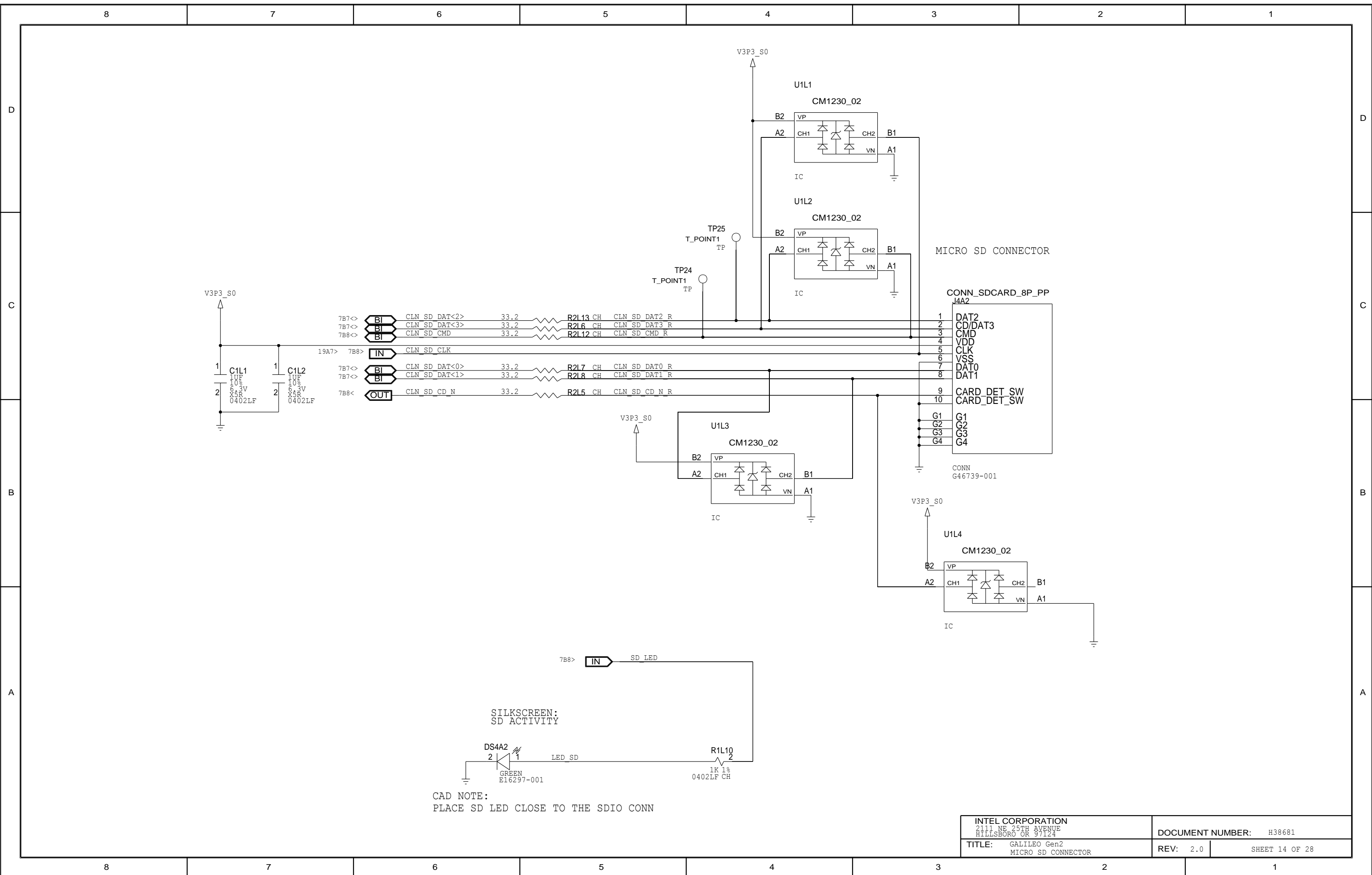






CAD:  
DITRIBUTE DECOUPLING AMONG  
TERMINATION RESISTORS





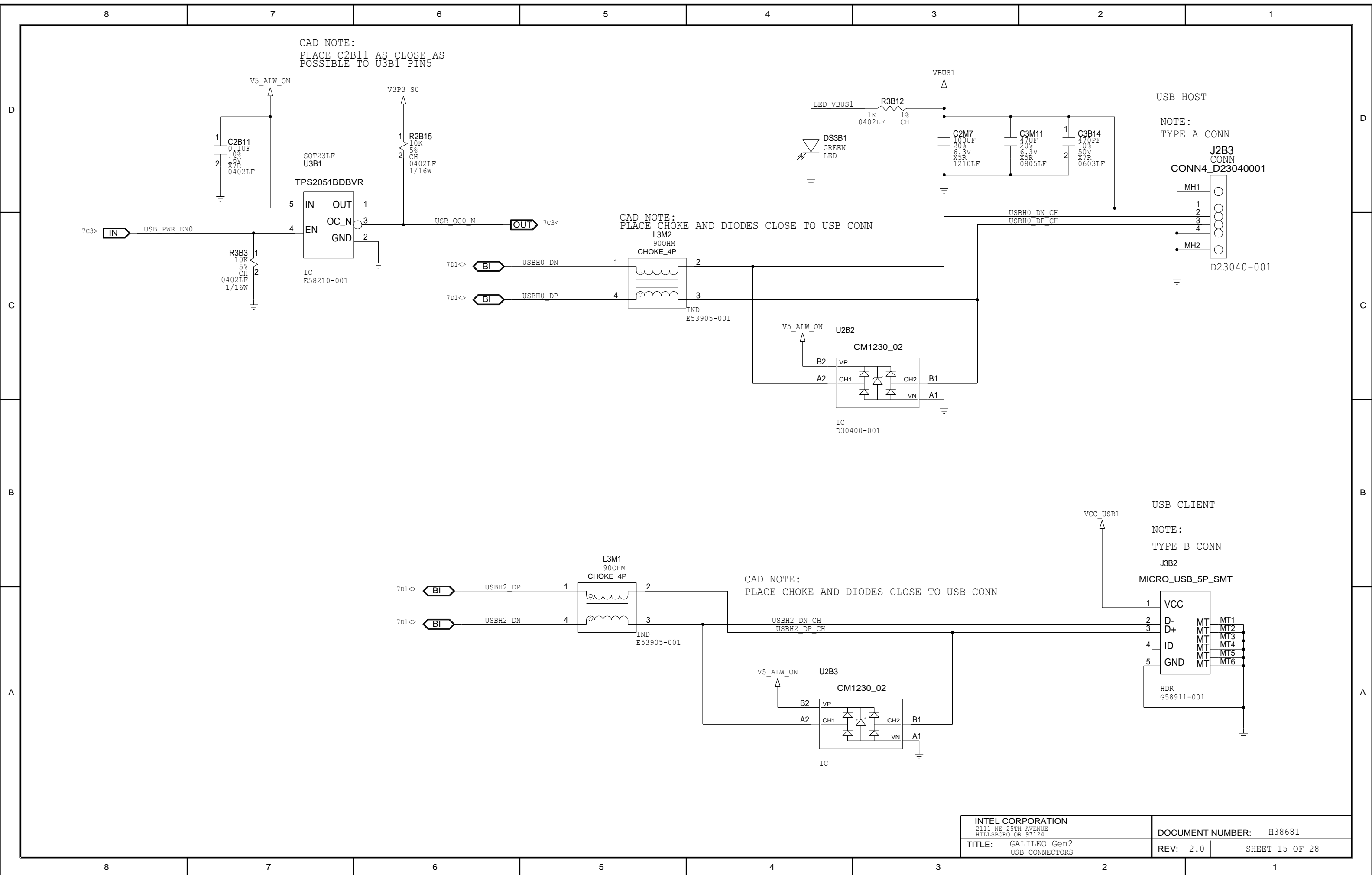
7B7<	BI	CLN_SD_DAT<2>	33.2	R2L13	CH	CLN_SD_DAT2	R
7B7<	BI	CLN_SD_DAT<3>	33.2	R2L6	CH	CLN_SD_DAT3	R
7B8<	BI	CLN_SD_CMD	33.2	R2L12	CH	CLN_SD_CMD	R
19A7>	IN	CLN_SD_CLK					
7B7<	BI	CLN_SD_DAT<0>	33.2	R2L7	CH	CLN_SD_DAT0	R
7B7<	BI	CLN_SD_DAT<1>	33.2	R2L8	CH	CLN_SD_DAT1	R
7B8<	OUT	CLN_SD_CD_N	33.2	R2L5	CH	CLN_SD_CD_N	R

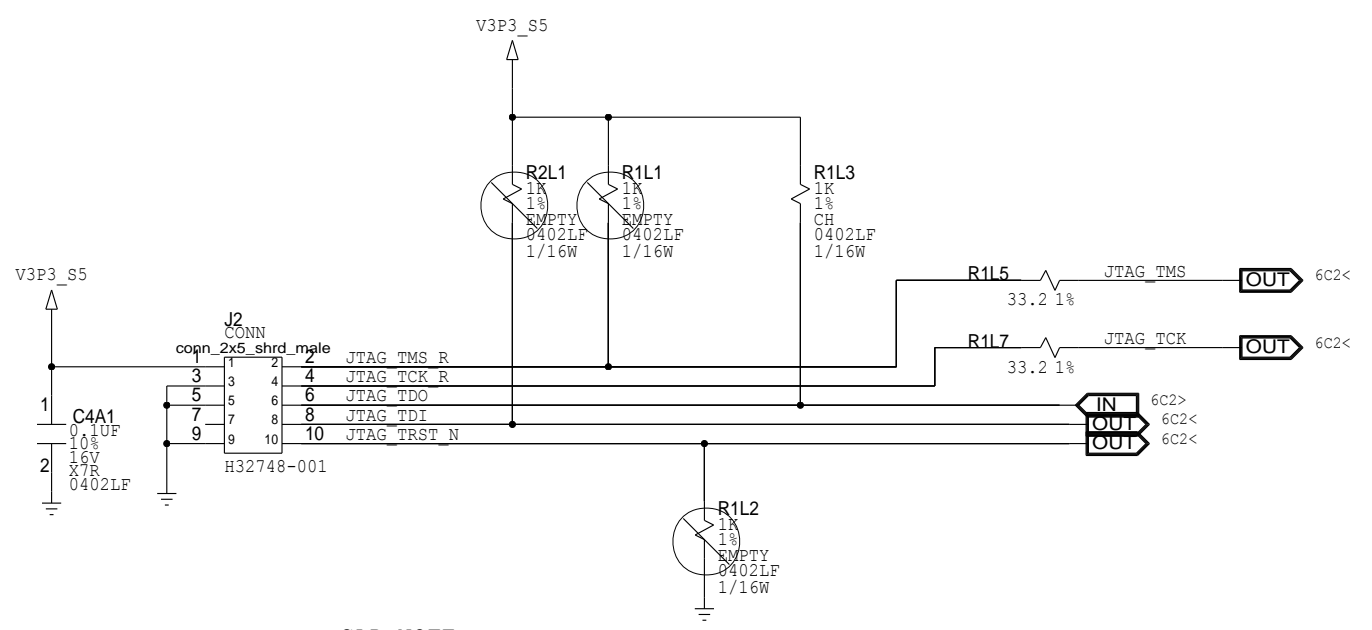
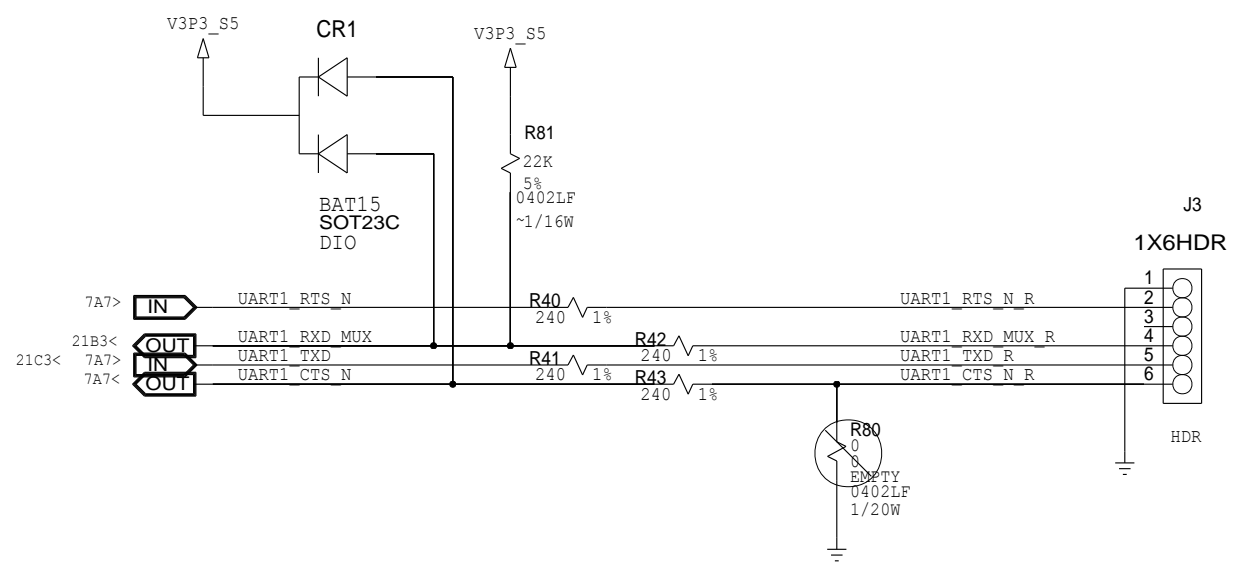
SILKSCREEN:  
SD ACTIVITY



CAD NOTE:  
PLACE SD LED CLOSE TO THE SDIO CONN

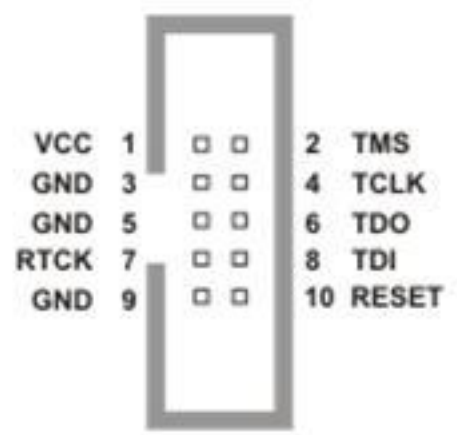
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 MICRO SD CONNECTOR		REV: 2.0	SHEET 14 OF 28





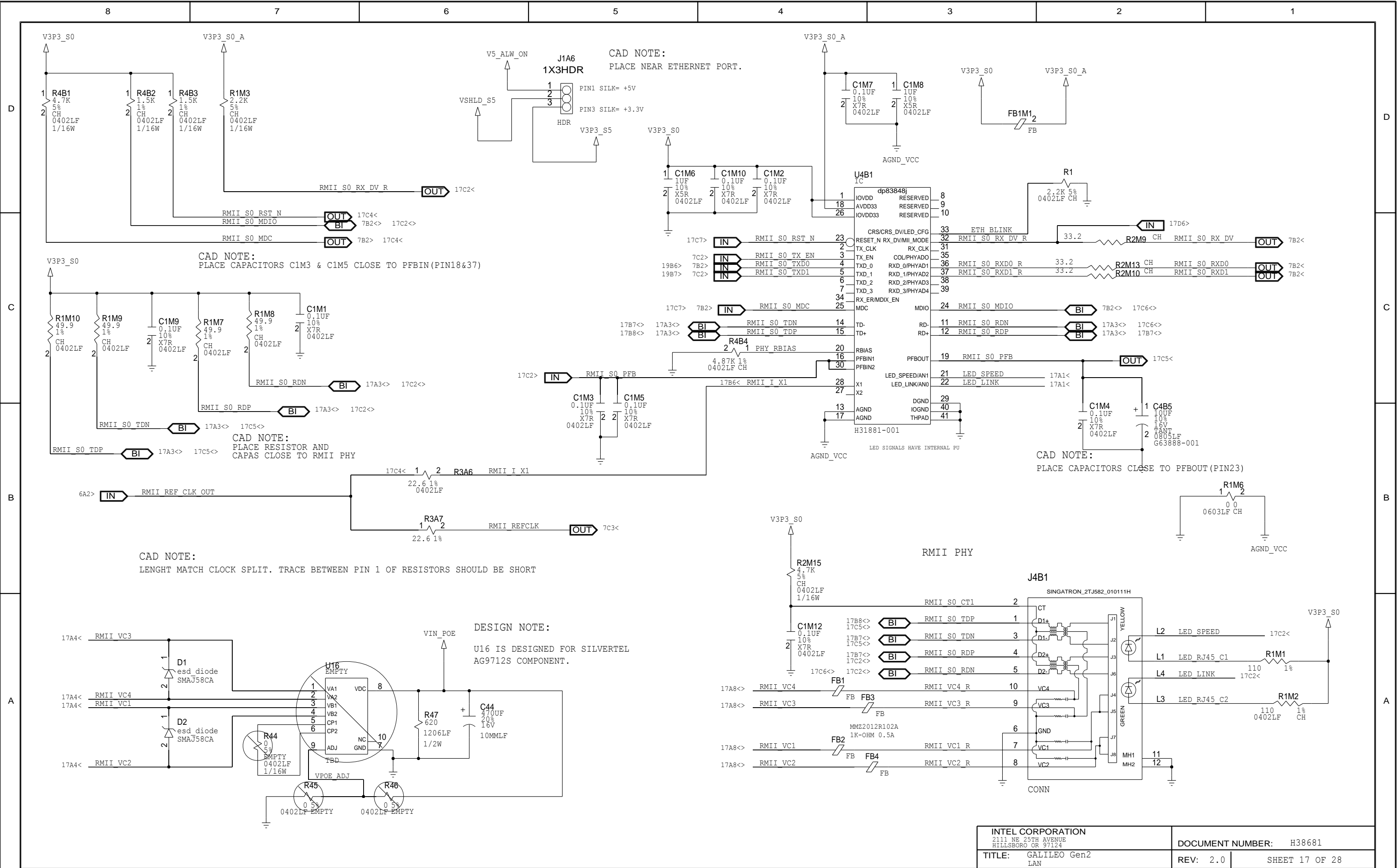
CAD NOTE:  
PLACE CONNECTOR ON SOLDER-SIDE.

### MINI-JTAG CONNECTOR



INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 UART 1 & JTAG		REV: 2.0	SHEET 16 OF 28





CAD NOTE:  
PLACE NEAR ETHERNET PORT.

CAD NOTE:  
PLACE CAPACITORS C1M3 & C1M5 CLOSE TO PFBIN(PIN18&37)

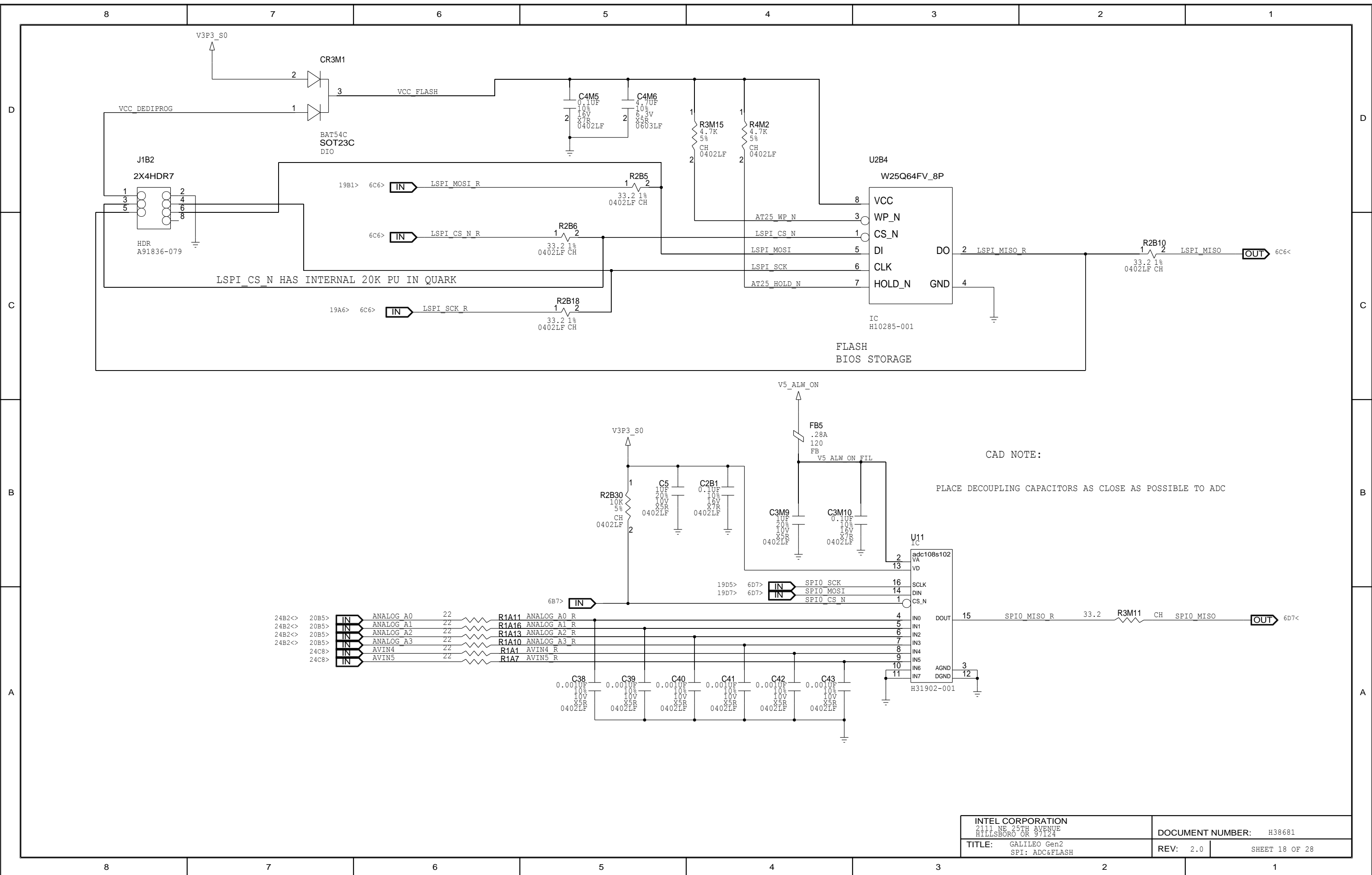
CAD NOTE:  
PLACE RESISTOR AND CAPAS CLOSE TO RMIILAN PHY

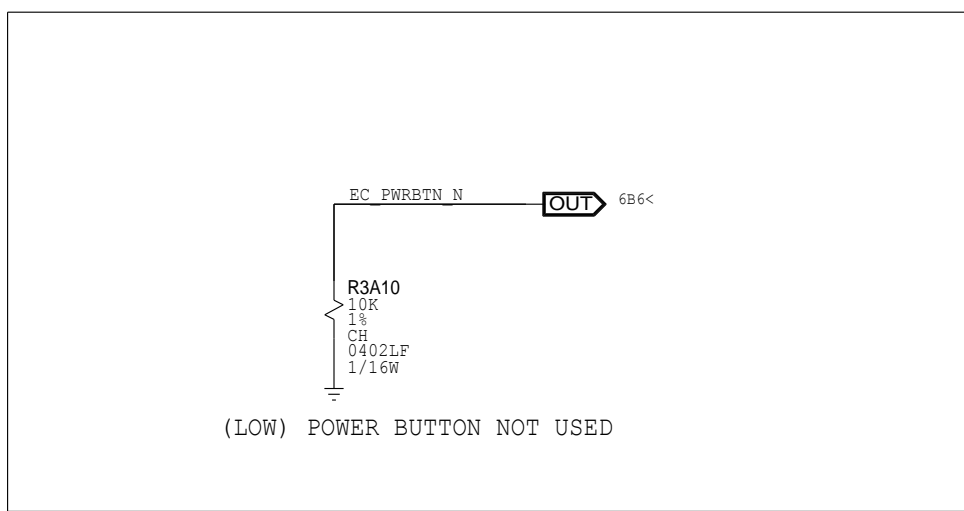
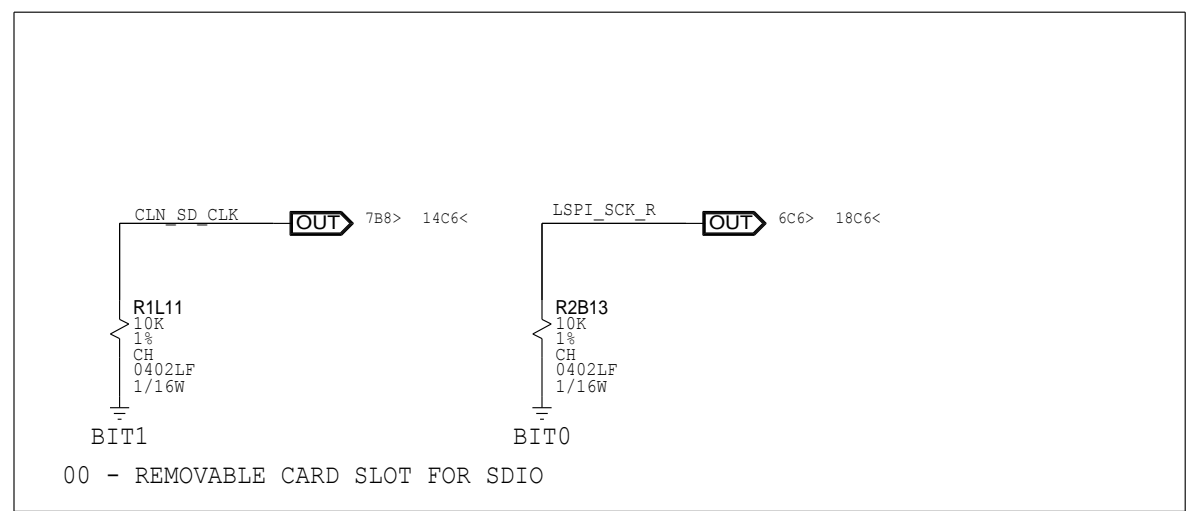
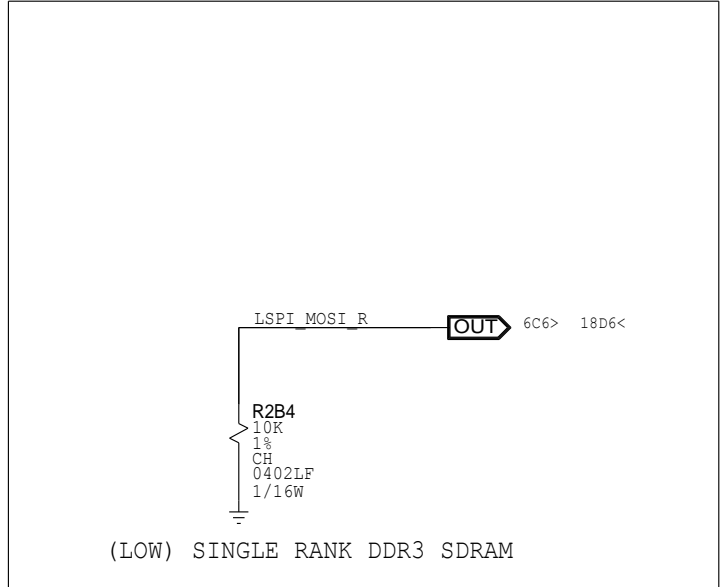
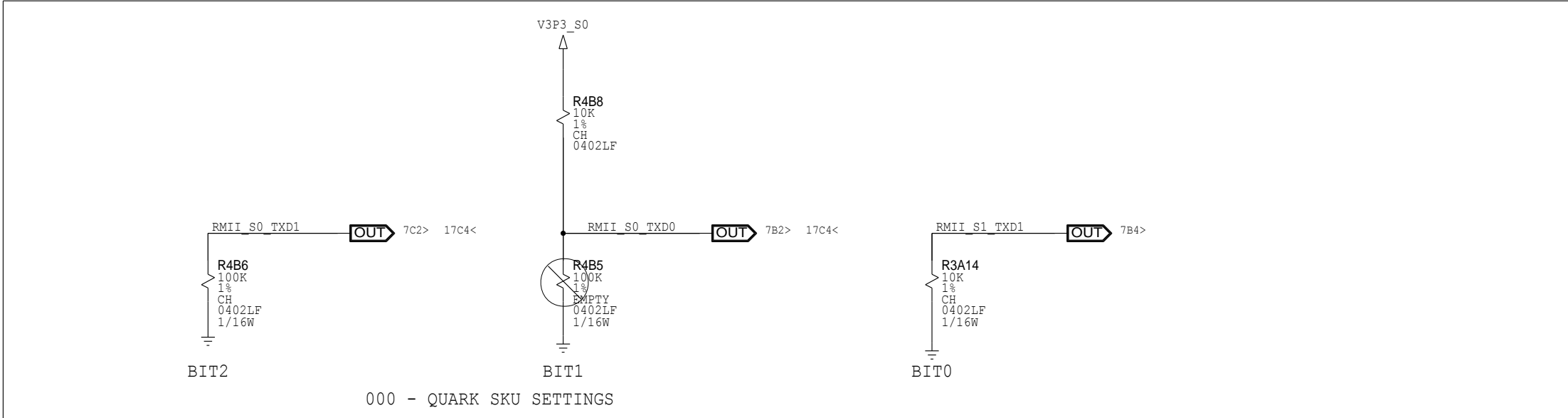
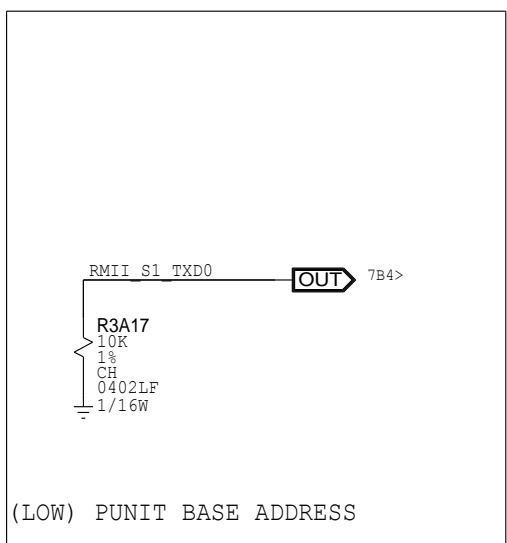
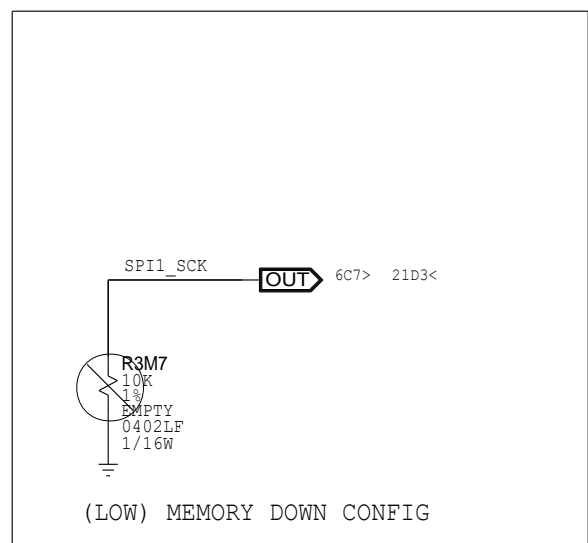
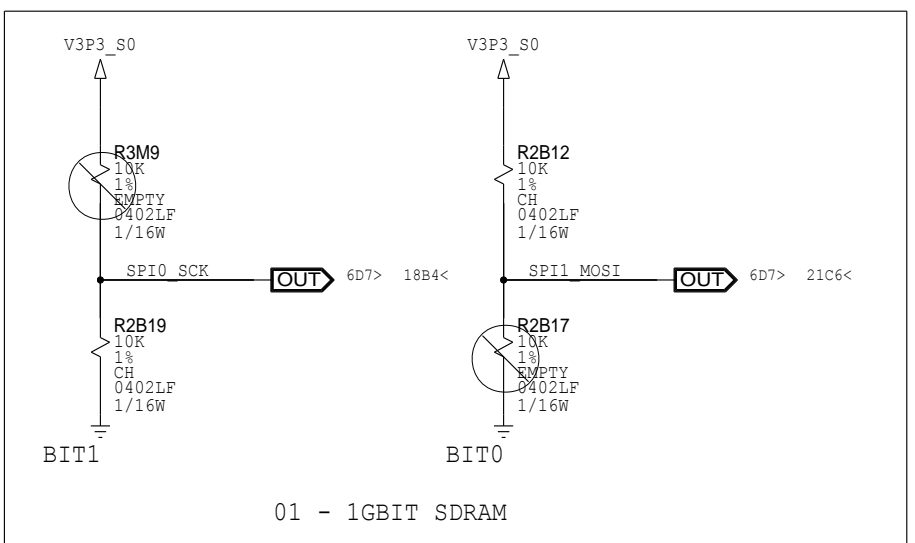
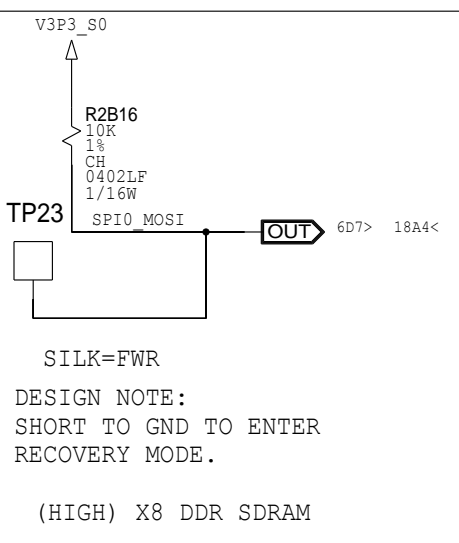
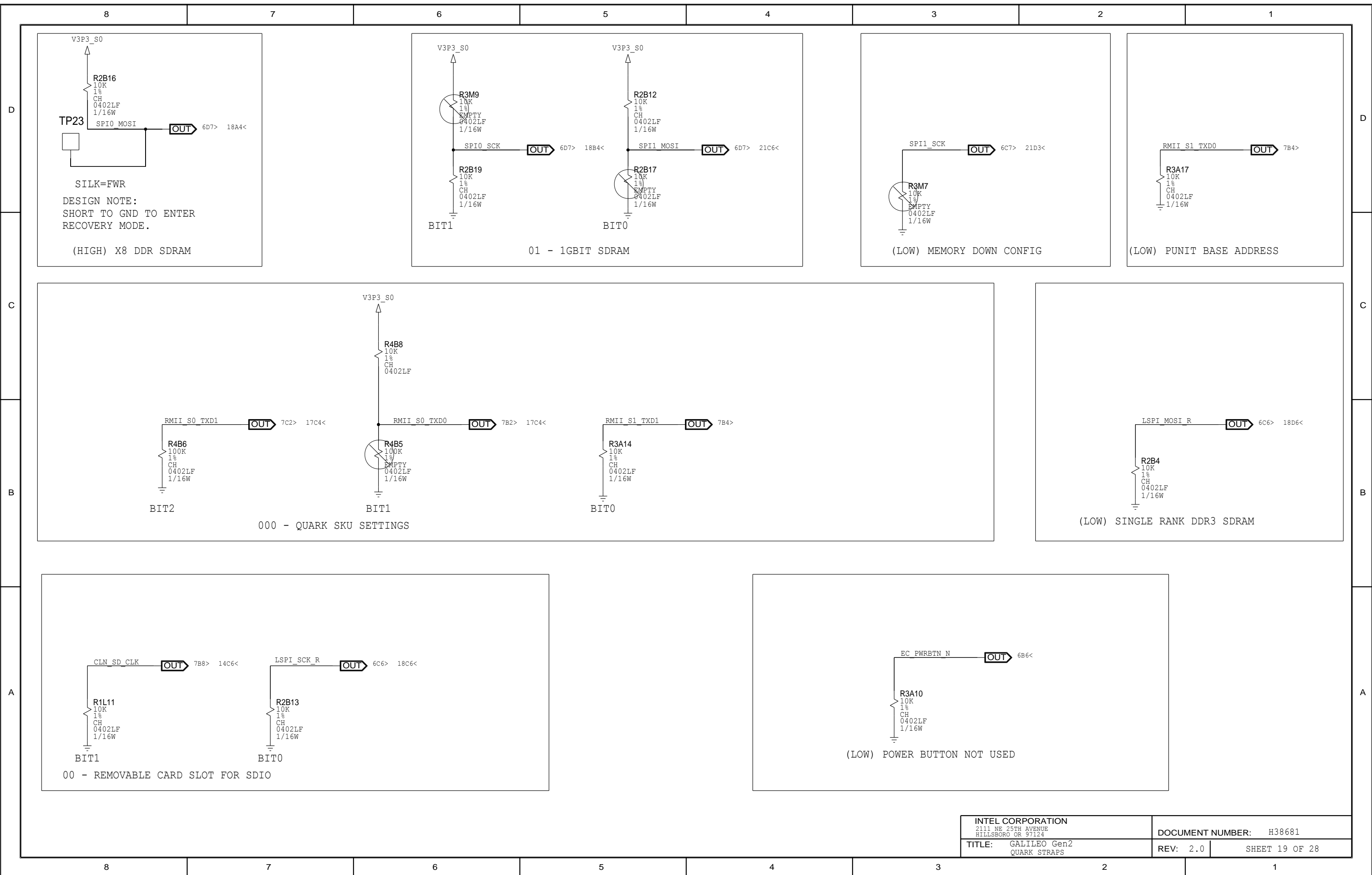
CAD NOTE:  
PLACE CAPACITORS CLOSE TO PFBOUT (PIN23)

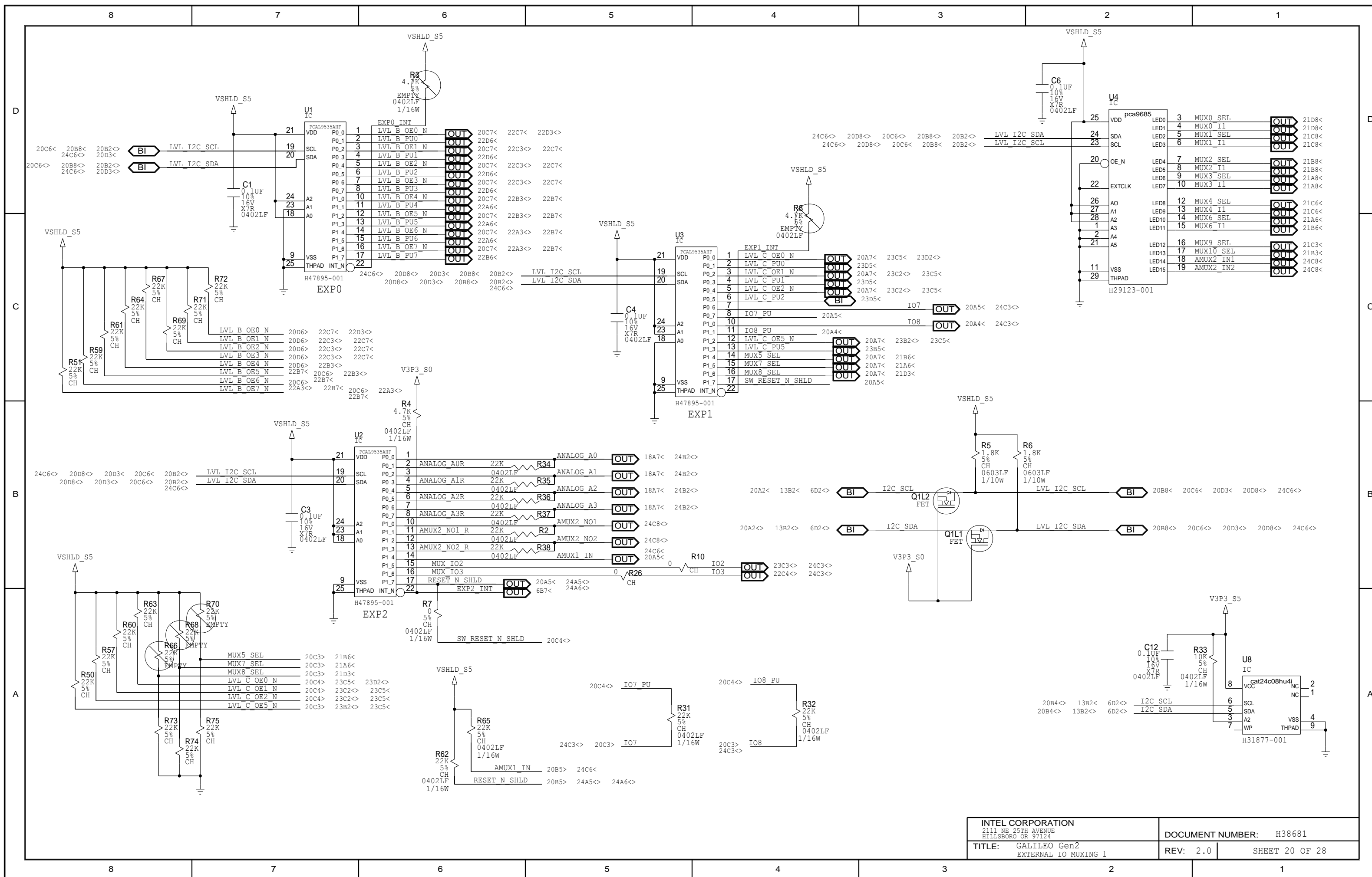
CAD NOTE:  
LENGTH MATCH CLOCK SPLIT. TRACE BETWEEN PIN 1 OF RESISTORS SHOULD BE SHORT

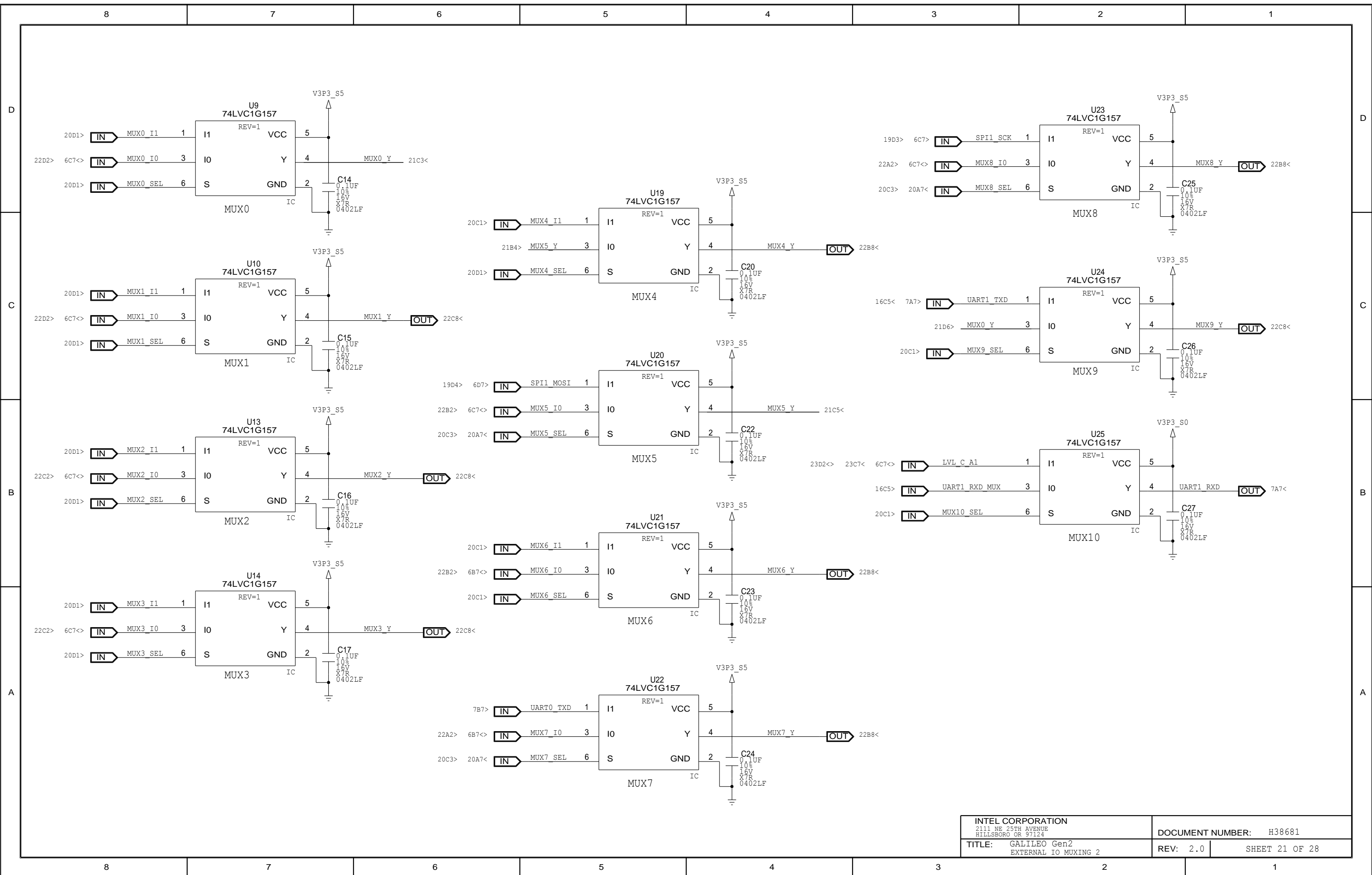
DESIGN NOTE:  
U16 IS DESIGNED FOR SILVERTEL AG9712S COMPONENT.

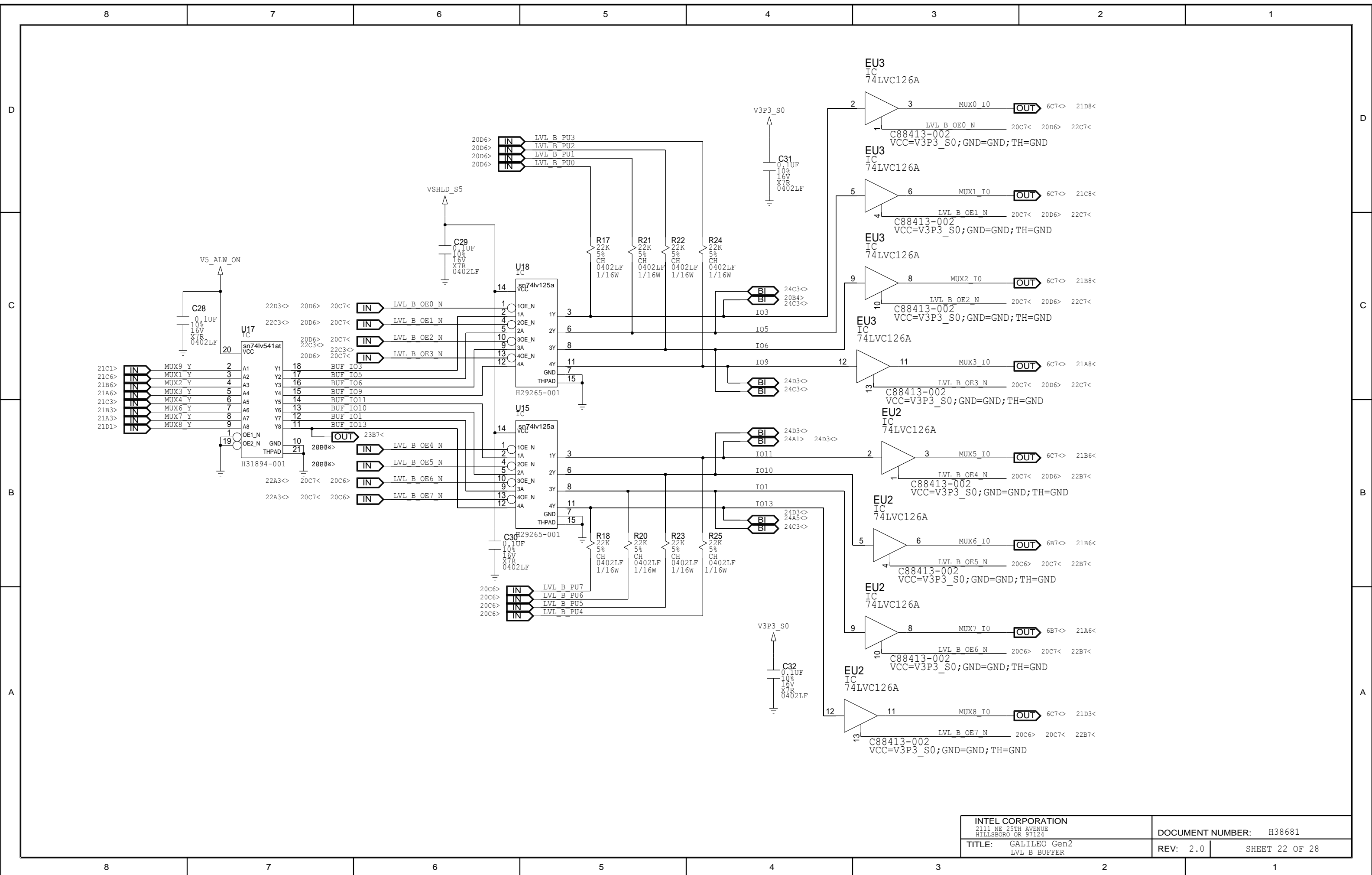
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 LAN		REV: 2.0	SHEET 17 OF 28

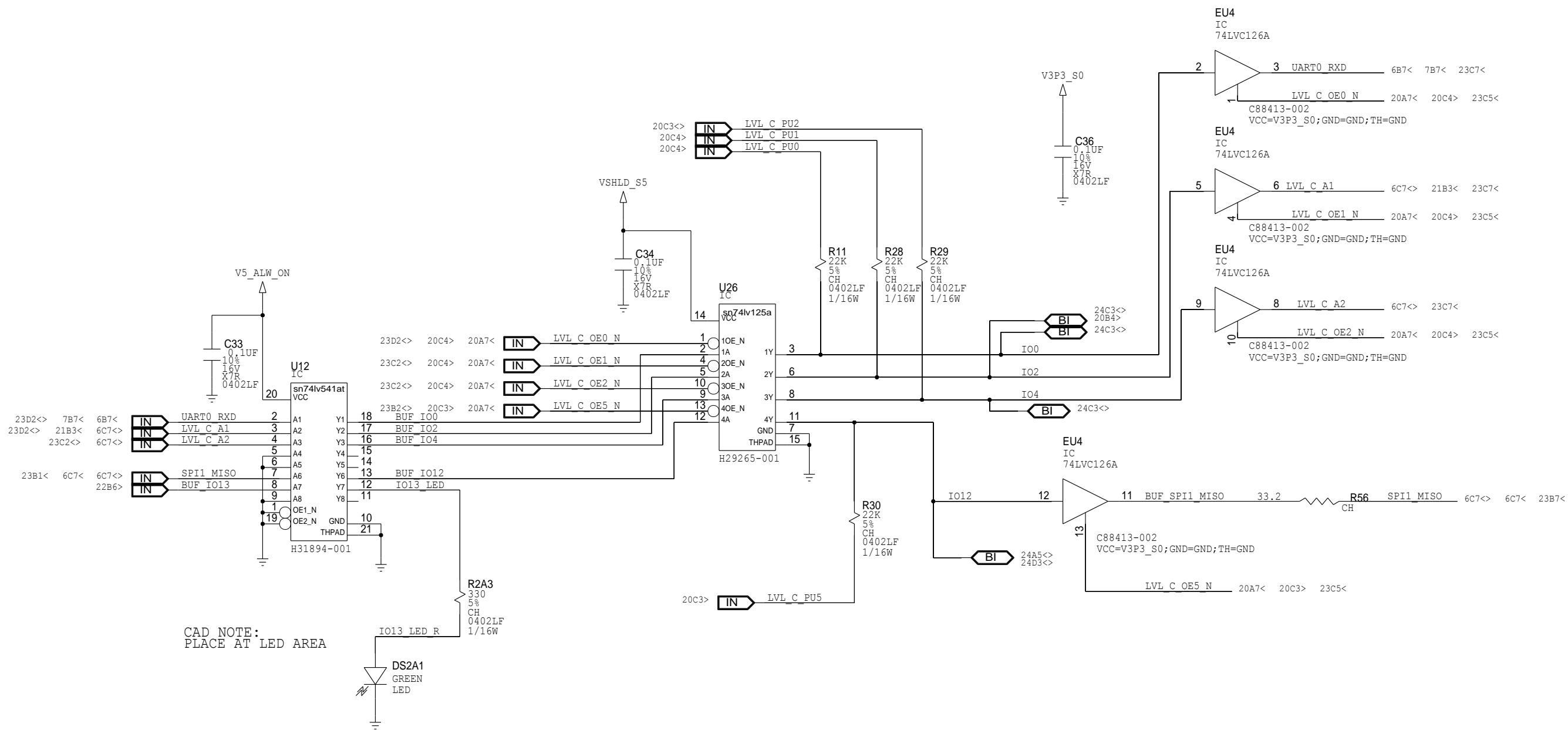




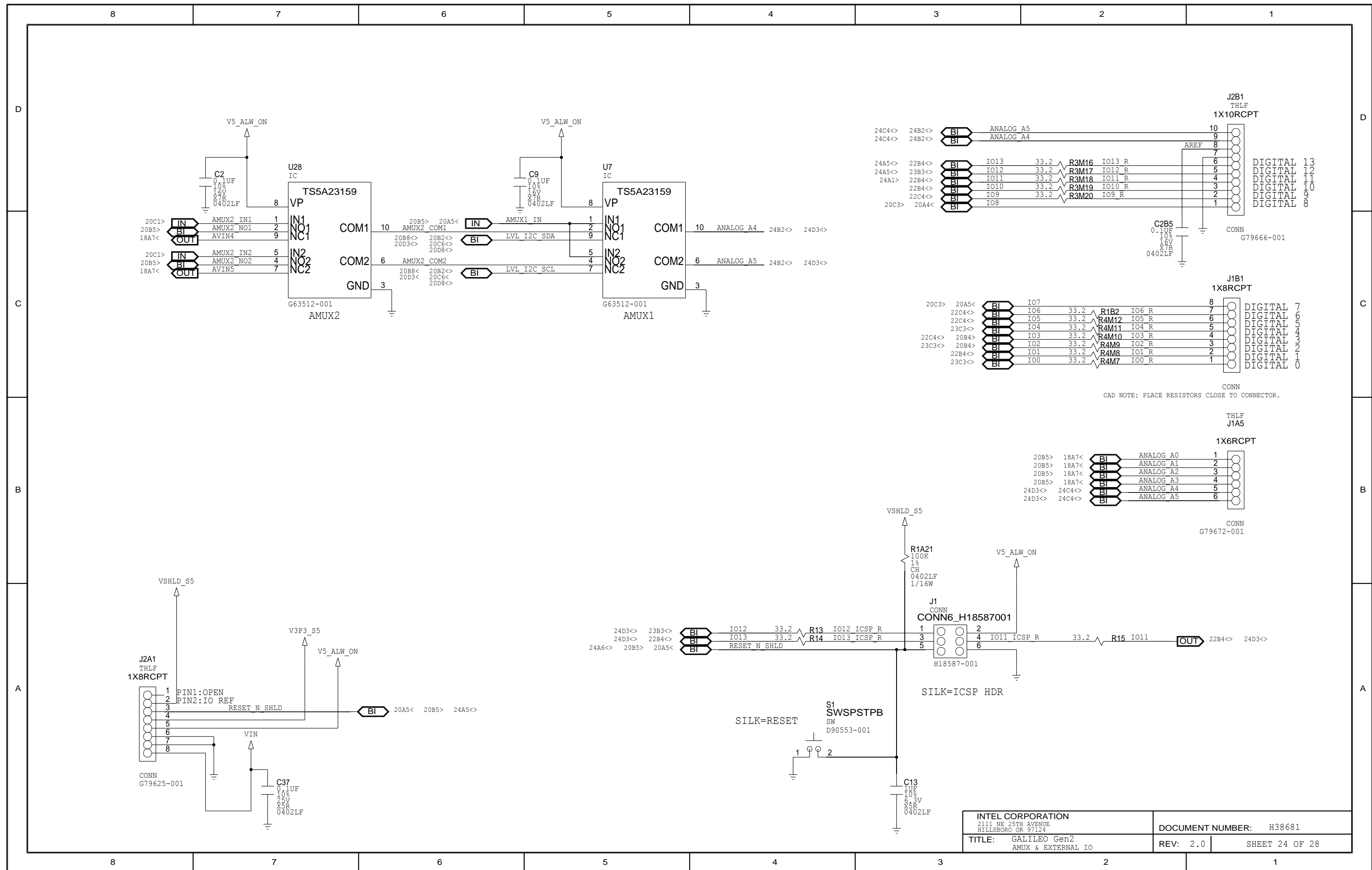






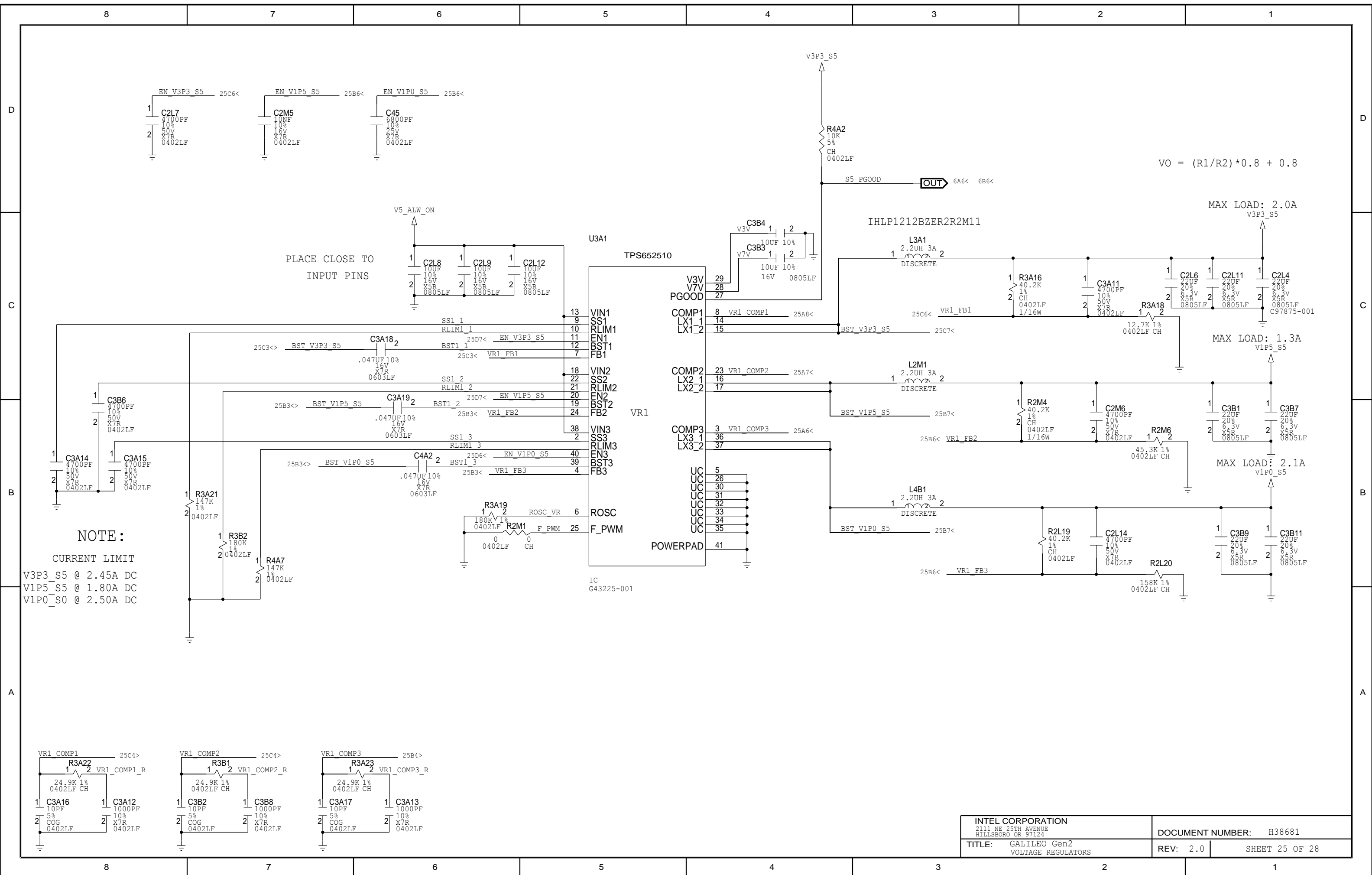


INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 LVL C BUFFER		REV: 2.0	SHEET 23 OF 28



CAD NOTE: PLACE RESISTORS CLOSE TO CONNECTOR.



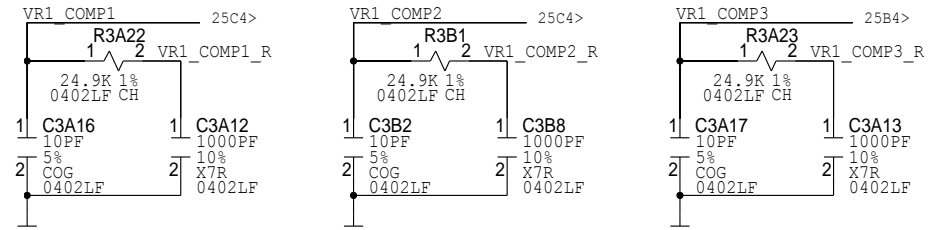


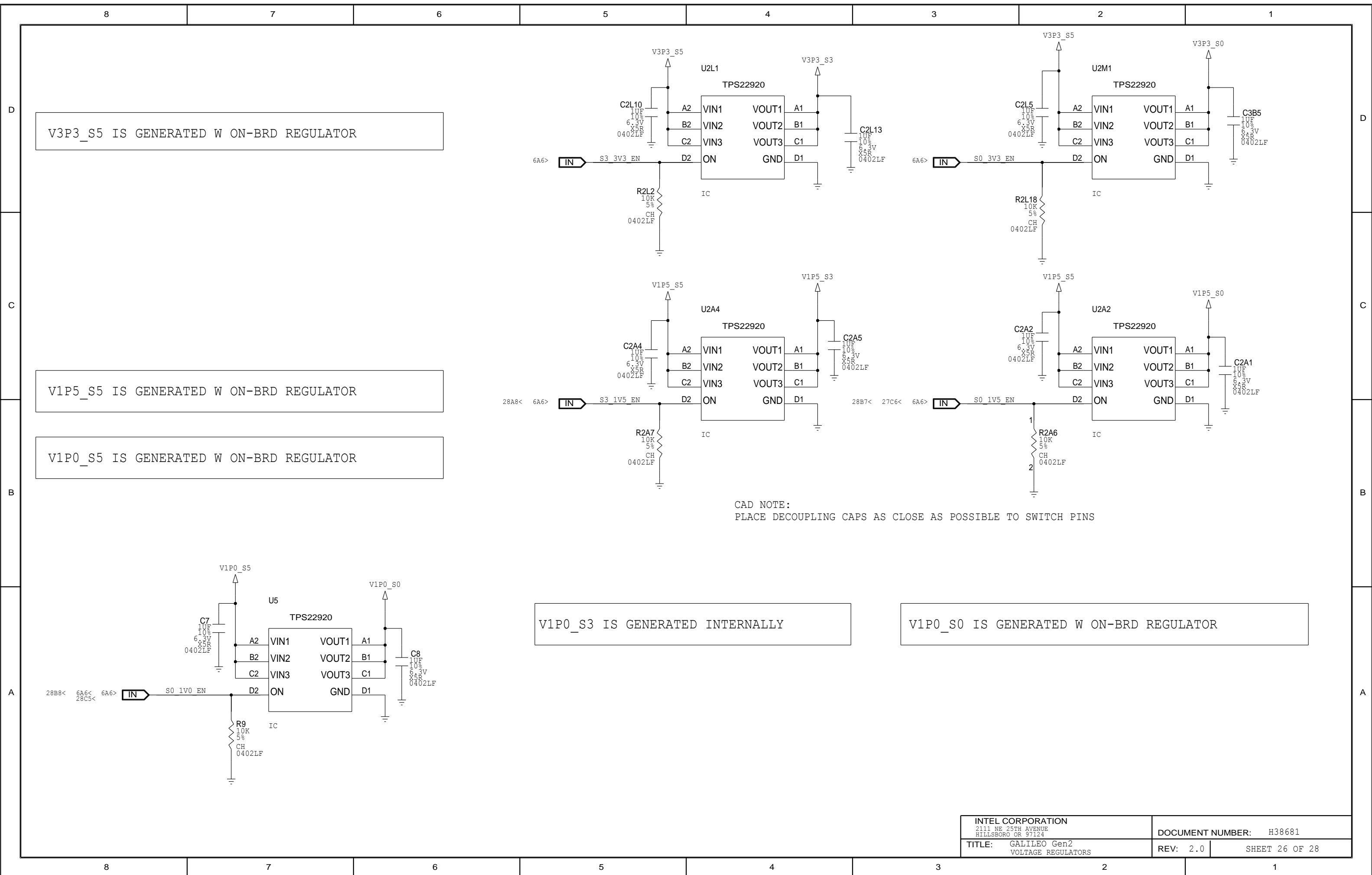
$$VO = (R1/R2) * 0.8 + 0.8$$

PLACE CLOSE TO INPUT PINS

**NOTE:**

- CURRENT LIMIT
- V3P3\_S5 @ 2.45A DC
- V1P5\_S5 @ 1.80A DC
- V1P0\_S5 @ 2.50A DC





V3P3\_S5 IS GENERATED W ON-BRD REGULATOR

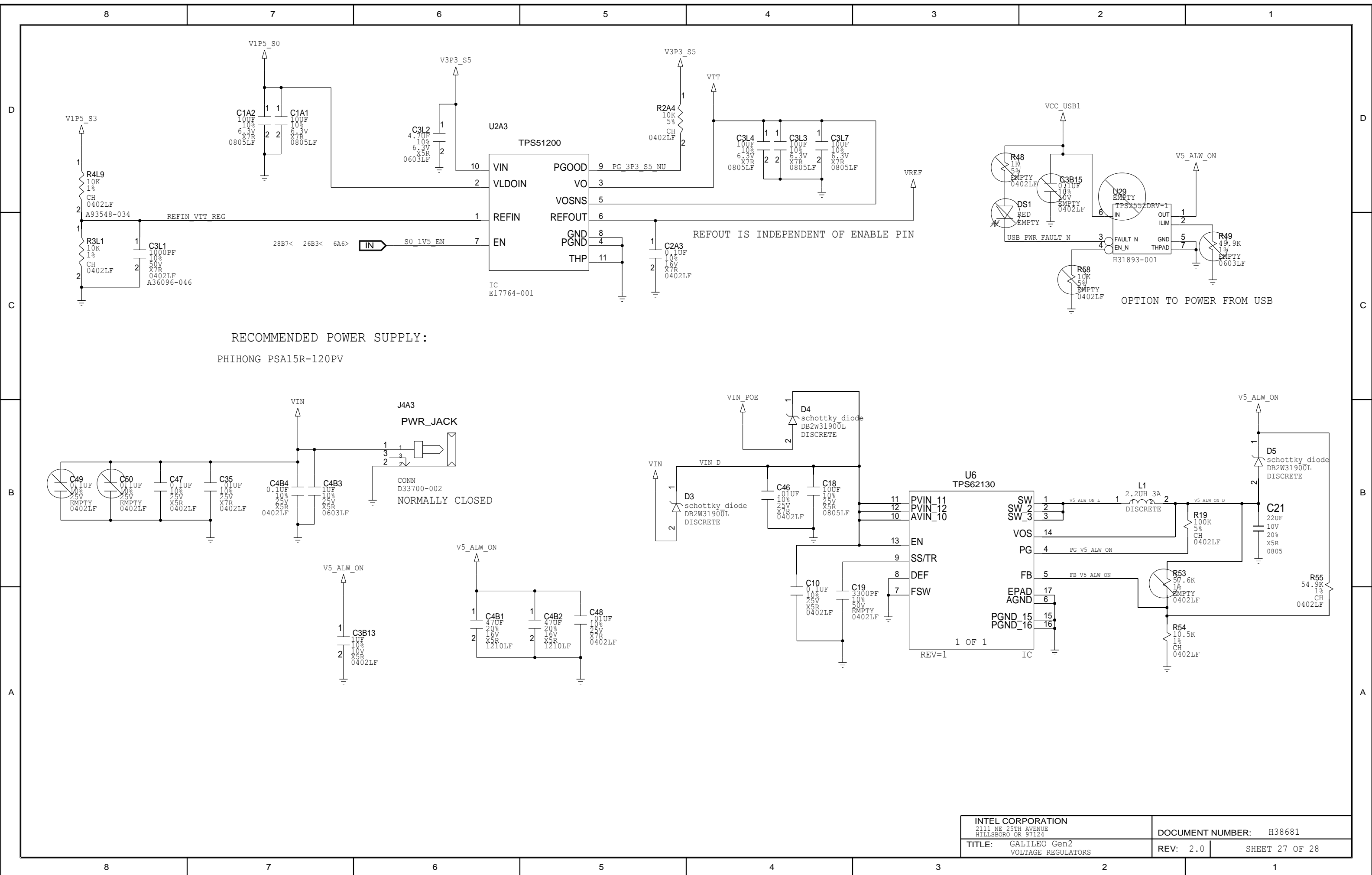
V1P5\_S5 IS GENERATED W ON-BRD REGULATOR

V1P0\_S5 IS GENERATED W ON-BRD REGULATOR

V1P0\_S3 IS GENERATED INTERNALLY

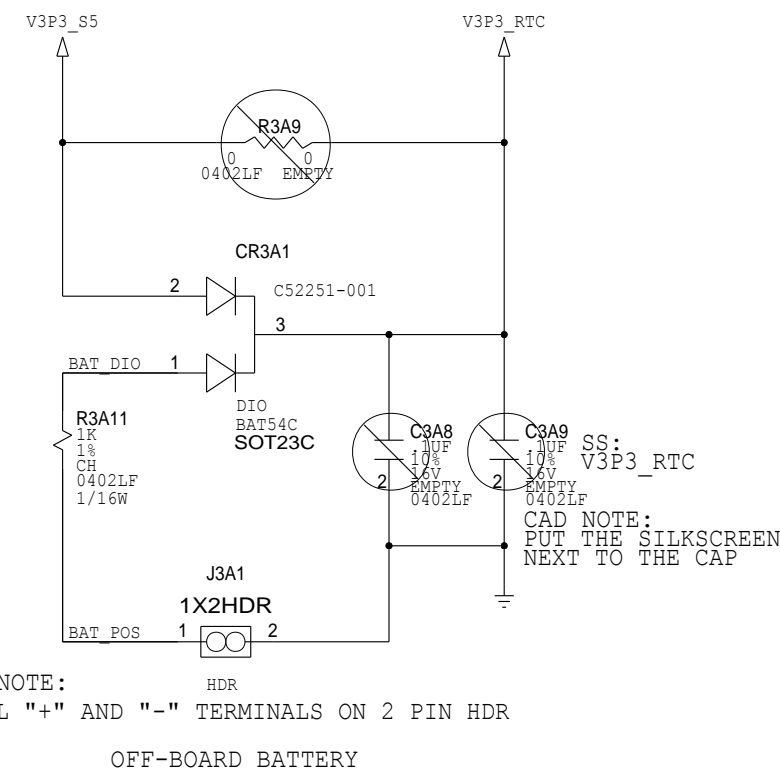
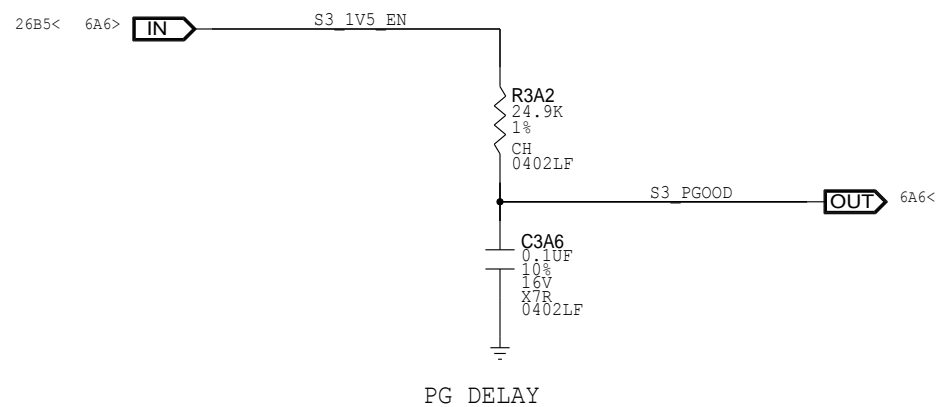
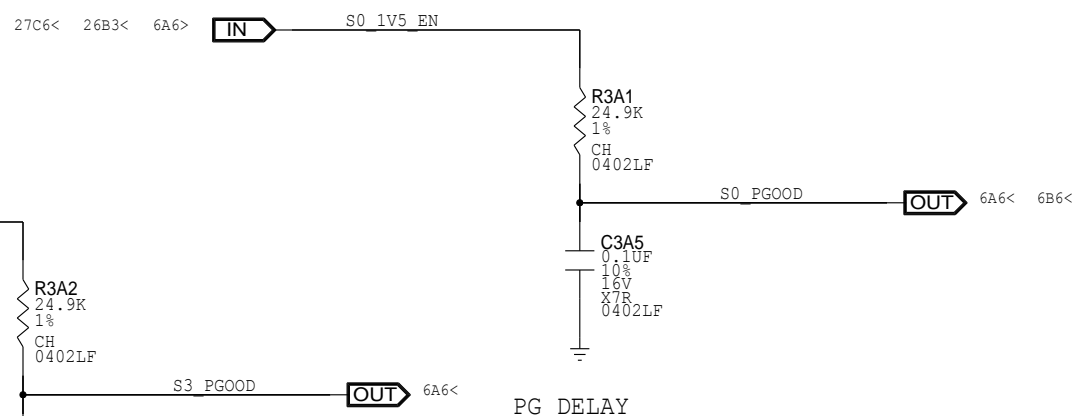
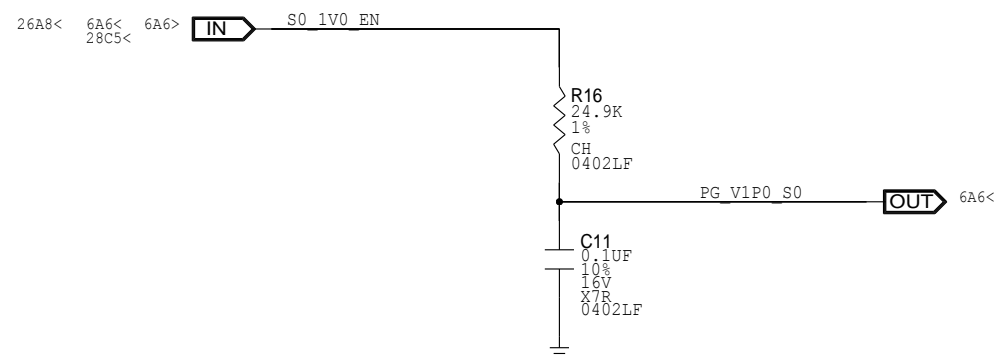
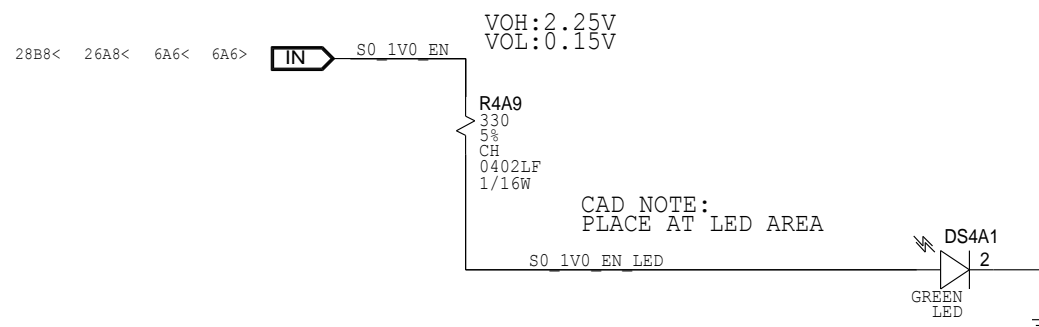
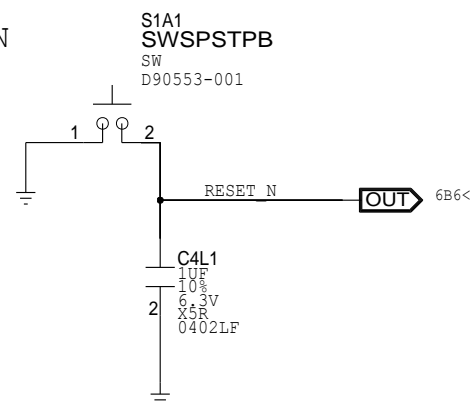
V1P0\_S0 IS GENERATED W ON-BRD REGULATOR

CAD NOTE:  
PLACE DECOUPLING CAPS AS CLOSE AS POSSIBLE TO SWITCH PINS



NOTE: RESET\_N HAS AN INTERNAL PU TO V3P3\_S3

SS:  
REBOOT BUTTON



CAD NOTE:  
LABEL "+" AND "-" TERMINALS ON 2 PIN HDR  
OFF-BOARD BATTERY

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 POWER BUTTONS & MISC		REV: 2.0	SHEET 28 OF 28