Electrical Characterization Design and Methodologies Guide

May 2018

Revision 001

Document Number: 337658-001US

Notice: This document contains information on products in the design phase of development. The information here is subject to change without notice. Do not finalize a design with this information.

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software, or service activation. Learn more at intel.com, or from the OEM or retailer.

No computer system can be absolutely secure. Intel does not assume any liability for lost or stolen data or systems or any damages resulting from such losses.

You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

This document contains information on products, services and/or processes in development. All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest Intel product specifications and roadmaps.

Intel disclaims all express and implied warranties, including without limitation, the implied warranties of merchantability, fitness for a particular purpose, and non-infringement, as well as any warranty arising from course of performance, course of dealing, or usage in trade.

Warning: Altering PC clock or memory frequency and/or voltage may (i) reduce system stability and use life of the system, memory and processor; (ii) cause the processor and other system components to fail; (iii) cause reductions in system performance; (iv) cause additional heat or other damage; and (v) affect system data integrity. Intel assumes no responsibility that the memory, included if used with altered clock frequencies and/or voltages, will be fit for any particular purpose. Check with memory manufacturer for warranty and additional details.

Tests document performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit http://www.intel.com/performance.

Cost reduction scenarios described are intended as examples of how a given Intel- based product, in the specified circumstances and configurations, may affect future costs and provide cost savings. Circumstances will vary. Intel does not guarantee any costs or cost reduction.

Results have been estimated or simulated using internal Intel analysis or architecture simulation or modeling, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance.

Intel does not control or audit third-party benchmark data or the web sites referenced in this document. You should visit the referenced web site and confirm whether referenced data are accurate.

Intel is a sponsor and member of the Benchmark XPRT Development Community, and was the major developer of the XPRT family of benchmarks. Principled Technologies is the publisher of the XPRT family of benchmarks. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases.

Copies of documents which have an order number and are referenced in this document may be obtained by calling 1-800-548-4725 or by visiting www.intel.com/design/literature.htm.

Intel, the Intel logo, and Xeon are trademarks of Intel Corporation in the U.S. and/or other countries.

*Other names and brands may be claimed as the property of others.

Copyright © 2018, Intel Corporation. All Rights Reserved.

Contents

Figures

Tables

Revision History

Document Number	Revision Number	Description	Date
337658	001	• Initial release of the document.	May 2018

1 Abstract

Channel loss is a dominant factor for the signaling performance of high-speed I/Os. Some platform design guides clearly specify the Printed Circuit Board (PCB) trace-only loss requirement. The via effect has a big impact on the loss of the entire channel and how to characterize the loss of a stripline design with the via effect being de-embedded is very important for a designer to select the right material and manufacturing process control, balancing the platform cost, and performance requirement.

An improper selection of PCB material may result in either a costly over design or an increased risk of platform performance. This is especially true for traces on a thicker board with a long via or any board with a long via stub. Furthermore, the impact of the via and the via stub is more prominent when low-loss PCB material is used.

Some methods for PCB trace loss characterization have been widely used in the industry, including Thru-Reflect-Line (TRL), Delta-L and Smart Fixture De-Embedding (SFD), to remove the unwanted via effect in the striplines. Some of the methods, such as TRL, require a series of measurement procedures with many de-embedding structures. How to effectively remove the via effect through a simple, efficient, and accurate approach in the high volume measurement is critical for platform designers, as well as PCB suppliers. In this paper, a study on PCB insertion loss measurement metrology is conducted to compare the accuracy and efficiency of different characterization methods.

2 Introduction

For the early stage PCB material selection, platform designers would like to have the accurate loss measurement to meet the channel requirement, because the PCB material contributes largely to the platform cost. Many metrologies have been proposed for PCB loss characterization in the industry. To understand the usage model and application for different PCB loss measurement metrologies, four characterization approaches, including Delta-L, SET2DIL, TRL, SFD with handheld probes and SMA launches, are designed in one single board to verify the loss measurement accuracy and efficiency. This is a good reference for users to select the appropriate metrology according to the design space, probing usage, accuracy and so on.

The metrology comparison is extremely critical for selecting the appropriate material for platform design. Without this comparison study, users did not understand the limitation of the certain methodology they have chosen for PCB loss characterization, and had resulted in mistakenly disqualifying materials which would have been a low cost solution for platform design.

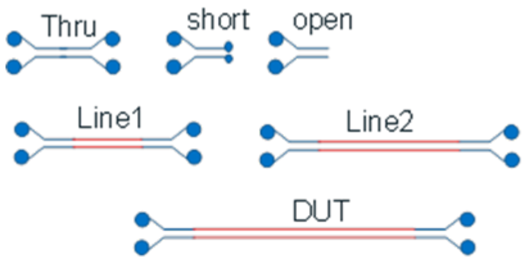
3 PCB Measurement Metrology

These four different measurement metrology, including TRL, SET2DIL, Delta-L and SFD, are briefly introduced in this section.

3.1 Thru-Reflect-Line (TRL) Heading 4 Style

This is a well-known de-embedding metrology and standard for the test fixture removal for PCB characterization in industry [1]. TRL is regarded as the golden reference to move the measurement reference plane from coaxial connectors to PCB structures. It requires various calibration structures with different routing lengths for the measurement frequency range shown in Figure 3-1. The process is complicated and it is less popular.

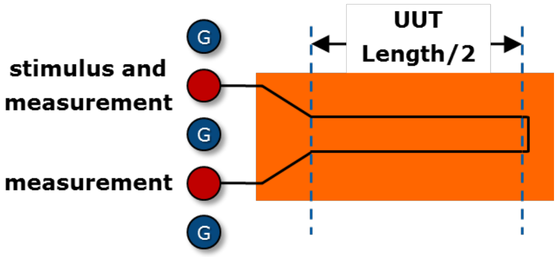
Figure 3-1. TRL Testing Structures



3.2 SET2DIL

This method uses single-ended TDR/TDT measurement to derive differential insertion loss (SDD21) [2]. Figure 3-2 shows that the testing structure is to short the middle of the original differential structure. Time domain step response is injected at one end, and the crosstalk is induced at the other end. By this short structure, the routing length can be half and the coupon size is small. But it lacks calibration and de-embedding capability, and the additional waveform manipulation/approximation during post-processing stage is required.

Figure 3-2. SET2DIL Testing Structures



3.3 Delta-L

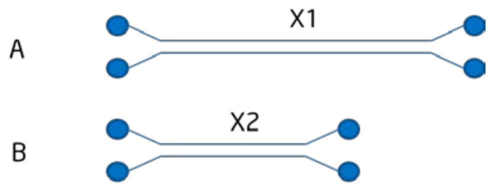
Delta-L uses two different routing structures for the stripline with the vias shown in Figure 3-3 [3-4]. The reference is the short routing “B” with the length of X1 inch and the other is the longer routing “A” with the length of X2 inch. Through Vector Network Analyzer (VNA) or Time-domain Reflection(TDR)/ Time-domain Transmission (TDT) measurement, the insertion loss difference between routing A and B is the loss of trace length (X1-X2) with via effect being de-embedded. The unit length loss, then, can be calculated.

Equation 1

$$\text{dB/unit loss} = [\text{Insertion Loss(A)} - \text{Insertion Loss(B)}] + / (X1 - X2)$$

Both stripline and microstrip can be used and this is an efficient de-embedding approach for transmission line structures without the requirement of various calibration structures. However, it is no suitable for full S parameter extraction.

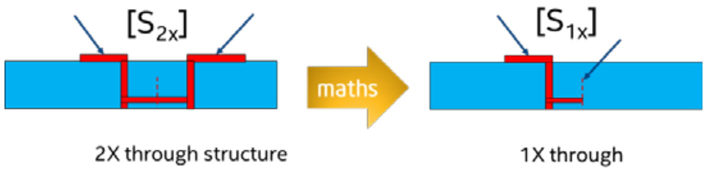
Figure 3-3. TRL Testing Structures



3.4 Smart Fixture De-Embedding (SFD)

The 4 port de-embedding measurement by using the 2X through structures is shown in Figure 3-4 [5]. Only one 2X through structure is needed. The S parameter of 1x through is mathematically calculated and it can significantly simplified calibration and de-embedding procedures. However, it needs one proprietary software.

Figure 3-4. 2X Through Structure



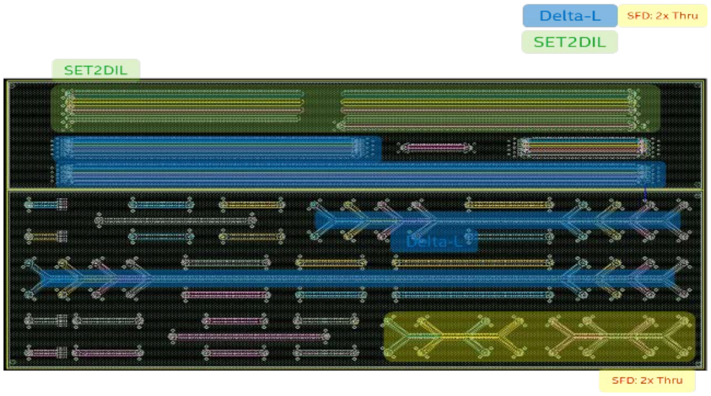
4 Characterization Board Design

These metrologies with the corresponding probing solution are also very important in the practical application for the high-volume measurement. Hence, Table 4-1 lists the configuration of testing structures with the selected probing options. The physical routings of these straight lines with the GERBER rotation of 10 degrees are shown in Figure 4-1, and the PCB stackup is based on 12-layer reference stackup of 72.2-mil thick for PCB loss with 3-mil core design.

Table 4-1. Testing Configurations

Method	Description	Probing
Delta-L	5 inch and 10 inch	SMA and Handheld probe
SET2DIL	8 inch	Handheld Pico-probe
SFD	5 inch and 10inch	SMA and Handheld probe
TRL*3(Thru-Reflect, Line) (1-inch Reference)	10 inch	SMA

Figure 4-1. Characterization Board Design



5 Results

Figure 5-1 shows the insertion loss results of 5 inch routings on the top, 3rd, 6th and 10th layers. L1 is the microstrip design without the via stub and L10 has the shorter via stub from 10th layer to 12th layer. The routing on L3 has the longer via stub from 3rd layer to 12th layer and the resonant frequency is around 18.7 GHz. It not only rejects the energy at the resonance by the via stub but also degrades the insertion loss profile. When the via or via stub is longer, the impact on the insertion loss is more serious.

Figure 5-2 is the frequency response comparison between routing on L3 with the via effect and only stripline characteristics by the Delta-L approach. De-embedding is very important for the accurate insertion loss profile. In the real manufacture, these two vias of 5 inch and 10 inch routings are not identical and this can explain that Delta-L curve is not so smooth close to the resonant frequency.

Figure 5-1. Via Impact on the Insertion Loss Profile

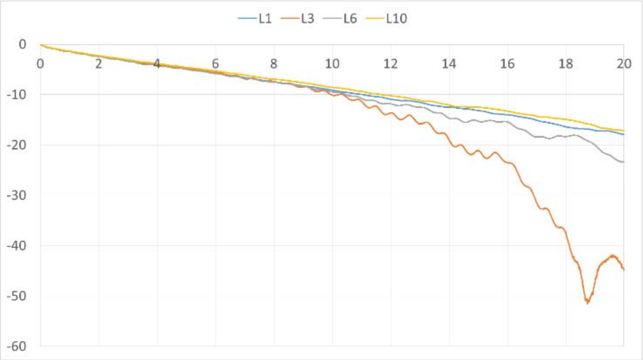
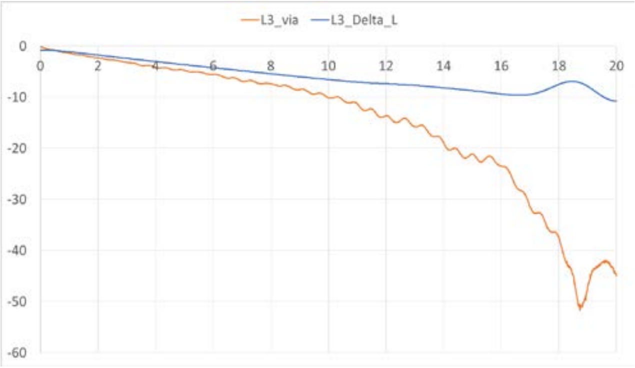


Figure 5-2. De-Embedding for Layer 3



Measurement results of different characterization methodologies, including Delta-L, SFD*, and TRL, are consistent for the microstrip and stripline in Table 5-1 and Table 5-2. The Delta-L results using SMA and handheld probes are consistent. The frequency response of TRL and Delta-L using SMA launches and handheld probes are correlated up to 20 GHz shown in Figure 5-3. However, measurement results using SET2DIL without de-embedding was pessimistic, especially at 8 GHz.

Figure 5-3. Frequency Response of Delta-L and TRL with SMA and Handheld Probes

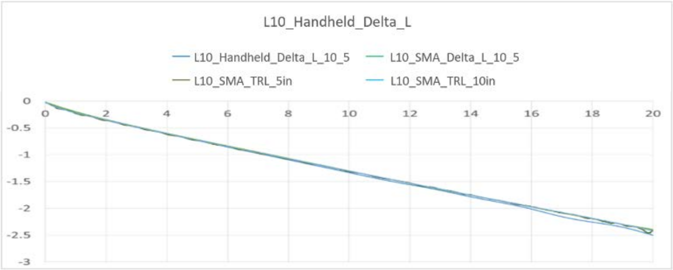


Table 5-1. Microstrip Result

Layer		Probing	
Probe	Method	Loss (dB/inch)	
		4 GHz	8 GHz
Pico-Probe	SET2DIL	0.68	1.23
Handheld	Delta_L	0.64	1.16

Table 5-2. Stripline Result

Layer			L3		L6		L10	
Probe	Method	Type	Loss(dB/inch)		Loss(dB/inch)		Loss(dB/inch)	
			4GHz	8GHz	4GHz	8GHz	4GHz	8GHz
Pico-Probe	SET2DIL	8 in	0.62	1.38	0.69	1.38	0.65	1.18
Handheld	TpNA	10in_5in	0.6	1.08	0.64	1.15	0.61	1.09
	Delta_L	10in_5in	0.61	1.08	0.65	1.15	0.61	1.09
	SFD	10in_5in	0.61	1.09	0.66	1.16	0.62	1.09
SMA	Delta_L	10in_5in	0.59	1.06	0.65	1.15	0.6	1.07
	SFD	10in_5in	0.6	1.07	0.65	1.15	0.61	1.1
	TRL	5in	0.62	1.08	0.68	1.16	0.62	1.09
		10in	0.6	1.07	0.65	1.16	0.61	1.08

6 Summary

A different PCB insertion loss metrology comparison was conducted for the measurement accuracy and efficiency. Delta-L is a simple way to get correct loss without fancy and complex de-embedding algorithms. A cross-check of the results show that the de-embedding results, including TRL, SFD and Delta-L, are consistent and accurate.

7 References

[1] Agilent Technologies*, “Stripline TRL calibration fixtures for 10- Gigabit interconnect analysis,” 2006

[2] J. loyer, R. Kunze, “SET2DIL: Method to Derive Differential Insertion Loss from Single-Ended TDR/TDT Measurements,” 2010 DesignCon

[3] J. Hsu, T. Su, K. Xiao, X. Ye, S. Huang, Y. Li, “Delta-L Methodology for Efficient PCB Trace Loss Characterization,” Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), 2014 9th International.

[4] *Intel Delta-L Methodology for Electrical Characterization*, Rev. 330223-001, http://www.intel.com/content/www/us/en/processors/xeon/delta-l-methodology-for-electrical-characterization-guide.html

[5] X. Ye, J. Fan and J. Drewniak, "New De-embedding Techniques for PCB Transmission-Line Characterization," to be published in Proc. of DesignCon 2015.