Intel Delta-L Methodology for Electrical Characterization

Intel Corporation
Data Center Platform Application Engineering
February 2014
Reference Number: 330223-001
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Outline

• De-embedding Overview

• Intel Delta-L Methodology

• Summary
De-embedding Overview
De-embedding Overview

- Why De-embedding
- De-embedding basics and General de-embedding approaches
- What if NOT de-embedding?
- Summary
Why De-embedding?

• In high speed interconnect designs, calibration is a very critical step to assure accuracy of measurement.

• Most instruments make measurements at well calibrated reference planes.

• Test fixtures are often needed to connect the calibrated reference plane to the device under test (a.k.a. DUT).

• These test fixtures distort measurement results and must be de-embedded.
The Importance of Reference Planes

Most instruments can move ref planes to here easily.

Probes can move ref planes here with calibration Kit.

De-embedding structures needed to move ref planes here.
General De-embedding Approaches

There are generally two types of approaches to remove the effects of test fixtures:

- The first approach uses specialized calibration standards that are inserted at the end of the test fixture, and performing a calibration process to move the reference plane to the end of the test fixture.

- The second approach makes direct S parameter measurements of the DUT with test fixture, meanwhile acquires the S parameter of the test fixture through either direct measurement or simulation. The S parameter of the DUT without test fixture can be mathematically calculated from above two S parameter data.
General De-embedding Approach#1

SOLT, TRL, LRM, and so forth (Separate de-embedding Structure)
General De-embedding Approach#2

S parameter of the test fixture can be derived through:

- Measurement
- Vendor provided
- Simulation
De-embedding Basics

Convert S parameter to T matrix first

\[
\begin{bmatrix}
T_A^{-1} & T_A & T_{DUT} & T_B & T_B^{-1}
\end{bmatrix}
= T_{DUT}
\]

\[
[T_{Measured}] = [T_L][T_{DUT}][T_R]
\]

\[
[T_{De-embedded}] = [T_L]^{-1}[T_{Measured}][T_R]^{-1}
= [T_L]^{-1}[T_L][T_{DUT}][T_R][T_R]^{-1} = [T_{DUT}]
\]
What if NOT de-embedding?
Example: if the via is NOT de-embedded

\[|S_{21}| \text{ of same Tline, with and without via}\]

10% error in reported Loss @ 4 GHz

20% error in reported Loss @ 8 GHz
How to De-embedding the Via

• Don’t de-embed it
  • It is part of the channel you need to characterize
  • Perform simulation and measurement correlation with via included
• De-embed through simulation
  • Use simulated via model to de-embed the results
    Note: need to perform correlation to make sure via model is correct
• De-embed through de-embedding structures
  • Delta-L Methodology
  • TRL
  • AFR* (Automatic Fixture Removal), ... and so forth.
• Minimize the via impact
  • Microvia
  • Backdrill, and so forth
• Others...
Delta-L Methodology
Delta-L Loss Characterization

- Direct through measurement for insertion loss.
  - Insertion Loss of structure A: IL (A) --- \{X1 inches + vias\}
  - Insertion Loss of structure B: IL (B) --- \{X2 inches + vias\}
  - dB/inch loss = \(\frac{[IL(A) - IL(B)]}{(X1 - X2)}\)

  **Note**: Suggested length: \(X2 \geq 4 \text{ inch}\), \(X1-X2 \geq 4 \text{ inch}\)

- No full SOLT or TRL calibration needed;
- VNA or TDR/TDT measurement
  - If TDT/TDT measured is performed, it needs to be converted to S parameter first.
Convergence of Loss versus Delta-L

Trace length of the 1st structure (X2) = 4 inches

Note: This result is under a very stressed condition with 80 mils of the via stub. In the reality, it can be probed from the opposite side of the board.
Example of Test Coupon Design

- Angle Routing

- Serpentine Design

NOTICE: THESE TEST COUPON DESIGNS ARE SUBJECT TO CHANGE WITHOUT NOTICE.
Delta-L Result in the Layer 3 (Angle Routing)
Delta-L Result in the Layer 6 (Angle Routing)
Delta-L Result in the Layer 3 (Serpentine Design)
Delta-L Result in the Layer 6 (Serpentine Design)
Angle Routing and Serpentine

<table>
<thead>
<tr>
<th></th>
<th>Angle L3</th>
<th>Serpentine L3</th>
<th>Angle L6</th>
<th>Serpentine L6</th>
<th>Angle L1</th>
<th>Serpentine L1</th>
</tr>
</thead>
<tbody>
<tr>
<td>4GHz</td>
<td>0.68</td>
<td>0.67</td>
<td>0.69</td>
<td>0.66</td>
<td>0.79</td>
<td>0.79</td>
</tr>
<tr>
<td>8GHz</td>
<td>1.22</td>
<td>1.25</td>
<td>1.26</td>
<td>1.20</td>
<td>1.36</td>
<td>1.40</td>
</tr>
<tr>
<td>10GHz</td>
<td>1.50</td>
<td>1.50</td>
<td>1.54</td>
<td>1.44</td>
<td>1.64</td>
<td>1.70</td>
</tr>
</tbody>
</table>

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Summary

• De-embedding is critical for the accuracy of interconnect measurement

• If de-embedding procedure is skipped in measurement (for whatever reason)
  • Need to understand the consequence
  • Need to know the S parameter of test fixture (measurement or simulation)

• Intel Delta-L methodology is good in the electrical characterization with the de-embedding to remove the unwanted effect, such as the via