Intel Delta-L Methodology for Electrical Characterization

Intel Corporation
Data Center Platform Application Engineering
February 2014
Reference Number: 330223-001

Legal Disclaimer

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

A "Mission Critical Application" is any application in which failure of the Intel Product could result, directly or indirectly, in personal injury or death. SHOULD YOU PURCHASE OR USE INTEL'S PRODUCTS FOR ANY SUCH MISSION CRITICAL APPLICATION, YOU SHALL INDEMNIFY AND HOLD INTEL AND ITS SUBSIDIARIES, SUBCONTRACTORS AND AFFILIATES, AND THE DIRECTORS, OFFICERS, AND EMPLOYEES OF EACH, HARMLESS AGAINST ALL CLAIMS COSTS, DAMAGES, AND EXPENSES AND REASONABLE ATTORNEYS' FEES ARISING OUT OF, DIRECTLY OR INDIRECTLY, ANY CLAIM OF PRODUCT LIABILITY, PERSONAL INJURY, OR DEATH ARISING IN ANY WAY OUT OF SUCH MISSION CRITICAL APPLICATION, WHETHER OR NOT INTEL OR ITS SUBCONTRACTOR WAS NEGLIGENT IN THE DESIGN, MANUFACTURE, OR WARNING OF THE INTEL PRODUCT OR ANY OF ITS PARTS.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined". Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents that have an order number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725 or by visiting Intel’s website at http://www.intel.com/design/literature.htm.

Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. See http://www.intel.com/products/processor_number for details.

Intel and the Intel logo are trademarks of Intel Corporation in the United States and other countries.

* Other names and brands may be claimed as the property of others.

Outline

- De-embedding Overview
- Intel Delta-L Methodology
- Summary

De-embedding Overview

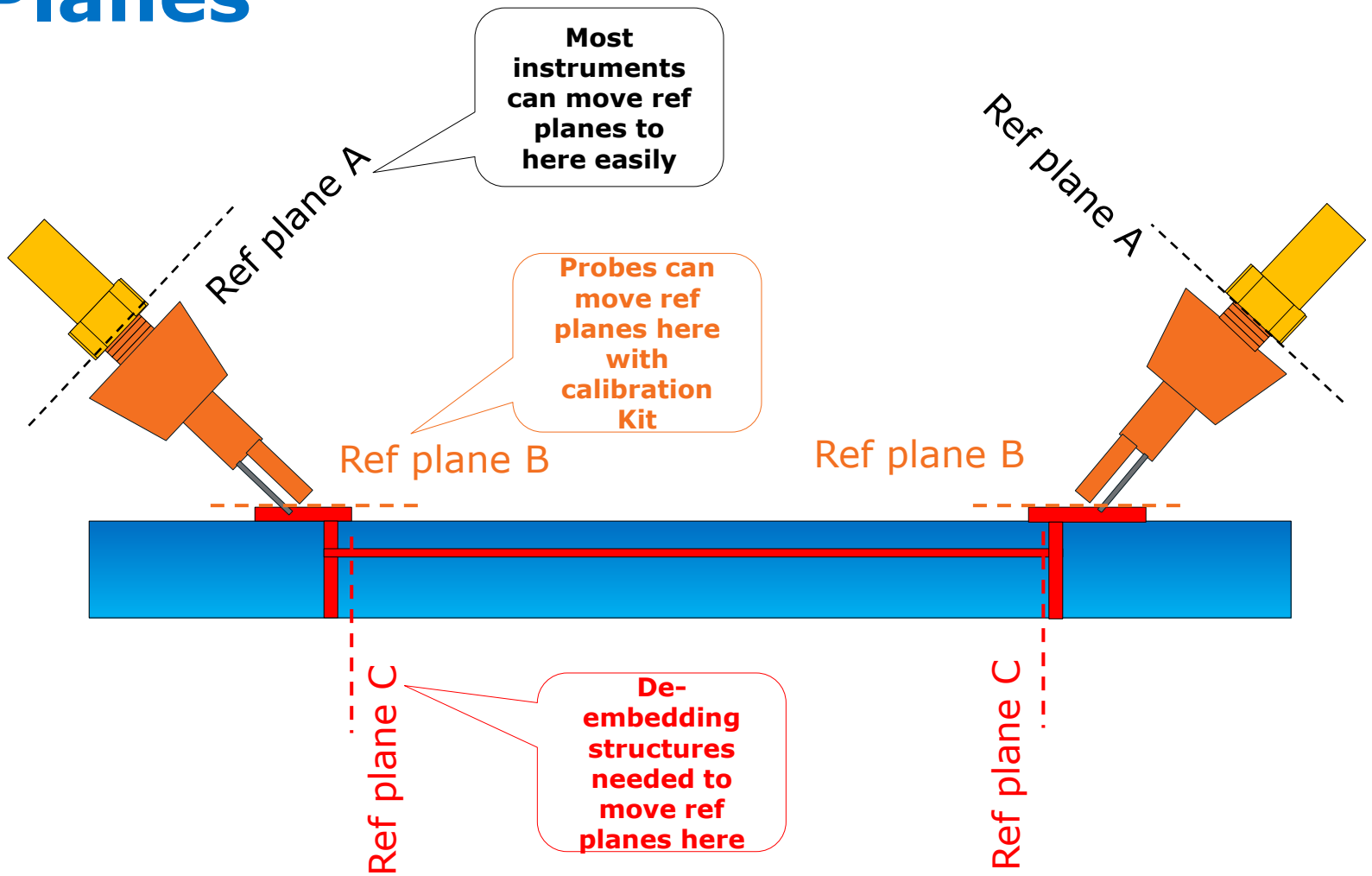
De-embedding Overview

- Why De-embedding
- De-embedding basics and General de-embedding approaches
- What if NOT de-embedding?
- Summary

Why De-embedding?

- In high speed interconnect designs, calibration is a very critical step to assure accuracy of measurement
- Most instruments make measurements at well calibrated reference planes
- Test fixtures are often needed to connect the calibrated reference plane to the device under test (a.k.a. DUT)
- These test fixtures distort measurement results and must be de-embedded

The Importance of Reference Planes

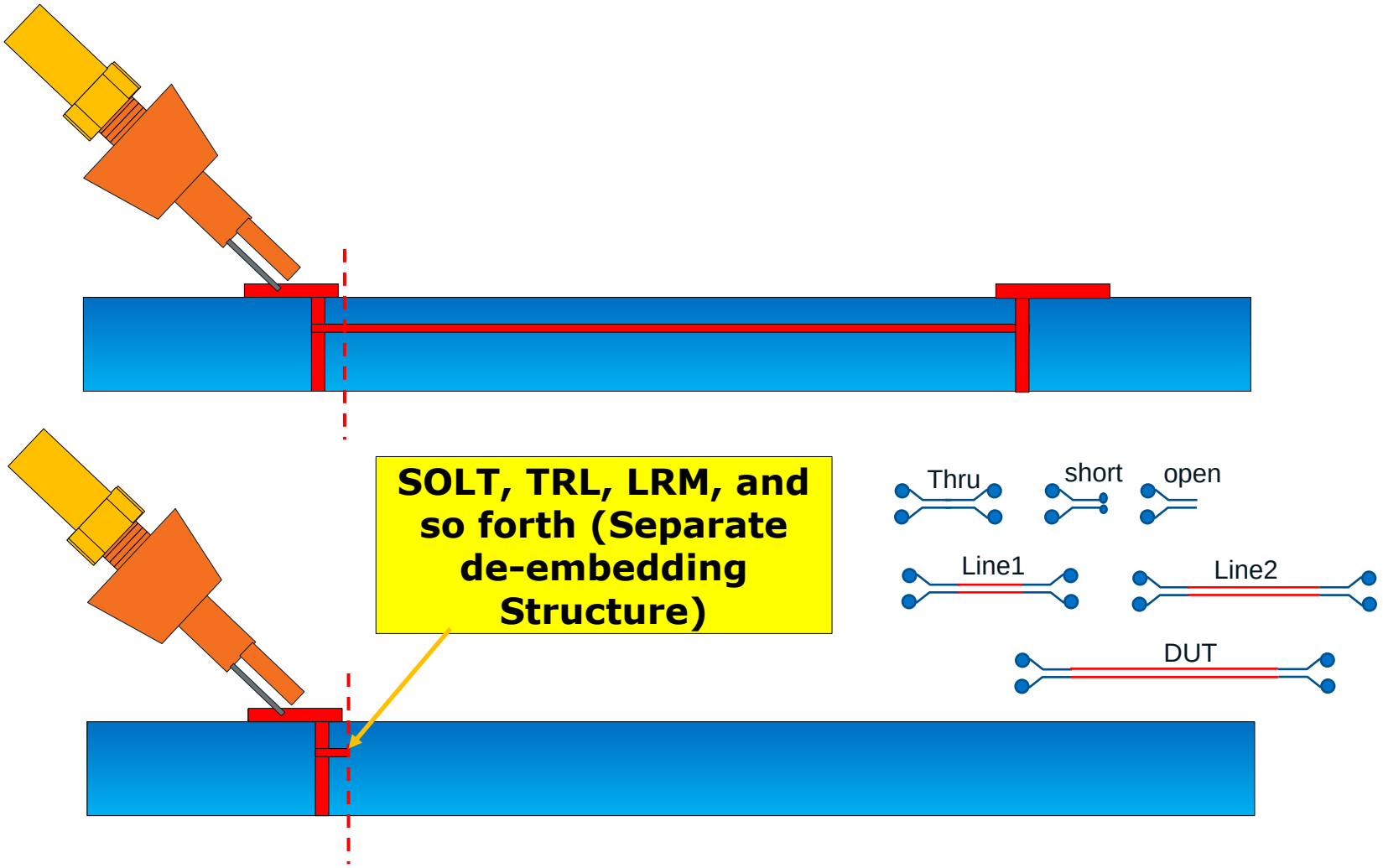


General De-embedding Approaches

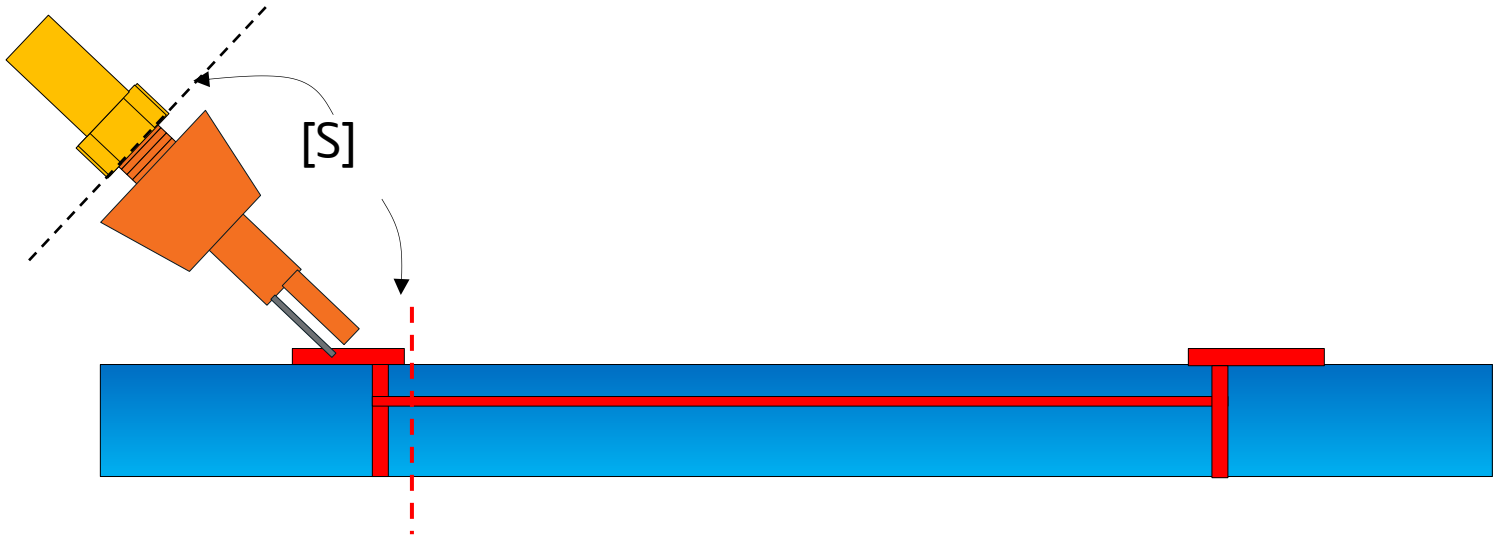
There are generally two types of approaches to remove the effects of test fixtures:

- The first approach uses specialized calibration standards that are inserted at the end of the test fixture, and performing a calibration process to move the reference plane to the end of the test fixture.
- The second approach makes direct S parameter measurements of the DUT with test fixture, meanwhile acquires the S parameter of the test fixture through either direct measurement or simulation. The S parameter of the DUT without test fixture can be mathematically calculated from above two S parameter data.

General De-embedding Approach#1



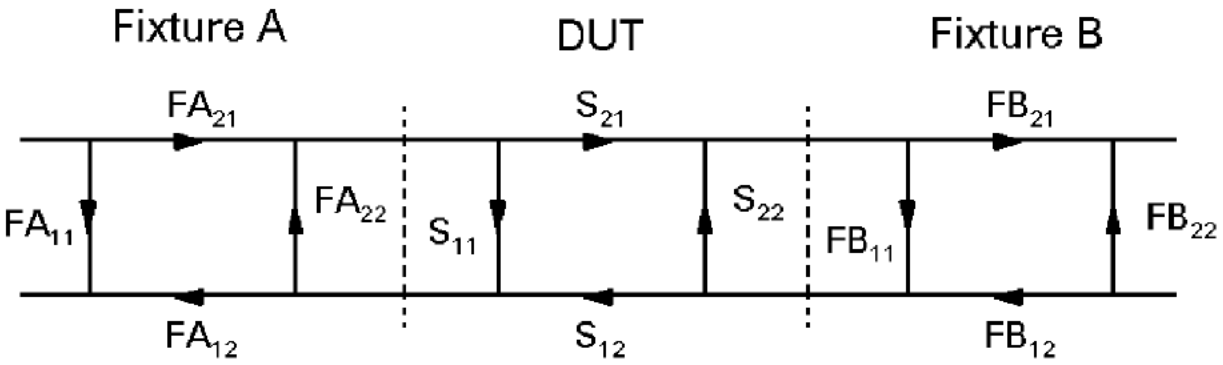
General De-embedding Approach#2



S parameter of the test fixture can be derived through:

- Measurement
- Vendor provided
- Simulation

De-embedding Basics



Convert S parameter to T matrix first

$$\left[T_A\right]^{-1}\left[T_A\right]\left[T_{DUT}\right]\left[T_B\right]\left[T_B\right]^{-1}$$

$$= \left[T_{DUT}\right]$$

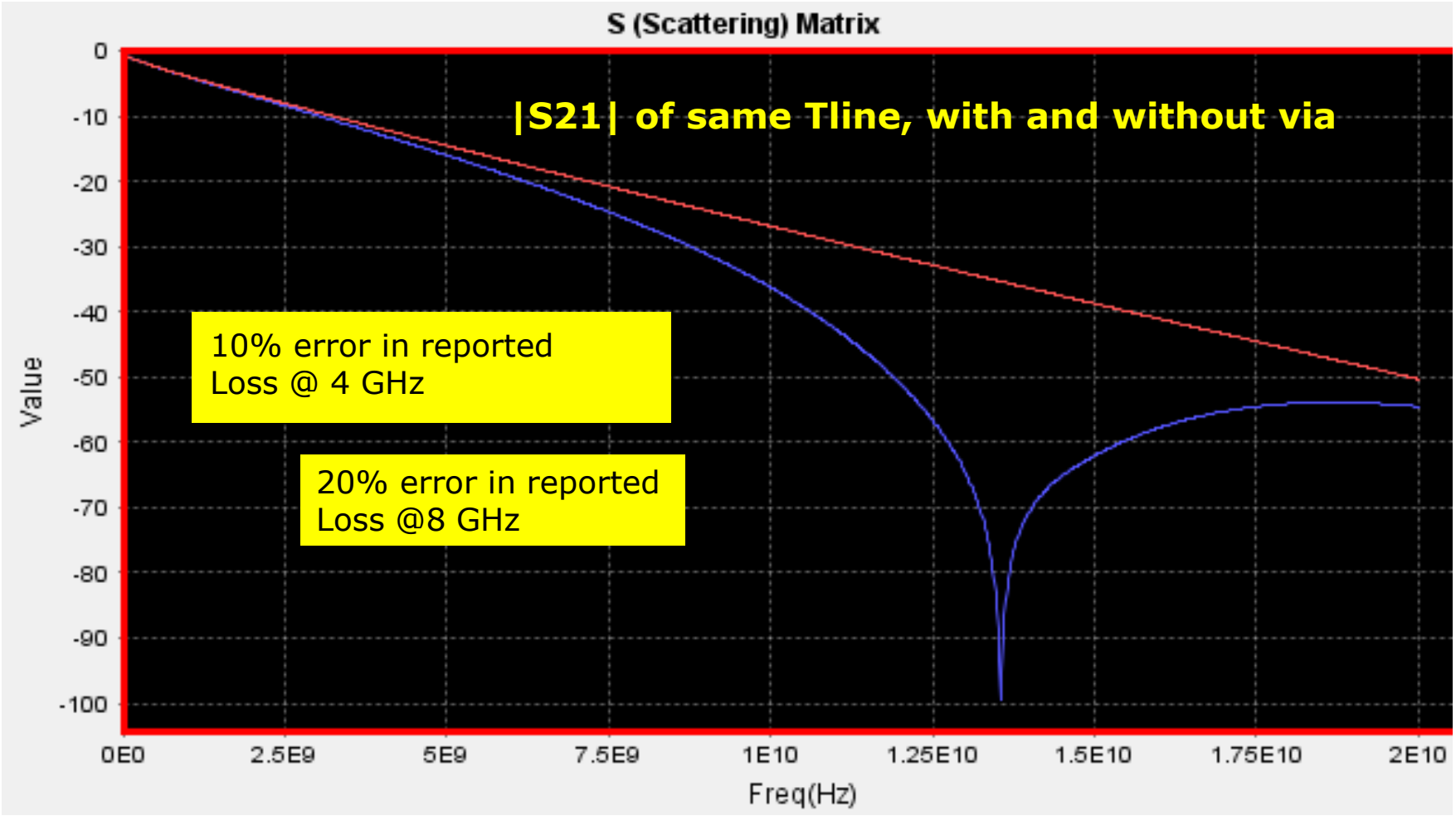
$$[T_{Measured}] = [T_L][T_{DUT}][T_R]$$

$$[T_{De-embedded}] = [T_L]^{-1}[T_{Measured}][T_R]^{-1}$$

$$= [T_L]^{-1}[T_L][T_{DUT}][T_R][T_R]^{-1} = [T_{DUT}]$$

What if NOT de-embedding?

Example:
if the via is NOT de-embedded



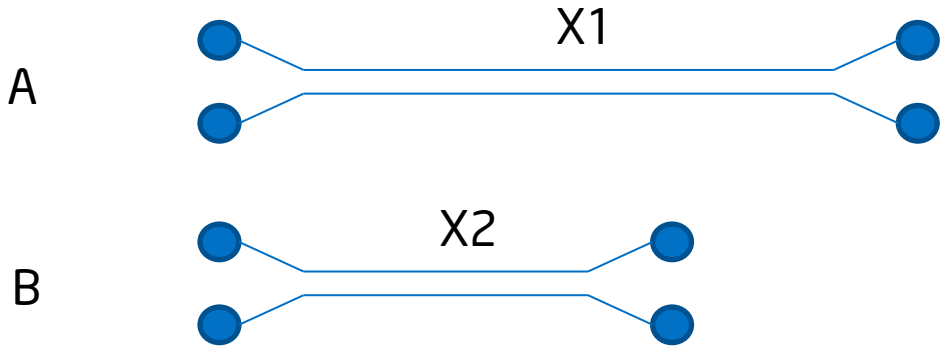
How to De-embedding the Via

- Don’t de-embed it
  - It is part of the channel you need to characterize
  - Perform simulation and measurement correlation with via included
- De-embed through simulation
  - Use simulated via model to de-embed the results

    Note: need to perform correlation to make sure via model is correct
- De-embed through de-embedding structures
  - Delta-L Methodology
  - TRL
  - AFR* (Automatic Fixture Removal), … and so forth.
- Minimize the via impact
  - Microvia
  - Backdrill, and so forth
- Others…

Delta-L Methodology

Delta-L Loss Characterization

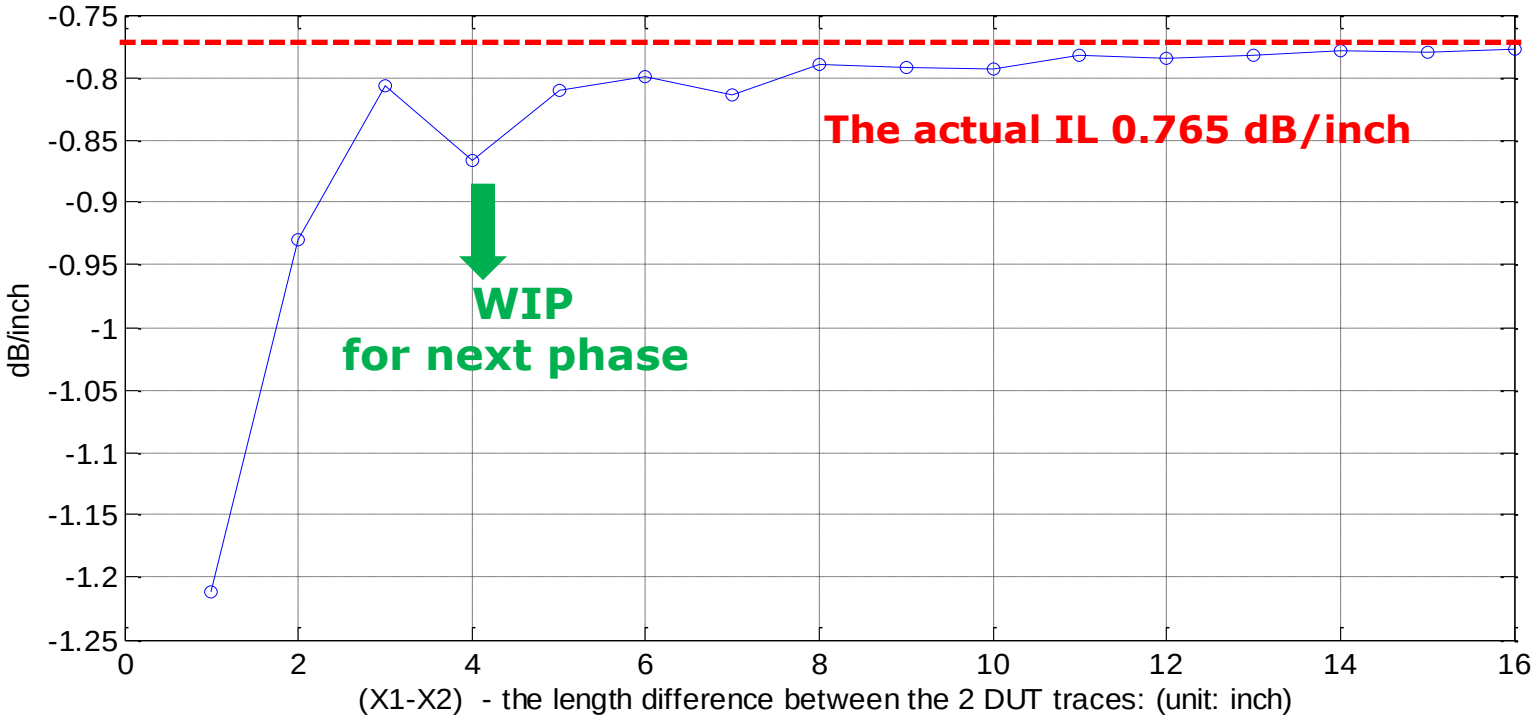


- Direct through measurement for insertion loss.
  - Insertion Loss of structure A: IL (A) --- {X1 inches + vias}
  - Insertion Loss of structure B: IL (B) --- {X2 inches + vias}
  - dB/inch loss = [IL(A) – IL(B)] / (X1 - X2)

  Note: Suggested length: X2 >= 4 inch, X1-X2 >=4 inch
- No full SOLT or TRL calibration needed;
- VNA or TDR/TDT measurement
  - If TDT/TDT measured is performed, it needs to be converted to S parameter first.

Convergence of Loss versus Delta-L

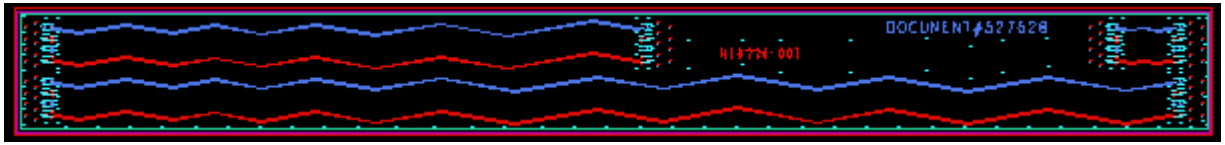
Trace length of the 1st structure (X2) = 4 inches

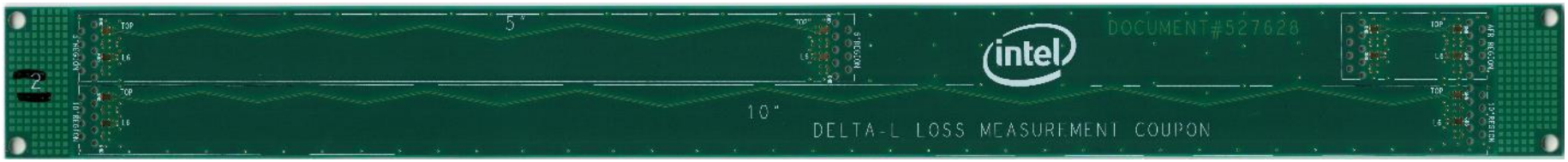


Note: This result is under a very stressed condition with 80 mils of the via stub. In the reality, it can be probed from the opposite side of the board.

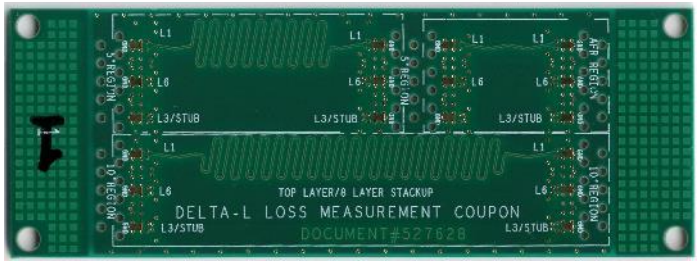
Example of Test Coupon Design

- Angle Routing



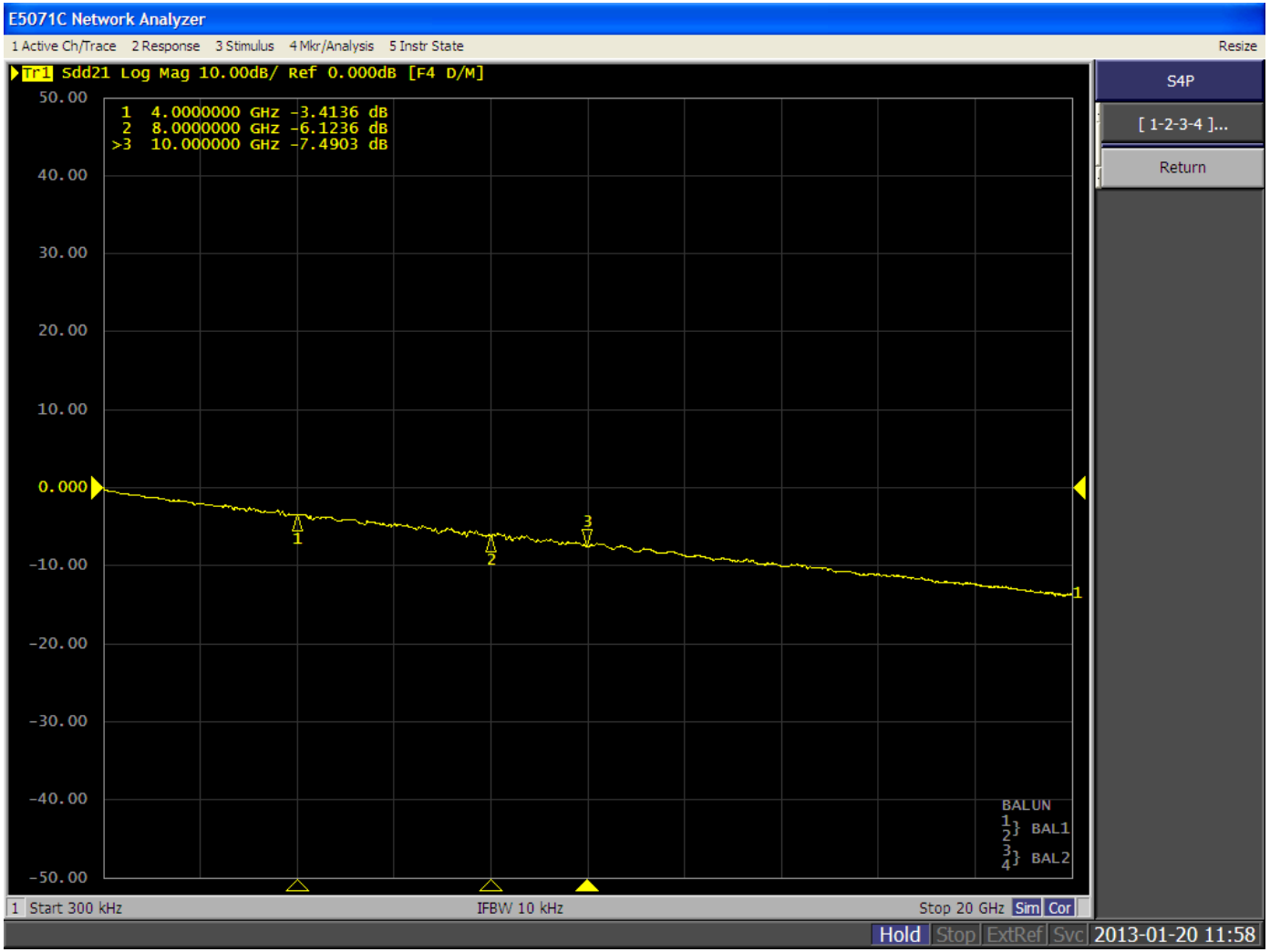


- Serpentine Design

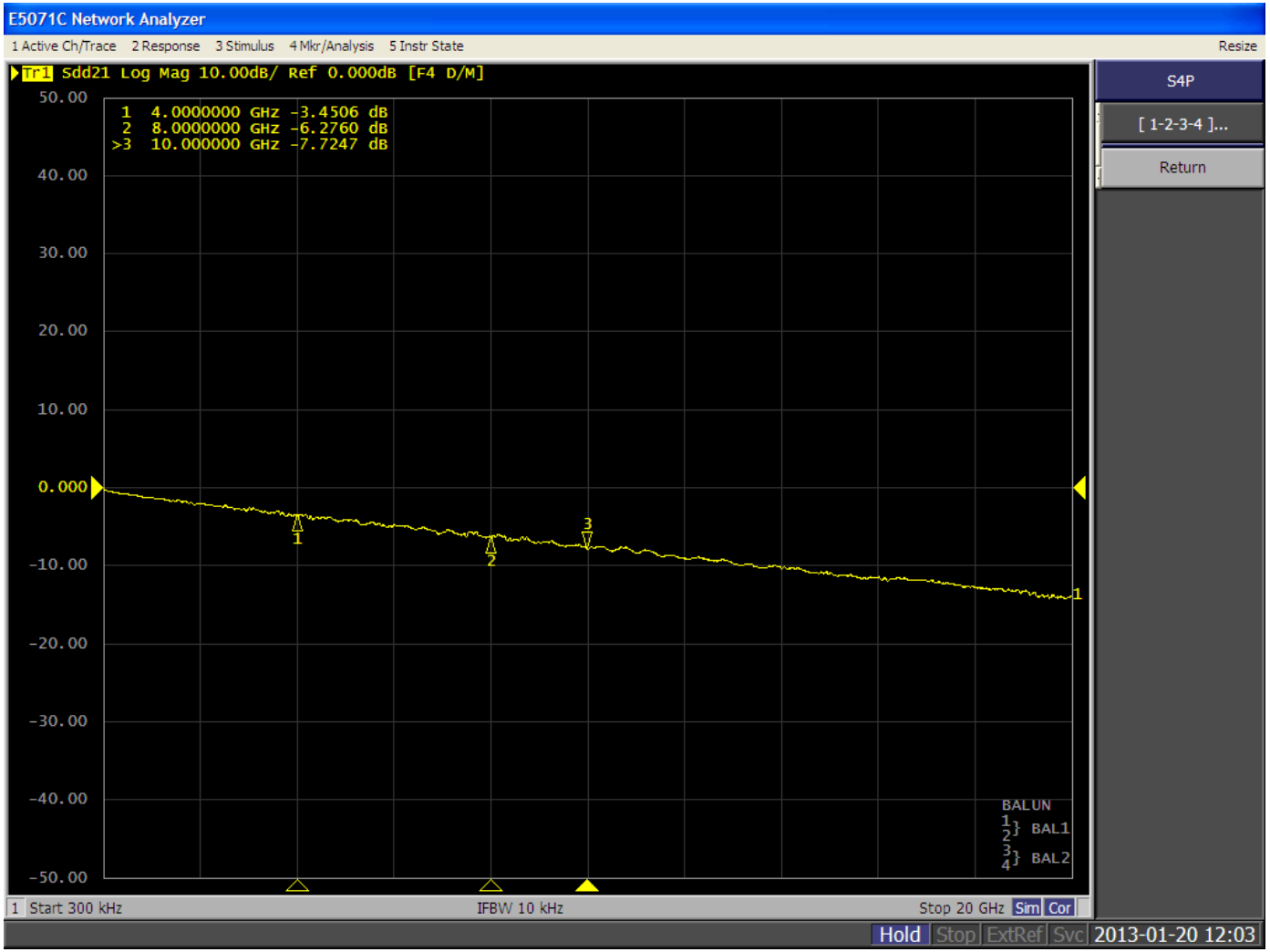


NOTICE: THESE TEST COUPON DESIGNS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

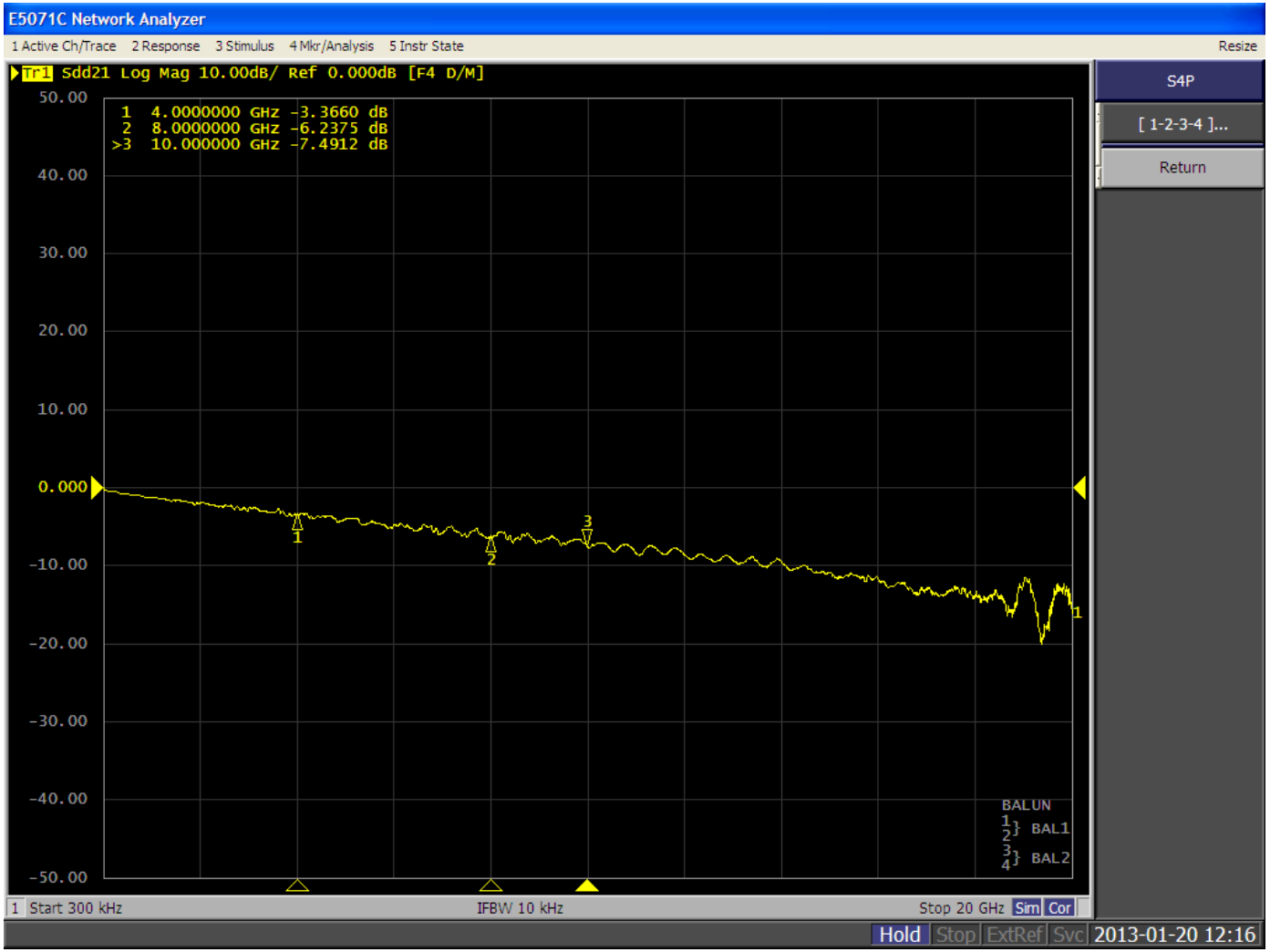
Delta-L Result in the Layer 3 (Angle Routing)



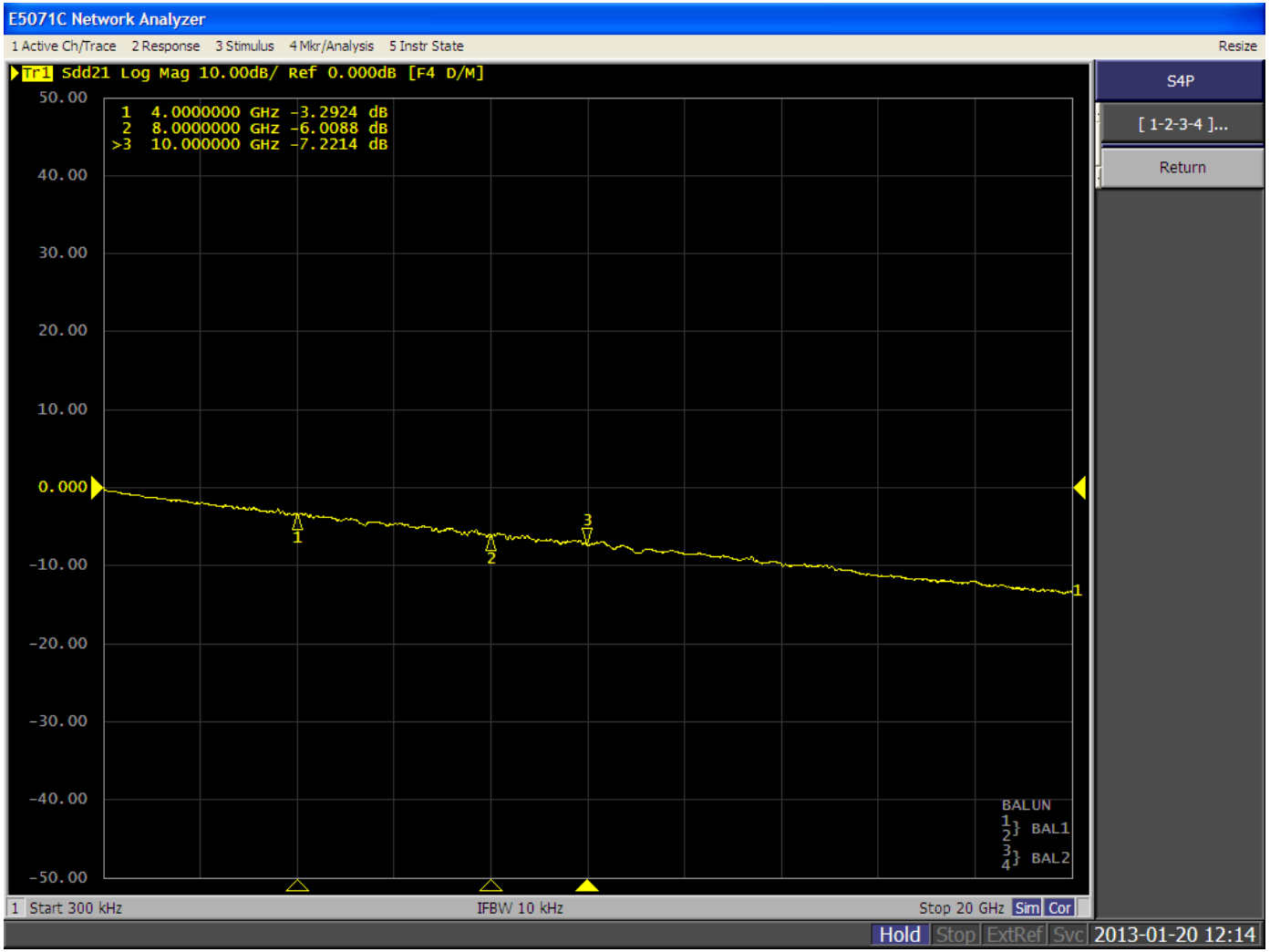
Delta-L Result in the Layer 6 (Angle Routing)



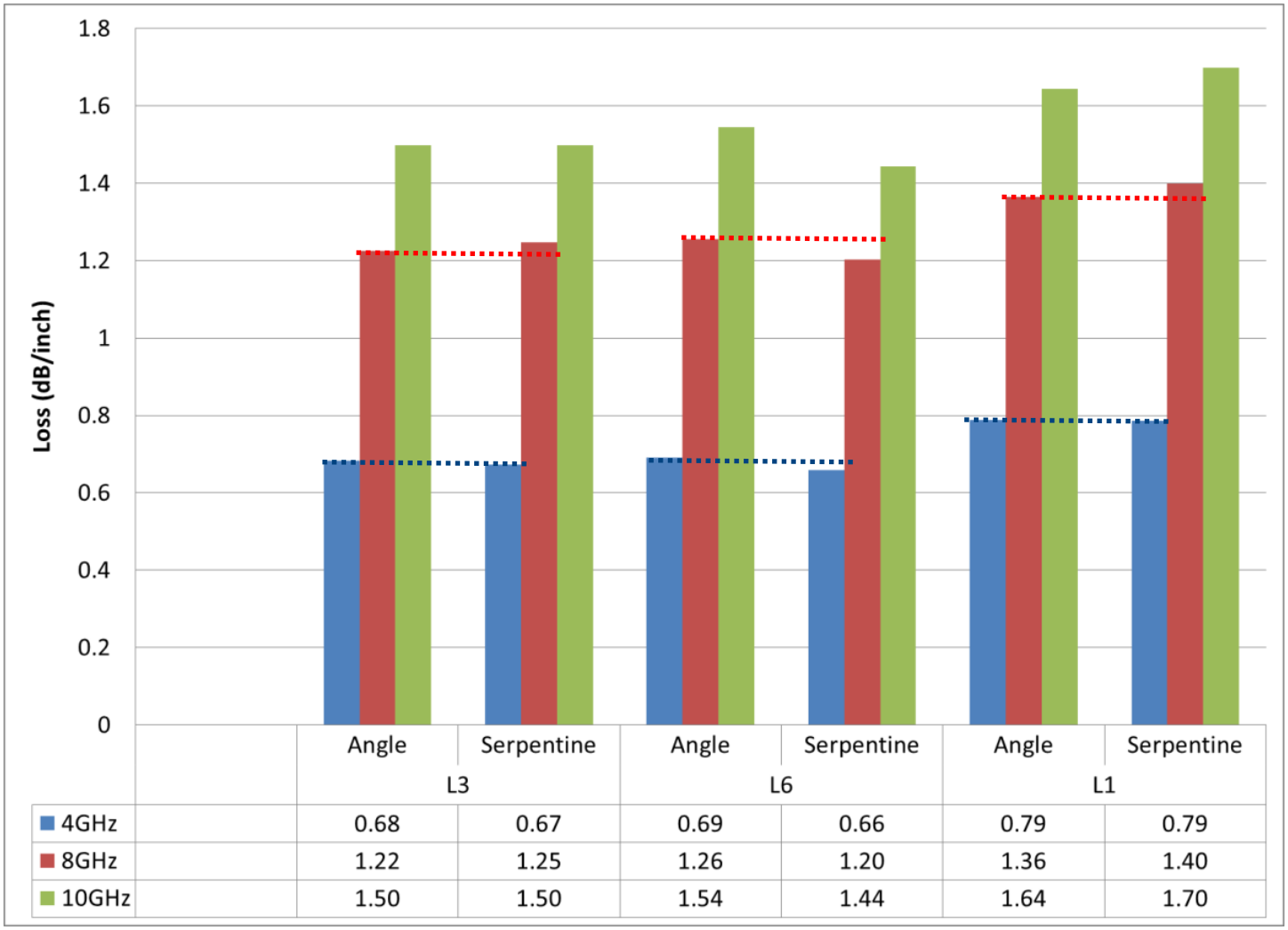
Delta-L Result in the Layer 3 (Serpentine Design)



Delta-L Result in the Layer 6 (Serpentine Design)



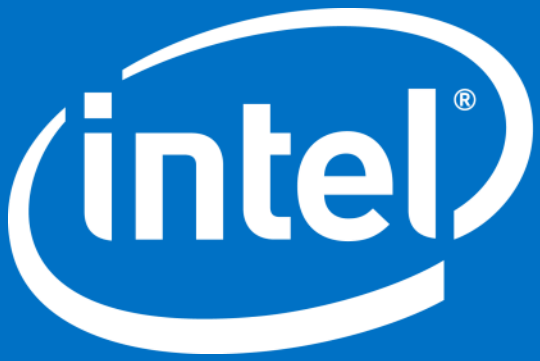
Angle Routing and Serpentine



	Angle	Serpentine	Angle	Serpentine	Angle	Serpentine
	L3		L6		L1	
4GHz	0.68	0.67	0.69	0.66	0.79	0.79
8GHz	1.22	1.25	1.26	1.20	1.36	1.40
10GHz	1.50	1.50	1.54	1.44	1.64	1.70

Summary

- De-embedding is critical for the accuracy of interconnect measurement
- If de-embedding procedure is skipped in measurement (for whatever reason)
  - Need to understand the consequence
  - Need to know the S parameter of test fixture (measurement or simulation)
- Intel Delta-L methodology is good in the electrical characterization with the de-embedding to remove the unwanted effect, such as the via


intel