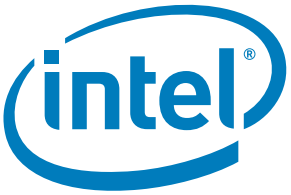

Intel® C620 Series Chipset

Thermal Mechanical Specifications and Design Guide

April 2019

Revision 003

Reference Number: 336068-003US

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Revision History

Document Number	Revision Number	Description	Date
336068	001	• Initial Release	July 2017
336068	002	• Updated Table 3-2, "Thermal Specification" with C629 Thermal Specifications	July 2018
336068	003	• Updated Table 3-2, "Thermal Specification" • Updated Table B-1, "Mechanical Drawing List" • Updated Figure B-1	April 2020

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1 Introduction

This document addresses thermal design and specifications for the Intel® C620 Series Chipset Platform Controller Hub (PCH). Information provided in this document is intended only for use with this product. Unless otherwise specified, specification and guidance provided in this document applies only to this product. In this document the term 'PCH' refers to Intel® C620 Series Chipset, unless otherwise identified.

The goals of this document are to:

- Outline the thermal and mechanical operating limits and specifications for Intel® C620 Series Chipset.
- Describe reference thermal solutions that meet the specifications of Intel® C620 Series Chipset.

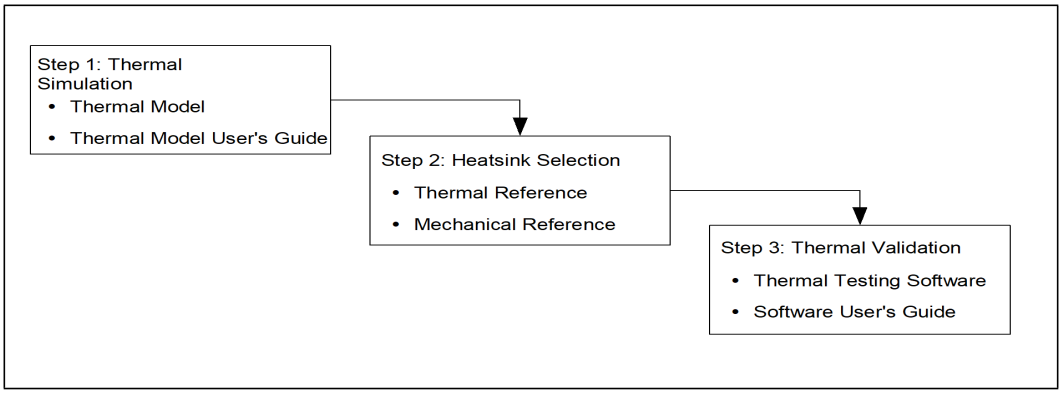
Properly designed thermal solutions provide adequate cooling to maintain the component die temperature within its thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the die to local-ambient thermal resistance. By maintaining the PCH die temperature at or below the specified limits, a system designer can ensure the proper functionality, performance, and reliability of the component. Operation outside the functional limits of the component is not supported and can cause loss of data integrity. Operation outside the damage limit can cause permanent, non-recoverable damage to the component.

The simplest and most cost-effective method to improve the inherent system cooling characteristics is through careful chassis design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heatsink can be varied to balance size and space constraints with acoustic noise.

1.1 Design Flow

To develop a reliable, cost-effective thermal solution, several tools have been provided to the system designer. The following figure illustrates the design process implicit to this document and the tools appropriate for each step.

Figure 1-1. Thermal Design Process



1.2 Definition of Terms

Table 1-1. Definition of Terms

Term	Definition
BLT	Bond Line Thickness - Final settled thickness of the thermal interface material after installation of heatsink.
DTS	Digital Thermal Sensor
FC-BGA	Flip Chip Ball Grid Array - A package type defined by a plastic substrate where a die is mounted using an underfill C4 (Controlled Collapse Chip Connection) attach style. The primary electrical interface is an array of solder balls attached to the substrate opposite the die. Note that the device arrives at the customer with solder balls attached.
MD	Metal Defined pad is one where a pad is individually etched into the PCB with a minimum width trace exiting it.
PCH	Platform Controller Hub
PECI	Platform Environment Control Interface (PECI) - One-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices.
T_{CASE_MAX}	Maximum die operating temperature, as measured at the geometric center of the package substrate at top of the IHS.
T_{CASE_MIN}	Minimum die operating temperature, as measured at the geometric center of the package substrate at top of the IHS.
TIM	Thermal Interface Material - A thermally conductive material used between the components and heatsink to improve thermal conduction.
TDP	Thermal Design Power - Thermal solutions should be designed to dissipate this target power level. TDP is not the maximum power that the chipset can dissipate.
T_{SENSOR}	Die temperature as reported by the device DTS.

1.3 Reference Documents

The reader of this specification should also be familiar with material and concepts presented in the following documents:

Table 1-2. Reference Documents

Title	Document Number	Notes
Intel® Xeon® Processor Scalable Family Datasheet: Volume 1 - Electrical	336062	
Intel® Xeon® Processor Scalable Family Datasheet: Volume 2 - Registers	336063	

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2 Packaging Technology

Intel® C620 Series Chipset is a surface mounted FCBGA15 package with a total of 1310 lead-free solder balls. PCH package substrate is 34 mm x 28 mm with an Integrated Heat Spreader (IHS) of 30.4 x 24.4 mm. See Appendix B for the package detailed drawing.

Solder Ball Grid Regions:

- Die Area: Uniform solder ball pitch
- Die Parameter: Staggered solder ball pitch
- Package Edges: Condensed staggered solder ball pitch
- Package Corners: Staggered solder ball pitch.

Additional package attributes can be found in the package mechanical drawing.

2.1 Package Mechanical Specifications

The PCH package mechanical load limits must not be exceeded during heatsink installation, mechanical stress testing, standard shipping conditions, and/or any other use condition.

Table 2-1. Package Mechanical Load Specifications

Parameter	Value	Notes
Maximum Allowable Static Normal Load	062 mil PCB thickness: 111 N [25 lbf] >093 mil PCB thickness: 156 N [35 lbf]	1, 2, 3
Maximum Transient Compressive Package Load	See Board Flexure Initiative (BFI) Strain	2, 3
Maximum Dynamic Compressive Package Load	See Q Strain Metric Guidance for Shock	

Notes:
1. The heatsink attach solutions must not include continuous stress onto the package with the exception of a uniform load to maintain the heatsink-to-package thermal interface.
2. These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
3. These specifications are based on limited testing for design characterization. Loading limits are for the package only.

2.2 Non-critical to Function Solder Joints

Several selected solder joints of the PCH are defined as non-critical to function (NCTF) when evaluating package solder joints post environmental testing. The PCH signals at NCTF locations are typically redundant ground or non-critical reserved pins, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality. See Section 6.1, "Land Pattern Guidance" for additional information on PCB land pattern recommendation.

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3 Thermal Specifications

This section lists the thermal specifications of the platform controller hub. Systems should be designed to meet the PCH maximum continuous power dissipation as defined in this section.

3.1 Thermal Design Power

Analysis indicates that real applications are unlikely to cause the component to consume maximum power dissipation for sustained time periods. Therefore, in order to arrive at a more realistic power level for thermal design purposes, Intel® characterizes power consumption based on known platform benchmark applications. The resulting power consumption is referred to as the Thermal Design Power (TDP). Hence, TDP is the design target for the thermal solution. TDP is not the maximum power that the PCH can dissipate.

FC-BGA packages have poor heat transfer capability into the board and have minimal thermal capability without a thermal solution. Intel recommends that system designers plan for a heatsink when using Intel® C620 Series Chipset.

3.2 Case Temperature

T_{CASE_MAX} is provided for the purpose of designing the PCH thermal solution. Refer to "Thermal Metrology," section for guidelines on accurately measuring package case temperature. Maintaining the PCH case temperature at or below the T_{CASE_MAX} ensures the component is operating within its functional limits.

3.3 Die Temperature

To ensure proper operation and reliability of the platform controller hub, die temperature must be kept within its thermal specifications. System and/or component level thermal solutions are required to maintain these temperature specifications.

3.3.1 Thermal Sensor

The PCH uses a thermal sensing device on the die to monitor its temperature status in real-time. The thermal sensor output, T_{SENSOR} is in degrees Celsius, and is available over PECI through the Intel® Management Engine (Intel® ME). This enables system thermal management to monitor and to implement policies such as fan speed control to maintain the die temperature within its operation and reliability temperatures. Die temperature is also compared with the PCH thermal trip set point. Platform compatible processors will monitor the PCH temperature via integrated iMC on the processor (host). The PCH is at its maximum operating temperature when TEMP_MID setpoint is reached. The PCH thermal thresholds on the processor enable the processor to implement policies in response to the changes in the die temperature.

3.3.2 Thermal Thresholds

The PCH thermal set points are programmed in the host controller. If enabled, the host upon reaching these thermal conditions will initiate throttling resulting in reduction of traffic through the PCH and hence reduction in its power.

TEMP_MID: Is a T_{SENSOR} based setpoint. Die temperature shall not exceed this setpoint while under any load to ensure functionality when using the sensor-based limiting specification. TEMP_MID is programmed in the processor at boot time. Additional margin, meaning lower than specified TEMP_MID value, can be programed if so desired in reducing occurrence of throttling caused by exceeding PCH thermal specifications.

TEMP_HI: Is a T_{SENSOR} based setpoint. Die temperature shall not exceed this setpoint while under any load to prevent damage to the component. TEMP_HI is programmed in the processor at boot time. Additional margin, meaning lower than specified TEMP_HI but greater than TEMP_MID value, can be programed to prevent damage to the component which may result from operating at higher temperature.

Table 3-1. Thermal Thresholds

Thresholds	Description	Action
TEMP_MID	T_{SENSOR} approaching functional limit	See Intel® C620 Series Chipset Datasheet
TEMP_HI	T_{SENSOR} approaching damage limit	See Intel® C620 Series Chipset Datasheet

Note: PCHHOT# is configured and asserted with either (TEMP_MID or TEMP_HI) threshold crossing.

3.3.3 $T_{CONTROL}$

$T_{CONTROL}$ is the temperature limit which must be maintained to ensure the component operates reliably over its expected life. $T_{CONTROL}$ is a thermal monitoring set point which is specified based on the thermal sensor output in degrees Celsius. Its value must be compared against the thermal sensor reading. The value of the $T_{CONTROL}$ threshold is specified in the PCH thermal specification table. $T_{CONTROL}$ value applies to the full range of the PCH operating power. Note that no internal response is generated by the PCH at $T_{CONTROL}$. Long term operation above the $T_{CONTROL}$ temperature set point reduces the life of the product.

A server thermal management controller can monitor the PCH temperature, and use the $T_{CONTROL}$ value as the threshold at which active system thermal management can be engaged. This will ensure reliable PCH operation over its expected life. In cases where maximum fan speed is reached and T_{SENSOR} cannot be maintained at or below the $T_{CONTROL}$ value, the T_{SENSOR} must still be maintained to be less than or equal to TEMP_MID if the thermal sensor specification is applied.

3.3.4 Thermal Trip

Once the thermal sensing device observes that the temperature of the die, T_{SENSOR}, has reached it catastrophic limit, the PCH will initiate shutdown. See 'Catastrophic Overtemp' error condition described in the Intel® C620 Series Chipset Datasheet.

3.3.5 Thermal Monitoring and Response

When:

- $T_{SENSOR}<T_{CONTROL}$, the system can run under any desired conditions.
- $T_{SENSOR}=T_{CONTROL}$, $T_{CONTROL}$ limit attained, system must increase fan speed until $T_{CONTROL}$ limit can no longer be maintained.
- $T_{SENSOR}>T_{CONTROL}$, fan speed increase is required to maintain T_{CASE} below T_{CASE_MAX} or the T_{SENSOR} to remain below TEMP_MID.
- T_{SENSOR}=TEMP_MID, PCH will issue PCHHOT#.

- T_{SENSOR}=TEMP_HI, PCH will transition the system to S5 state unconditionally.

3.3.6 Thermal Registers

Intel® C620 Series Chipset thermal registers have another name in the Datasheet. In order to make sure the same references are used when comparing the Datasheet to the TMDG, below is corresponding thermal registers for Intel® C620 Series Chipset thermal set points. Please refer to Intel® C620 Series Chipset Datasheet for details on the thermal registers.

— Catastrophic trip point = TEMP_HI

— Thermal Alert High = TEMP_MID

— Thermal Alert Low = Tcontrol

3.4 Thermal Specifications

Table 3-2. Thermal Specification

Parameter		C621	C622	C624	C625	C626	C627 / C629		C628		Notes
							120 Gbps Application[8]	High Performance Application[9]	120 Gbps Application[8]	High Performance Application[9]	
TDP (W)		15	17	19	21	23	26.6	28.6	24.3	26.3	1, 3, 4
TEMP_HI (°C)		107	106	105	106	106	106	106	106	106	2, 3, 4, 6
TEMP_MID (°C)		87	86	85	86	86	92	91	92	91	2, 3, 4, 6
$T_{CONTROL}$ (°C) [Sensor Based]	7 yrs	77	76	75	76	76	82	81	82	82	4, 6
	10 yrs	67	66	65	66	66	72	71	72	71	4, 6
$T_{CASE\_MAX@TDP}$ (°C)		86	86	85	86	86	88	87	89	87	4, 5
T_{CASE_MIN} (°C)		5	5	5	5	5	5	5	5	5	
	10 yrs	66	66	65	66	66	68	67	69	67	4, 5, 7

Notes:
1. TDP value for each SKU is based on SKU features
2. Refer to the PCH Datasheet document for thermal management mechanism
3. Temperature value is based on thermal sensor output.
4. These specifications are based on preliminary measurement and subject to change.
5. Use T_{CASE} for heatsink sizing
6. Use temperature sensor output in maintain die temperature within its specifications
7. Where temperature sensor is not used to monitor die temperature, maintaining PCH T_{CASE} at $T_{CONTROL}$ (T_{CASE} based) ensures compliance with product rel requirements.
8. x16 PCIe3 uplink, 100 kops PKE/100Gbps crypto/100Gbps compression, 120 Gbps max concurrent
9. x24 PCIe3 uplink, 100kops PKE/>100 Gbps crypto/100Gbps compression, >120Gbps max concurrent

Dual thermal specifications based on T_{CASE} and Digital Thermal Sensor enables the thermal solution designer to optimize the component thermal solution and the system thermal management in a way that is best suited for the integration of the PCH thermal management. Systems not utilizing thermal threshold must ensure compliance with T_{CASE} specifications. Equation below provides a conversion between T_{SENSOR} and T_{CASE} at the PCH maximum operating temperature.

T_{SENSOR} = (T_{CASE} ± 7) at T_{CASE} ranges of 65°C to Tcase_max @ TDP

3.5 Storage Specifications

The following table includes a list of the specifications for device storage in terms of maximum and minimum temperatures and relative humidity.These conditions should not be exceeded in storage or transportation.

Table 3-3. Storage Conditions

Parameter	Description	Min	Max	Notes
$T_{absolute\ storage}$	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to for any length of time.	-25 °C	125 °C	1, 2, 3
$T_{sustained\ storage}$	The ambient storage temperature limit (in shipping media) for a sustained period of time.	-5 °C	40 °C	4, 5
$RH_{sustained\ storage}$	The maximum device storage relative humidity for a sustained period of time.	60% @24 °C		5, 6
$TIME_{sustained\ storage}$	A prolonged or extended period of time; typically associated with customer shelf life.	0 Months	6 Months	6

Notes:
1. Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals.
2. Specified temperatures are based on data collected. Exceptions for surface mount reflow are specified in by applicable JEDEC standard and MAS document. Non-adherence may affect component reliability.
3. $T_{absolute}$ storage applies to the unassembled component only and does not apply to the shipping media, moisture barrier bags or desiccant.
4. Intel® branded board products are certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40 °C to 70 °C & Humidity: 50% to 90%, non-condensing with a maximum wet bulb of 28 °C). Post board attach storage temperature limits are not specified for non-Intel® branded boards.
5. The JEDEC, J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
6. Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by $T_{sustained}$ and customer shelf life in applicable Intel® box and bags.

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4 Thermal Metrology

The system designer must make temperature measurements to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques to measure the component die temperatures. This section of the document provides guidelines on how to accurately measure the component die temperatures.

4.1 Case Temperature Measurements

To ensure functionality and reliability, the chipset component T_{CASE} must be maintained at or between the maximum/minimum operating range of the temperature specification. The surface temperature at the geometric center of the die corresponds to T_{CASE}. Measuring T_{CASE} requires special care to ensure an accurate temperature measurement.

Temperature differences between the temperature of a surface and the surrounding local ambient air can introduce errors in the measurements. The measurement errors could be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, and/or contact between the thermocouple cement and the heatsink base (if a heatsink is used). For maximum measurement accuracy, only the 0° thermocouple attach approach is recommended.

Figure 4-1. Zero Degree Angle Attach Methodology (Top View)

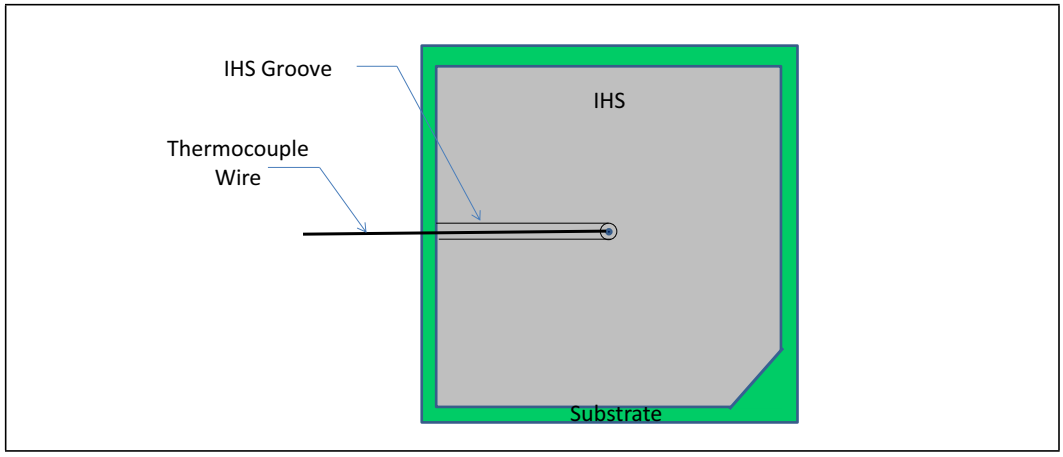
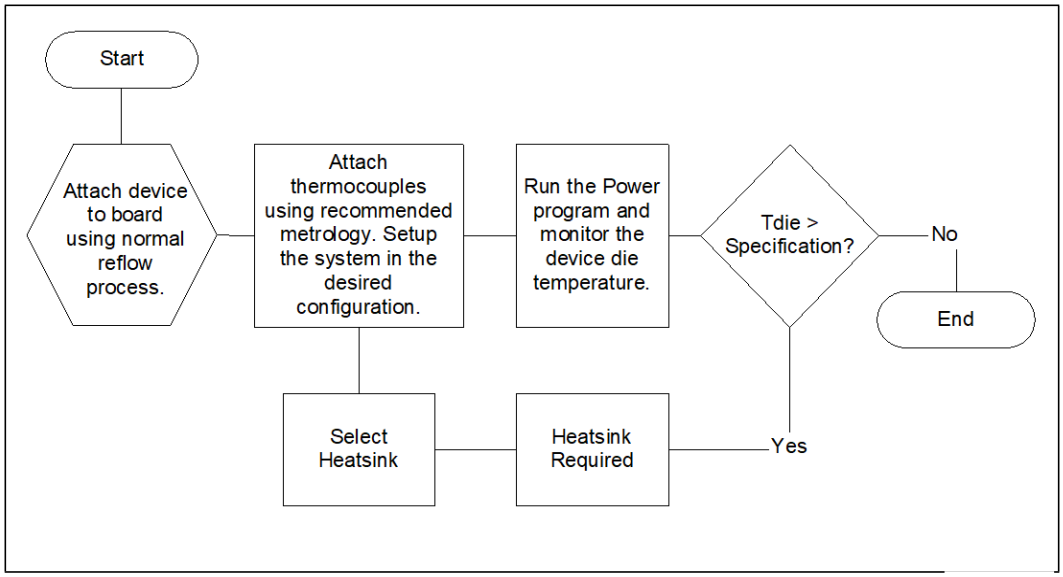


Figure 4-2. Thermal Solution Decision Flowchart



4.2 Thermal Solution Performance Characterization

The case-to-local ambient Thermal Characterization Parameter (Ψ_{CA}) is defined by:

Equation 4-1. $\Psi_{CA} = (T_{CASE} - T_{LA}) / TDP$

Where:

- T_{CASE} = PCH case temperature (°C).
- T_{LA} = Local ambient temperature in chassis at PCH (°C).
- **TDP** = TDP (W) assumes all power dissipates through the integrated heat spreader. This inexact assumption is convenient for heatsink design.

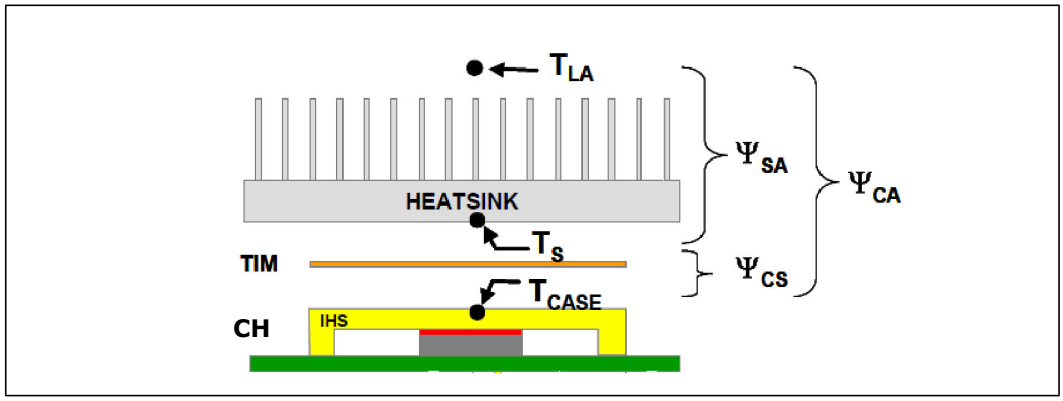
Equation 4-2. $\Psi_{CA} = \Psi_{CS} + \Psi_{SA}$

Where:

- Ψ_{CS} = Thermal characterization parameter of the TIM (°C/W) is dependent on the thermal conductivity and thickness of the TIM.
- Ψ_{SA} = Thermal characterization parameter from heatsink-to-local ambient (°C/W) is dependent on the thermal conductivity and geometry of the heatsink and dependent on the air velocity through the heatsink fins.

Figure 4-3 illustrates the thermal characterization parameters.

Figure 4-3. Processor Thermal Characterization Parameter Relationships



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5 Design Considerations

When designing a thermally capable system, all critical components must be simultaneously considered. The responsible engineer must determine how each component will affect another, while ensuring target performance for all components. The system design team must set these target performance goals during the design phase so that they can be achieved with the selected component layout.

The location of components and their interaction must be considered during the layout phase. A poorly cooled device will have worse performance. The thermal engineer's responsibility is to ensure that each and every component meets its performance goals bounded by thermal and acoustic specifications but also to determine optimum system configuration.

To develop a reliable and cost-effective thermal solution, thermal characterization and simulation should be carried out at the entire system level, accounting for the thermal requirements of each component. In addition, acoustic noise constraints may limit the size, number, placement, and types of air-movers that can be used in a particular design.

5.1 Operating Environment

The reference thermal solution design assumes both a max fan speed condition and an acoustic fan speed condition. The thermal designer must carefully select the location to measure airflow to obtain an accurate estimate.

5.2 Altitude Correction

Simulated performance of a thermal solution will change by varying approach air velocity. For data that is modeled at sea level a correction factor would be required to estimate thermal performance at a different altitudes. Equation 5-1 can be used to determine the heatsink performance based on the adjusted altitude.

Equation 5-1.Altitude Correction

$$\theta_{ca} = \alpha + \beta \times Q_{alt}^{-\Upsilon\left(\frac{\rho_{alt}}{\rho_o}\right)^{-\Upsilon}}$$

α, β and γ can be obtained from the heatsink thermal performance curve versus the approach air velocity.

Q - "velocity through heatsink fin area (m/s)". Velocity is the value on X axis of the heatsink thermal performance curve versus the approach air velocity.

ρ_{alt} - Air density at given altitude

ρ_0 - Air density at sea level

5.3 Effect of Pressure on TIM Performance

As mechanical pressure increases on the TIM, the thermal resistance of the TIM decreases. This phenomenon is due to the decrease of the bond line thickness (BLT). BLT is the final settled thickness of the thermal interface material after installation of the heatsink. The effect of pressure on the thermal resistance of the Honeywell PCM45 F* TIM is shown in Table 5-1. Intel provides both End of Line and End of Life TIM thermal resistance values for Honeywell PCM45 F*.

End of Line and End of Life TIM thermal resistance values are obtained through measurement on a Test Vehicle similar to the component's physical attributes using an extruded aluminum heatsink. The End of Line value represents the TIM performance post heatsink assembly while the End of Life value is the predicted TIM performance when the product and TIM reaches its end of life. The heatsink retention provides enough pressure for the TIM to achieve an End of Line thermal resistance.

Table 5-1. Honeywell PCM45 F* TIM Performance as a Function of Attach Pressure

Pressure on Thermal solution and package interface (PSI)	Thermal Resistance (°C × cm^2)/W
	End of Life
4.35	0.187

5.4 Board-Level Components Keepout Dimensions

The location of hole patterns and keepout zones for the reference thermal solution are shown in Figure B-3. Note that additional keep-out may be necessary to address board assembly and rework process tool requirements.

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6 PCB Design Considerations

6.1 Land Pattern Guidance

Recommendation for Printed Circuit Board (PCB) Land Patterns is to ensure solder joint reliability during dynamic stresses, often encountered during shipping and handling and hence to increase package reliability. For specific product land pattern specification refer to Intel product thermal/mechanical specifications and design guide or the related Intel product Manufacturing Advantage Services collateral.

6.2 Pad Type Recommendations

Intel defines two types of pad types based on how they are constructed. A metal defined (MD) pad is one where a pad is individually etched into the PCB with a minimum width trace exiting it. The solder mask defined (SMD) pad is typically a pad in a flood plane where the solder mask opening defines the pad size for soldering to the component.

In thermal cycling a MD pad has shown to be more robust than a SMD pad type. The solder mask that defines the SMD pad can create a sharp edge on the solder joint as the solder ball / paste conforms to the window created by the solder mask.

For certain failure modes the MD pad may not be as robust in shock and vibration (S&V). During S&V, the predominant failure mode for a MD pad in the corner of the BGA layout is pad craters and solder joint cracks. A corner MD pad can be made more robust and behave like a SMD pad by having a wide trace enter the pad. This trace should be 10 mil minimum but not to exceed the pad diameter and exit the pad at a 45 degree angle (parallel to the diagonal of the package). During board flexure that results from shock & vibration a SMD pad is less susceptible to a crack initiating due to the larger surface area.

MD: Metal Defined (traditional trace Via to BGA-Pad

- I/O Driven, typical 5 mil trace because of impedance matching.
- *No Connect* is a metal pad with no trace connected.

WTMD: *Wide Trace Metal Defined* (trace is equal to or less than the pad diameter)

- xWTMD >> 1WTMD = 1 Wide Trace, 2WTMD = 2 wide Traces
- Multiple “Wide Traces”, can look or behave as a Spoke design

SMD: **Solder Mask Defined** (100%, flood copper and/or larger metal pad)

Note: MD pad type is preferred for T/C performance. SMD preferred for shock performance.

Figure 6-1. Pad Definition

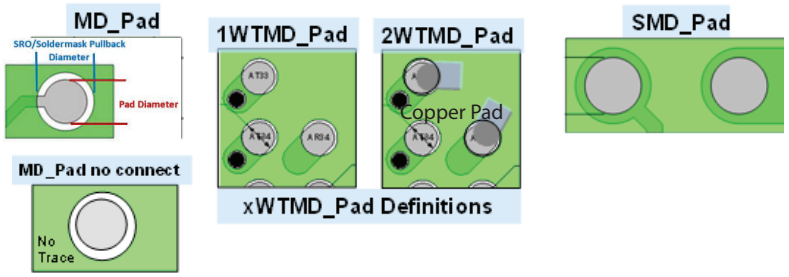


Figure 6-2. 1310 FCBGA15 Land Pattern Guidance

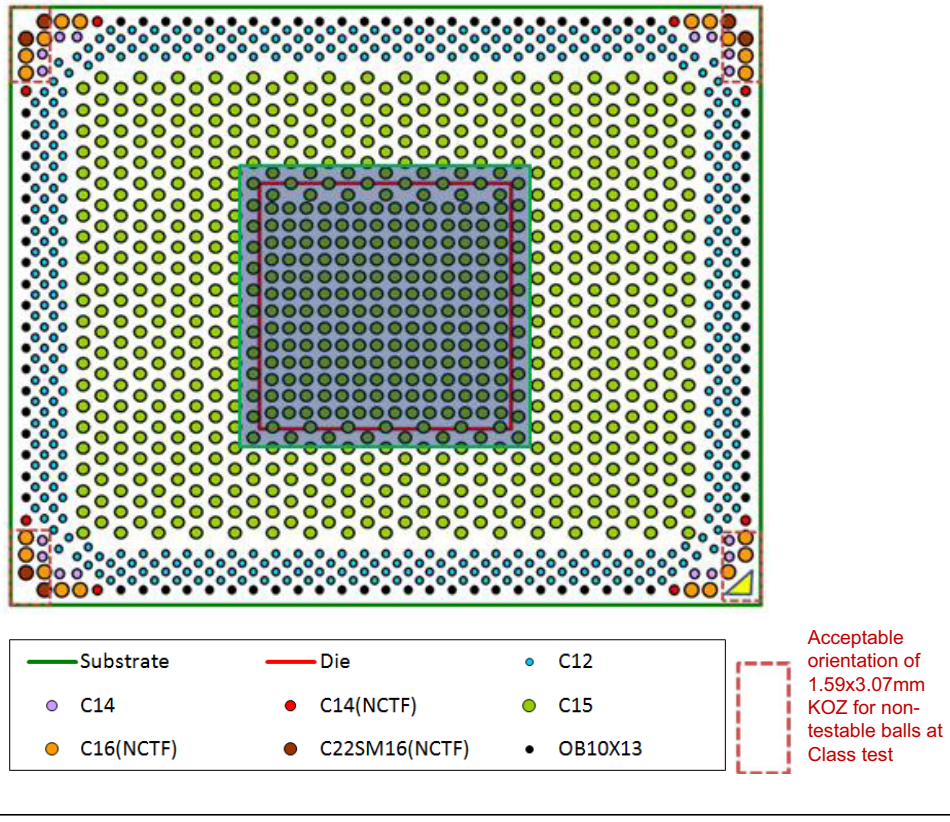
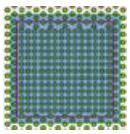


Table 6-1. Land Pattern Notes

Symbol	Count	Pad Type	Diameter	Comments
	Qty 6	SMD	558.8 µm (22 mil) pad, 406.4 µm (16 mil) SRO 254 µm (10mil) traces 45° outward from die center	nCTF
	Qty 20	MD	406.4 µm (16 mil) pad, 508 µm (20 mil) SRO Where possible 254 µm (10mil) traces 45° outward from die center	nCTF
	Qty 8	MD	355.6 µm (14 mil) pad, 457.2 µm (18 mil) SRO	nCTF
	Qty 16	MD	355.6 µm (14 mil) pad, 457.2 µm (18 mil) SRO	CTF
	Qty 88	MD / SMD	MD/SMD 254 x 342.9 µm (10 x 13 mil) Oblong Pads Long axis perpendicular to closest pkg edge 355.6 x 431.8 µm (14 x 17 mil) SRO	CTF
	Qty 400	MD / SMD	MD/SMD304.8 µm (12 mil) pad, 406.4 µm (16 mil) SRO	CTF
	Qty 772	MD / SMD	MD/SMD381 µm (15 mil) pad, 482.6 µm (19 mil) SRO	CTF
		N/A	All pins inside the dotted box are non-testable during package e- test.	Any
		MD / Spoke Pads Only	The area shaded in gray (under Die Shadow Area should be MD or Spoke Pad). Cannot be SMD due to TC risk (entire die interior and 1 row outside die edge). Use 1WTMD or spoked pads in this area. For Die shadow: Because this LP covers Intel® Atom Processor C3000 Product Family, Intel C624 PCH and C626, refer to the package specification to define the "Die Shadow" region.	Only MD / Spoke Pads

6.3 Strain Guidance

Intel provides manufacturing strain guidance commonly referred to as Board Flexure Initiative or BFI Strain Guidance. The BFI strain guidance apply only to transient bend conditions seen in board manufacturing assembly environment. It should be noted that any strain metrology is sensitive to boundary conditions.

Intel recommends the use of BFI to prevent solder joint defects. For additional guidance on BFI, see *Manufacturing With Intel® Components - Strain Measurement for Circuit Board Assembly*, also referred to as BFI MAS (Manufacturing Advantage Services) and BFI STRAIN GUIDANCE SHEET (1310-FCBGA). Consult your Intel Customer Quality Engineer for additional guidance in setting up a BFI program in your facility.

6.4 Board Deflection

Exceeding the maximum Board Deflection may result in solder joint failure. Board deflection under the package can be kept to an acceptable level by adhering to the maximum load values.

Method by which the PCB is supported with the chassis will have an impact on board deflection and resultant package solder ball stress. Customers need to assess shock for their designs as their heatsink retention, heatsink mass, and the PCB attachment mechanism may vary.

Designs that exceed the maximum Heatsink Static Compressive Load, should follow Board Deflection Measurement Methodology as outlined to assess risk to package solder joint reliability.

6.5 Reliability Guidelines

Each motherboard, heatsink and attach combination may vary the mechanical loading of the component. Based on the end user environment, the user should define the appropriate reliability test criteria and carefully evaluate the completed assembly prior to use in high volume. The reference solution is to be mounted to a fully configured system. Some general recommendations are shown in Table 6-2.

Table 6-2. Reliability Guidelines

Test[1]	Objective	Inspection Guidelines[2]
Mechanical Shock	50g, board level, 10 msec, 3 shocks/axis	Visual Check and Electrical Functional Test
Random Vibration	3.13g, board level, 10 min/axis, 20 Hz to 500 Hz	Visual Check and Electrical Functional Test
Temperature Life	85°C, 2000 hours total, check points at 168, 500, 1000 and 2000 hours	Visual Check
Thermal Cycling	-5°C to +70°C, 500 cycles	Visual Check
Humidity	85% relative humidity, 55°C, 1000 hours	Visual Check

6.6 Shock Strain Guidance

A useful metric to compare the impact of design modifications to SJR and assess SJR risk during shock events is strain measurement. This strain measurement, also referred to as shock strain, utilizes strain gages to measure the surface strain of a motherboard. Please note that Intel also publishes strain guidance specifically for manufacturing. This manufacturing guidance is part of the Board Flexure Initiative (BFI) and those strain limits are commonly referred to as BFI strain. More information is available in the BFI Manufacturing Advantage Service (MAS). **DO NOT use BFI strain values for shock strain testing and DO NOT use shock strain guidance for BFI.** These two strain metrics are significantly different and are not interchangeable. Using the BFI strain values for a design metric will likely result in a poor system design.

Given parameters unique to the board of interest, such as board thickness, the board surface strain directly correlates to the amount of board curvature. The amount of motherboard curvature in the critical locations directly beneath the solder balls is indicative of the reliability of the component solder joints. This measurement is typically made at the corners of the BGA components. The shock strain results are sensitive to the application of the strain gages. Guidance for strain gage application is available in the Shock Strain Monitoring Customer Reference Document (CRD). Your Intel Corporate Quality Engineer is also available for help with strain gage attach

training. This Shock Strain Monitoring CRD outlines the proper selection, application, and usage of the strain gages and strain instrumentation to attain repeatable and valid results. The Shock Strain Monitoring CRD also discusses proper reduction of the data in order to use the data to compare to the Intel strain guidance.

The strain guidance was developed from simulations and empirical testing using the Intel reference thermal solution for the PCH and Intel recommended pad types and sizes. Three strain ranges are determined to quantify associated SJR risk for the Critical to Function solder joints. The Non-Critical to Function solder balls may have some cracking and fractures when the strain measurements are within this guidance.

The following table lists the three ranges for the PCH.

Table 6-3. Shock Strain Guidance

For 0.062" boards Shock Strain (micro strain, με)	For 0.093" boards Shock Strain (micro strain, με)	For 0.13" boards Shock Strain (micro strain, με)	Associated Risk	Comments
1500	1200	1100	1,2	3,4

Notes:
1. The Minimum Principal Strain (E-min) Metric values in all corners should be less than the E-min guidance.
2. In a design exceeding the guidance, a change to the design is strongly recommended to reduce the bending of the motherboard under shock.
3. This E-min metric guidance value is only applicable to this package.
4. Strain value is provided for guidance only. Testing is recommended on actual design to confirm SJR performance.

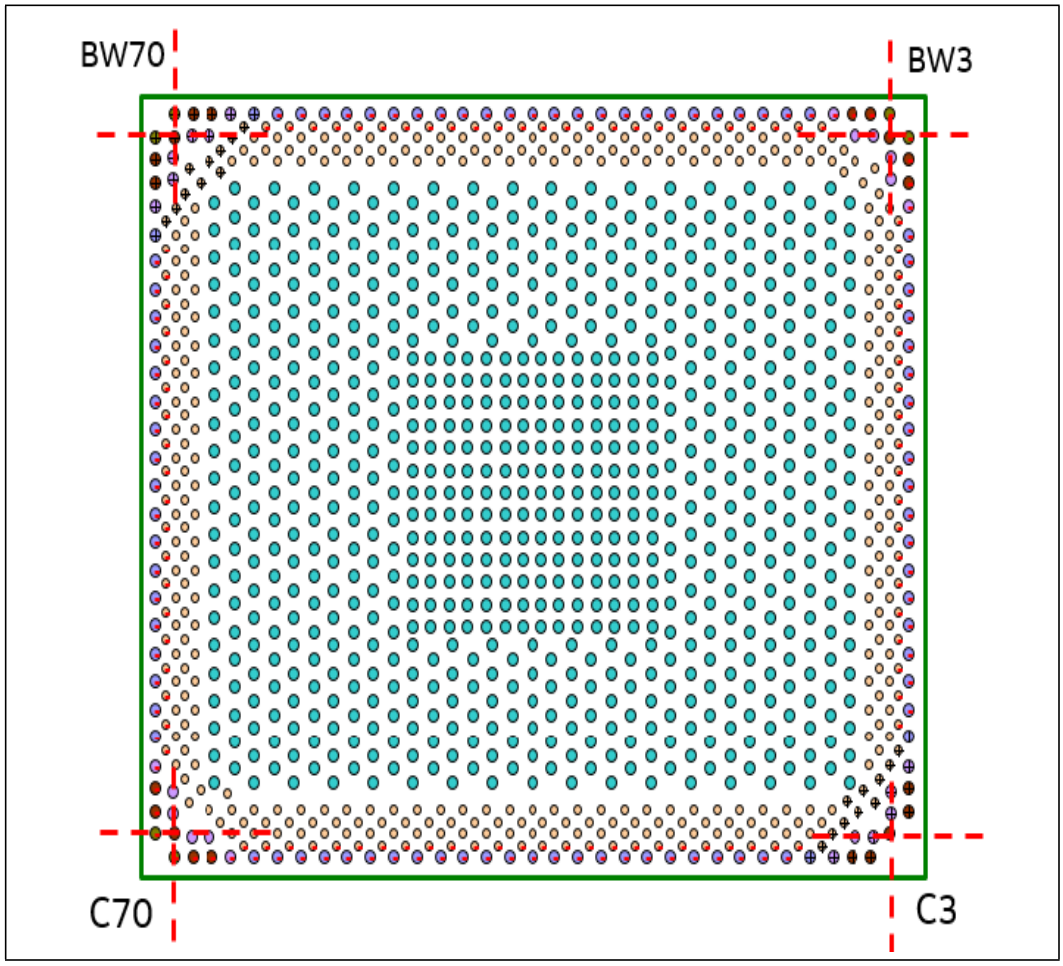
The associated risk levels correspond to the likelihood of solder joint failure. A Low level of risk is unlikely to result in critical to function solder joint failures. When strain measurements are made from a small sample of boards or systems and fall within the Medium risk range, there is insufficient information to assess the risk. It is suggested that additional systems or boards are tested and failure analysis, such as dye and peel, is conducted to assess the risk. A High risk is likely to result in a significant quantity of solder joint failures of critical solder balls. A change to the design is strongly recommended to reduce the bending of the motherboard under shock. Incorporating the Intel Reference Design Heatsink into the design or adopting the design practices outlined in the Desktop, Workstation, and Server System Mechanical Design Guidance for Dynamic Events will improve the strain response and therefore reduce SJR risk.

The BGA Shock strain gage location is a critical parameter for strain accuracy. The strain gage rosette center will be published in x,y coordinates with the (0,0) located at the package center. Please take note that the PCB coordinate system may have a different center (0,0) location; so the strain gage coordinates may need to be offset or adjusted for local package coordinate center. Please refer to Table 6-4 and Table 6-3 for specifics on the coordinates and strain gage rosette centers.

Table 6-4. Intel® C620 Series Chipset BGA Shock Strain Gage Coordinates Location

Corner	Strain Gage Coordinates (x, y)
C3	15.497 mm, -12.497 mm
BW3	15.497 mm, 12.497 mm
BW70	-15.497 mm, 12.497 mm
C70	-15.497 mm, -12.497 mm

Figure 6-3. Intel® C620 Series Chipset BGA Shock Strain Gage Location



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7 Reference Thermal Solution

7.1 Reference Thermal Solution

Intel has developed a reference thermal solutions to meet the cooling needs of the component under operating environments and specifications defined in this document. This chapter describes the overall requirements for the push-pinned heatsink reference thermal solution, including critical-to-function dimensions, operating environment, and validation criteria.

7.1.1 Operating Environment

The reference thermal solution was designed assuming both a max fan speed condition and an acoustic fan speed condition. Table 7-1 provides operating environmental conditions applied in defining and designing the reference cooling solution.

Table 7-1. Operating Environmental Boundary Conditions

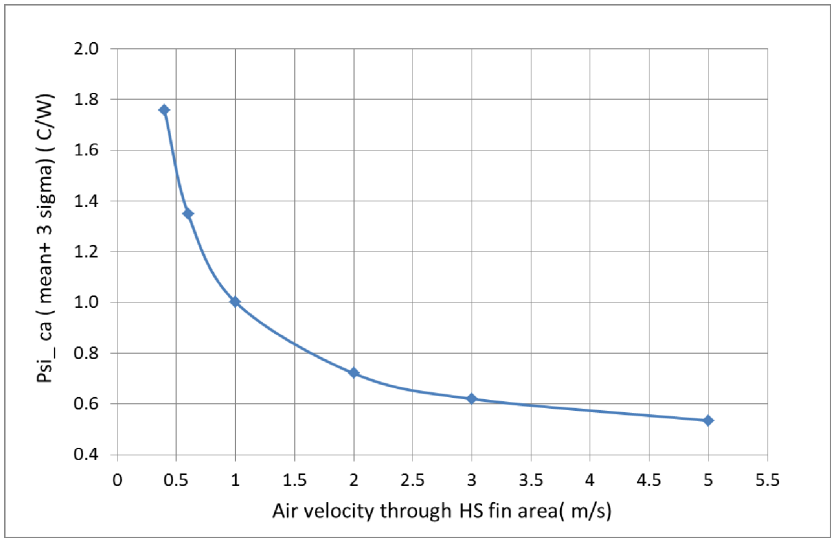
	Conditions		
Parameter	**High Fan Speed**	**Acoustic Fan Speed**	**Notes**
T_{SA}	35 °C	25 °C	1
Altitude	900 m		
T_{LA}	60 °C	60 °C	2
Air Flow	2 m/s	> 0.65 m/s	
Power	TDP		3

Notes:
1. T_{SA} refers to the environment external to the system.
2. T_{LA} refers to the inlet temperature at the component heatsink.
3. Power dissipated by the device under acoustic conditions is considered to be at mid point between idle power and TDP.

7.1.2 Reference Design Heatsink Performance

The *simulated* thermal performance of reference heatsink performance characterization is provided in Figure 7-1. Since this data was measured at sea level, a correction factor would be required to estimate thermal performance at other altitudes.

Figure 7-1. 59 x 65.5 x 30 mm Heatsink Thermal Performance Versus Approach Velocity

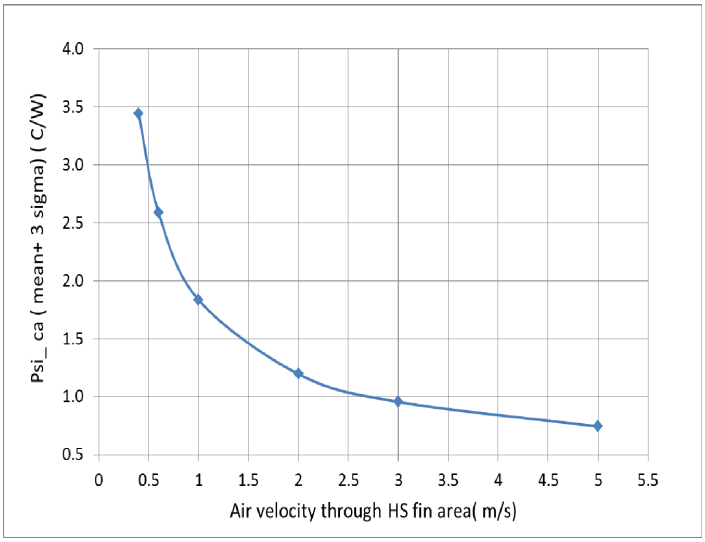


Notes:

1. Where Alpha= 0.8757, Beta = 0.6207, Gamma= 0.8689 based on SKU T.
2. Thermal Interface Material (TIM): Honeywell PCM45F*
3. IM effective end of life (EOLife) performance model derived from test results:

Psi-cs=0.187C/W, Effective K=1.2 W/MK, 0.127 mm thickness, for pressure at 4.35 Psi TIM preload on IHS.

Figure 7-2. 59 x 65.5 x 10.9 mm Heatsink Thermal Performance Versus Approach Velocity



Notes:

1. See the following table for Alpha, Beta and Gamma values.
2. Thermal Interface Material (TIM): Honeywell PCM45F*
3. IM effective end of life (EOLife) performance model derived from test results:

Psi-cs=0.187C/W, Effective K=1.2 W/MK, 0.127 mm thickness, for pressure at 4.35 Psi TIM preload on IHS.

Table 7-2. 59 x 65.5 x 10.9 mm Heatsink Performance Curve Alpha, Beta, Gamma Values

	H62045-001						
	59 X 65.5 X 10.9						
SKU	1G	2	4	E	M	L	T
Alpha	0.3581	0.3564	0.3560	0.3394	0.3339	0.3156	0.3198
Beta	1.5515	1.5376	1.5246	1.5154	1.5005	1.5192	1.4938
Gamma	0.7866	0.7867	0.7875	0.7879	0.7876	0.7878	0.7875

Table 7-3. Reference Heatsinks Cooling Capabilities

Heatsink Description	Heatsink P/N	System	Altitude (m)	Velocity (m/s)	Trise (°C)	T_{LA}	Max Cooling Capability (W)	Notes
59 x 65.5 x 30 mm Extruded Al	H53980-001 H54219-001 H73752-001	Max airflow	900	2	18	53	37.9	1, 3, 5
		HTA	900	2	18	63	29.6	1, 3, 5
		Fan Failure	900	1	13	48	33.9	1, 3, 5
		Max airflow	900	1.8	23	58	32.8	1, 3, 4
		Fan Failure	900	1.6	25	60	30.1	1, 3, 4
59 x 65.5 x 10.9 mm Extruded Al	H62045-001	Max airflow	900	2	18	53	23.9	2, 3, 5
		HTA	900	2	18	63	18.6	2, 3, 5
		Fan Failure	900	1	13	48	19.8	2, 3, 5

Notes:
1. Heatsink performance determined based on C627 SKU.
2. Heatsink performance determined based on C628SKU.
3. Performance analysis are only based on CFD modeling.
4. Thermal environmental conditions are based on a 4U reference system
5. Thermal environmental conditions are based on a 2U reference system

7.1.3 Heatsink Assembly

The reference thermal solution for the components is a passive extruded heatsink with thermal interface. It is secured to the PCB using 4 push-pin fasteners. Following illustration shows the reference thermal solution assembly and associated components.

Full mechanical drawings of the thermal solution assembly and the heatsink clip are provided in the appendix.

Figure 7-3. Heatsink Assembly

7.1.3.1 Heatsink Orientation

Since this solution is based on a unidirectional heatsink, it implies that the airflow direction must be aligned with the direction of the heatsink fins.

7.1.3.2 Extruded Heatsink Profiles

The reference thermal solution uses an extruded heatsink for cooling the components. Other heatsinks with similar dimensions and increased thermal performance may be available. See full mechanical drawings for additional details.

7.1.3.3 Thermal Interface Material

A thermal interface material (TIM) improves conductivity between the package IHS and heatsink. The reference thermal solution uses Honeywell PCM45F, 0.25 mm (0.010 in.) thick, 35 mm x 35 mm (1.38 in. x 1.38 in.) square.

Note: Unflowed or "dry" Honeywell PCM45F has a material thickness of 0.010 in. The flowed or "wet" Honeywell PCM45F has a material thickness of ~0.003 in. after it reaches its phase change temperature.

To achieve TIM performance target, heatsink shall apply 22.3 N [5.0 lbf]. This defines the minimum heatsink load requirement insuring minimum TIM bond line thickness (BLT) is achievable.

7.1.4 Heatsink Mass

Table 7-4. Reference Heatsinks Mass

Heatsink Description	Heatsink P/N	Mass (g)
59 x 65.5 x 30 mm Extruded Al	H53980-001	120±10
	H53980-001 H54219-001 H73752-001	120±12
59 x 65.5 x 10.9 mm Extruded Al	H62045-001	46±4.6

7.1.5 Heatsink Retention

The reference solution uses a 4 push-pins. Push-pins are selected to support boards thickness ranges 1.57 mm to 3.3 mm [0.062” and 0.130”].

Table 7-5. Push-Pin P/N

Part Number	MB Thickness	Heatsink Preload Range	Pullout Force
83FT02-03-9909	62-78 mil	62 mil: 7.0 to 12.72 lbf 78 mil: 7.75 to 13.6 lbf	30 lbf each push-pin
83FT05-03-9909	93 mil	6.9 to 12.7 lbf	30 lbf each push-pin
83FT11-03-9909	130 mil	6.6 to 12.9 lbf	30 lbf each push-pin

Notes:

1. Push-pins are designed for specific board thickness. See supplier specifications for details.
2. Heatsink preload ranges are based on 3 sigma worst case analysis.

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A Component Suppliers

Third-party suppliers are enabled so that reference thermal and mechanical components are available. Suppliers identified in Table A-1 have notified Intel of their intent to support the Intel® C620 Series Chipset PCH by supplying thermal and mechanical solutions based on Intel reference design.

Notes:

1. Supplier information provided in the table was deemed accurate at the time of this document release. Customers planning on using Intel reference designs should contact the component suppliers for the latest information.
2. These vendors are listed by Intel as a convenience for its customers. Intel does not make any representations or warranties whatsoever regarding the quality, reliability, functionality, or compatibility of these devices.

Table A-1. Thermal Solution Enabled Supplier Listing

Part		Intel Part Number	Supplier (Part Number)	Contact Information
59 x 65.5 x 30 mm Heatsink Assembly includes: • Heatsink • Thermal Interface Material • Push-pin Assembly	62 to 78 mil boards	H53980-001	0A15064101	Chaun-Choung Technology Corp (CCI)* Monica Chih (Taiwan) 866-2-29952666, x131 monica_chih@ccic.com.tw
	93 mil board	H54219-001	0A15117101	
	130 mil board	H73752-001	0A15118101	
59 x 65.5 x 10.9 mm Heatsink Assembly includes: • Heatsink • Thermal Interface Material • Push-pin Assembly	62 to 78 mil boards	H62045-001	0A14015101	
Thermal Interface 0.25 x 35 x 35 mm	PCM45F_35x35		Honeywell PCM45F*	Andrew Ho (Worldwide, HK) (852)9095-4593 andrew.ho@honeywell.com David Shen (PRC) david.shen@honeywell.com 86-21-289-44064

Table A-1. Thermal Solution Enabled Supplier Listing

Part		Intel Part Number	Supplier (Part Number)	Contact Information
Heatsink Attach Fastener	62 to 78 mil boards		83FT02-03-9909	ITW Electronics Business Asia Co. Ltd A4, 3-2, K.E.PZ. Kaohsiung, Taiwan Tel. 886-7-811-9206~10 (5 lines) Fax: 886-7-811-1795 Taipei Office: 3F-7, No.193, Ching-Hsing RD., Wen-Shan District, Taipei, Taiwan Tel. 886-2-2930-8340~1 (2 lines) Fax: 886-2-2930-8342
	93 mil board		83FT05-03-9909	
	130 mil board		83FT11-03-9909	
	62 to 78 mil boards		83FT02-37-9909	

Notes:
1. Contact the supplier directly to verify time of component availability.
2. Heatsink fastener is independent of heatsink assembly. Proper push-pin fastener selection protects the chipset heatsink from shock and vibration.

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B Mechanical Drawings

Table B-1 lists the mechanical drawings included in this appendix.

Table B-1. Mechanical Drawing List

Drawing Description	Figure Number
1310-FCBGA15 Package Mechanical Drawing (Sheet 1 of 2)	Figure B-1
1310-FCBGA15 Package Mechanical Drawing (Sheet 2 of 2)	Figure B-2
PCB Mechanical Keep-out Drawing - 4 Hole Heatsink (Sheet 1 of 2)	Figure B-3
PCB Mechanical Keep-out Drawing - 4 Hole Heatsink (Sheet 2 of 2)	Figure B-4
PCB Mechanical Keep-out Drawing - 2 Hole Heatsink (Sheet 1 of 2)	Figure B-5
PCB Mechanical Keep-out Drawing - 2 Hole Heatsink (Sheet 2 of 2)	Figure B-6
H53980 - Reference Heatsink Assembly Drawing - Sheet 1 of 2	Figure B-7
H53980 - Reference Heatsink Assembly Drawing - Sheet 2 of 2	Figure B-8
H54219 - Reference Heatsink Assembly Drawing - Sheet 1 of 2	Figure B-9
H54219 - Reference Heatsink Assembly Drawing - Sheet 2 of 2	Figure B-10
H73752 - Reference Heatsink Assembly Drawing - Sheet 1 of 2	Figure B-11
H73752 - Reference Heatsink Assembly Drawing - Sheet 2 of 2	Figure B-12
H62045 - Reference Heatsink Assembly Drawing - Sheet 1 of 2	Figure B-13
H62045 - Reference Heatsink Assembly Drawing - Sheet 2 of 2	Figure B-14

Figure B-1. 1310-FCBGA15 Package Mechanical Drawing (Sheet 1 of 2)

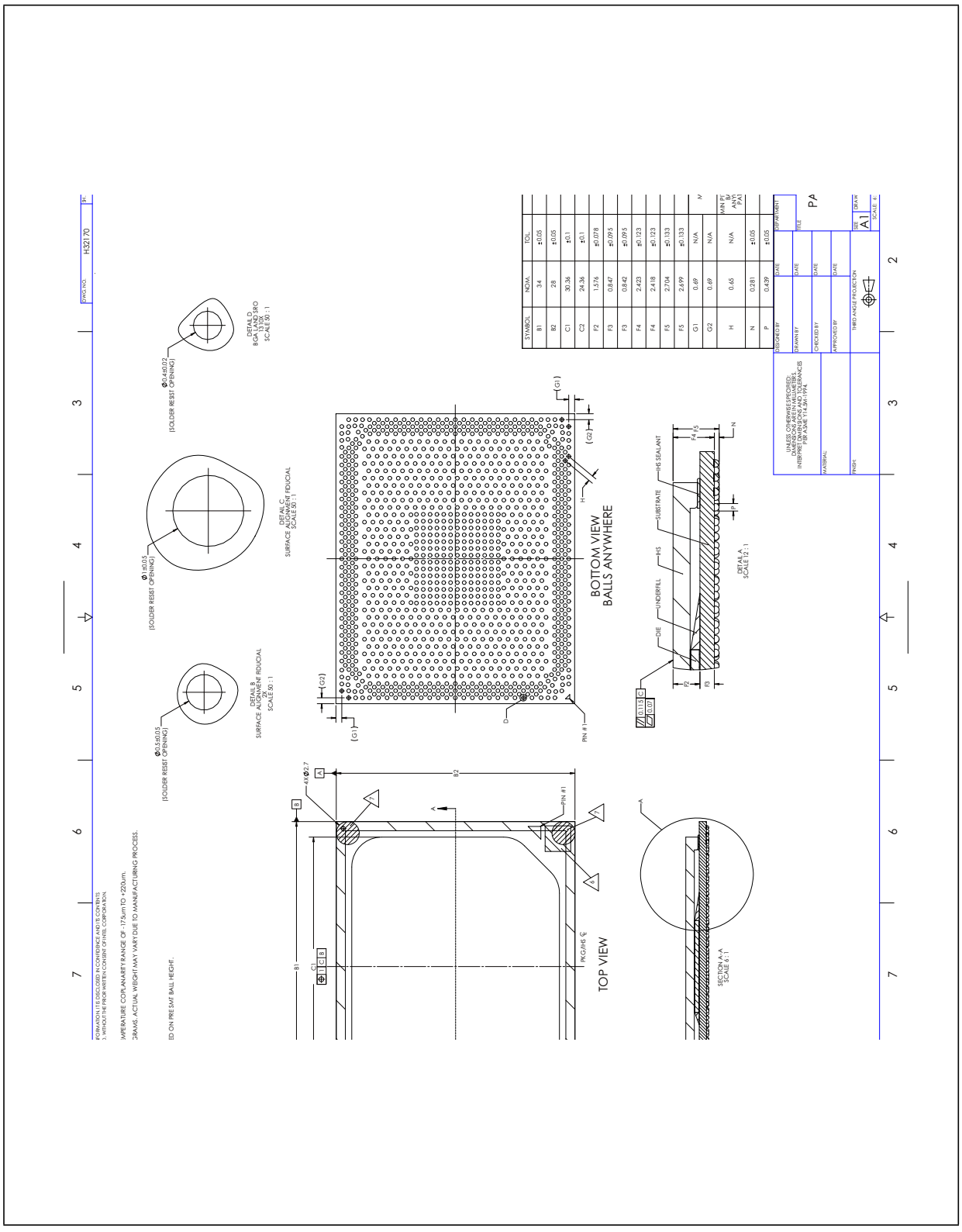


Figure B-2. 1310-FCBGA15 Package Mechanical Drawing (Sheet 2 of 2)

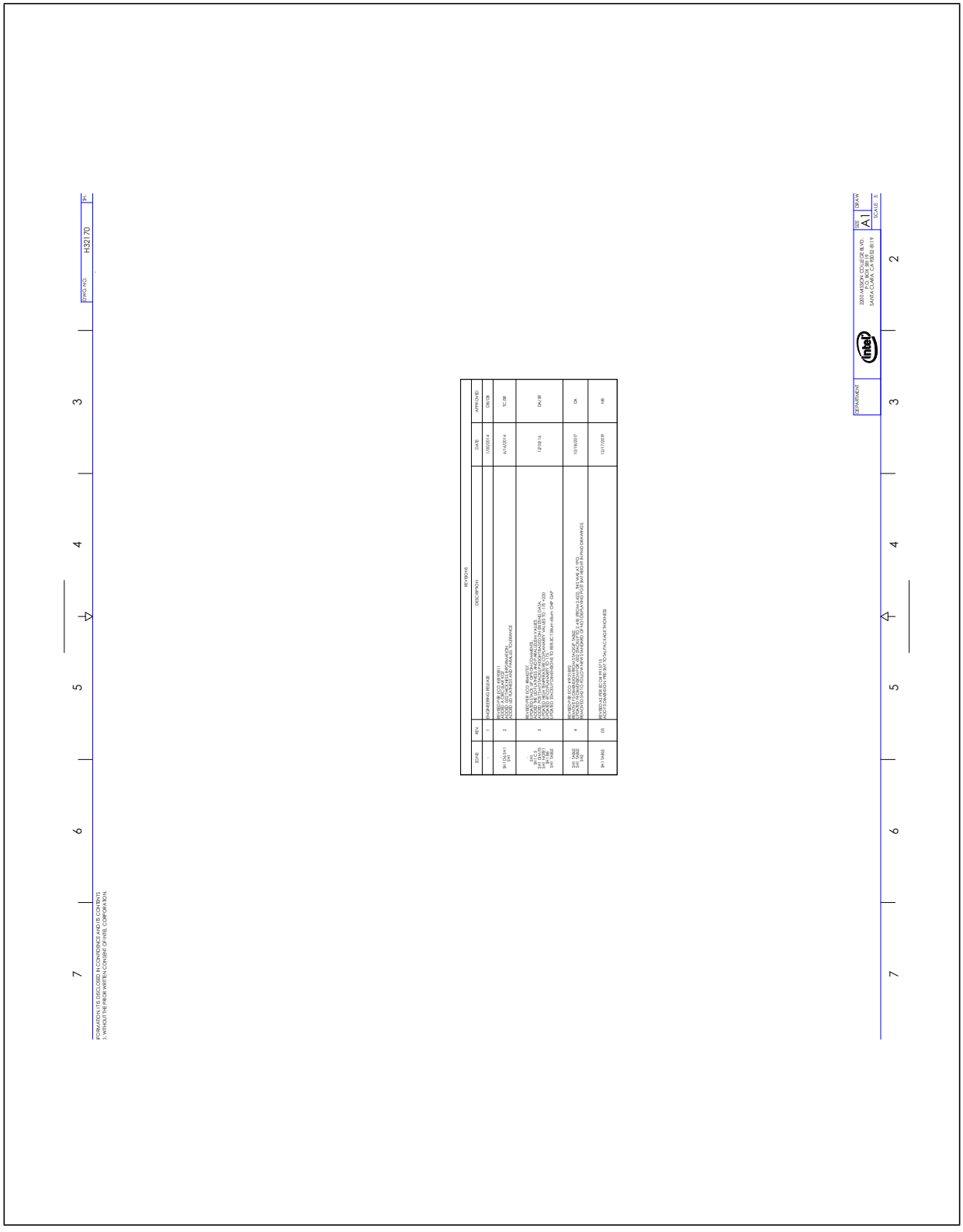


Figure B-3. PCB Mechanical Keep-out Drawing - 4 Hole Heatsink (Sheet 1 of 2)

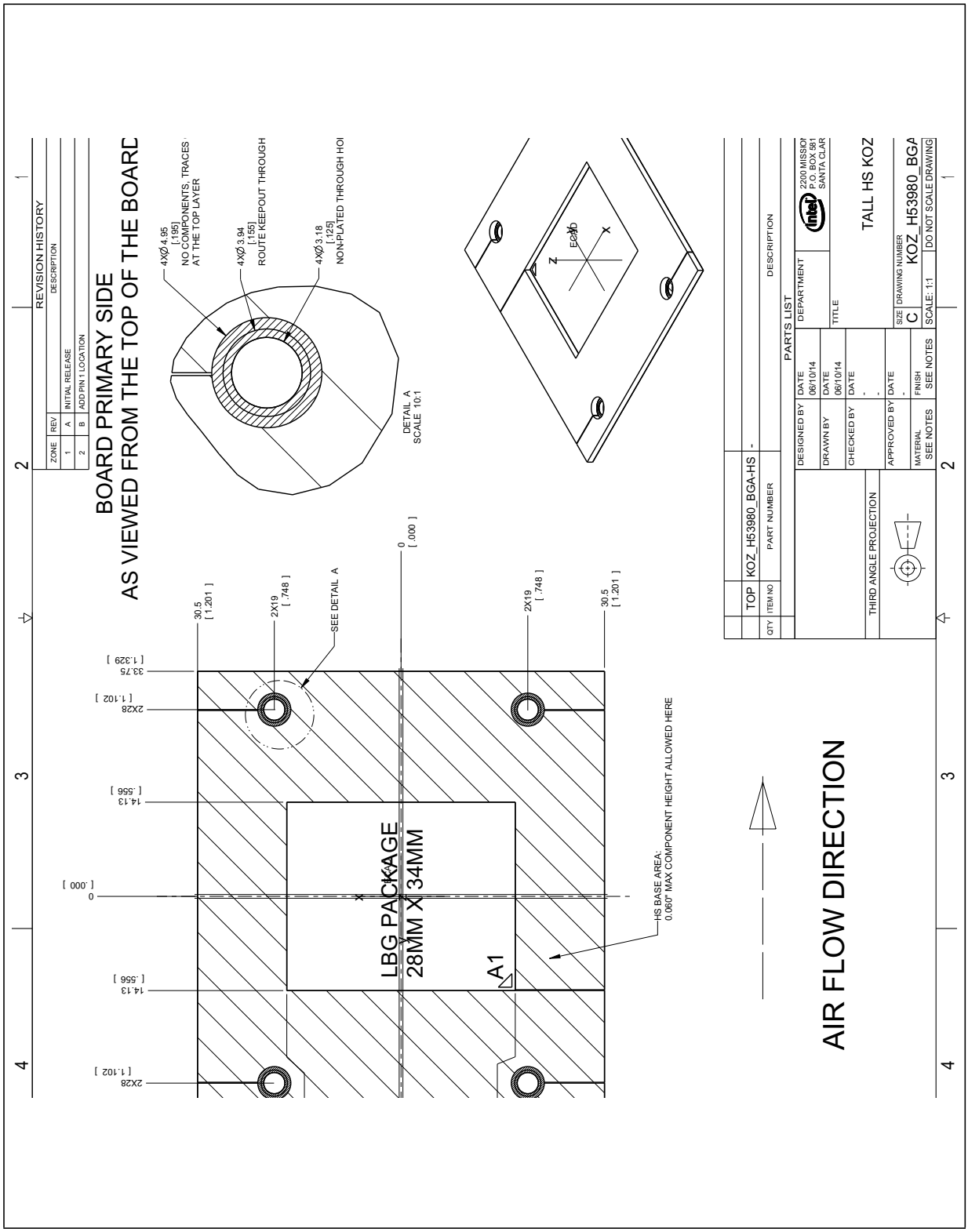


Figure B-4. PCB Mechanical Keep-out Drawing - 4 Hole Heatsink (Sheet 2 of 2)

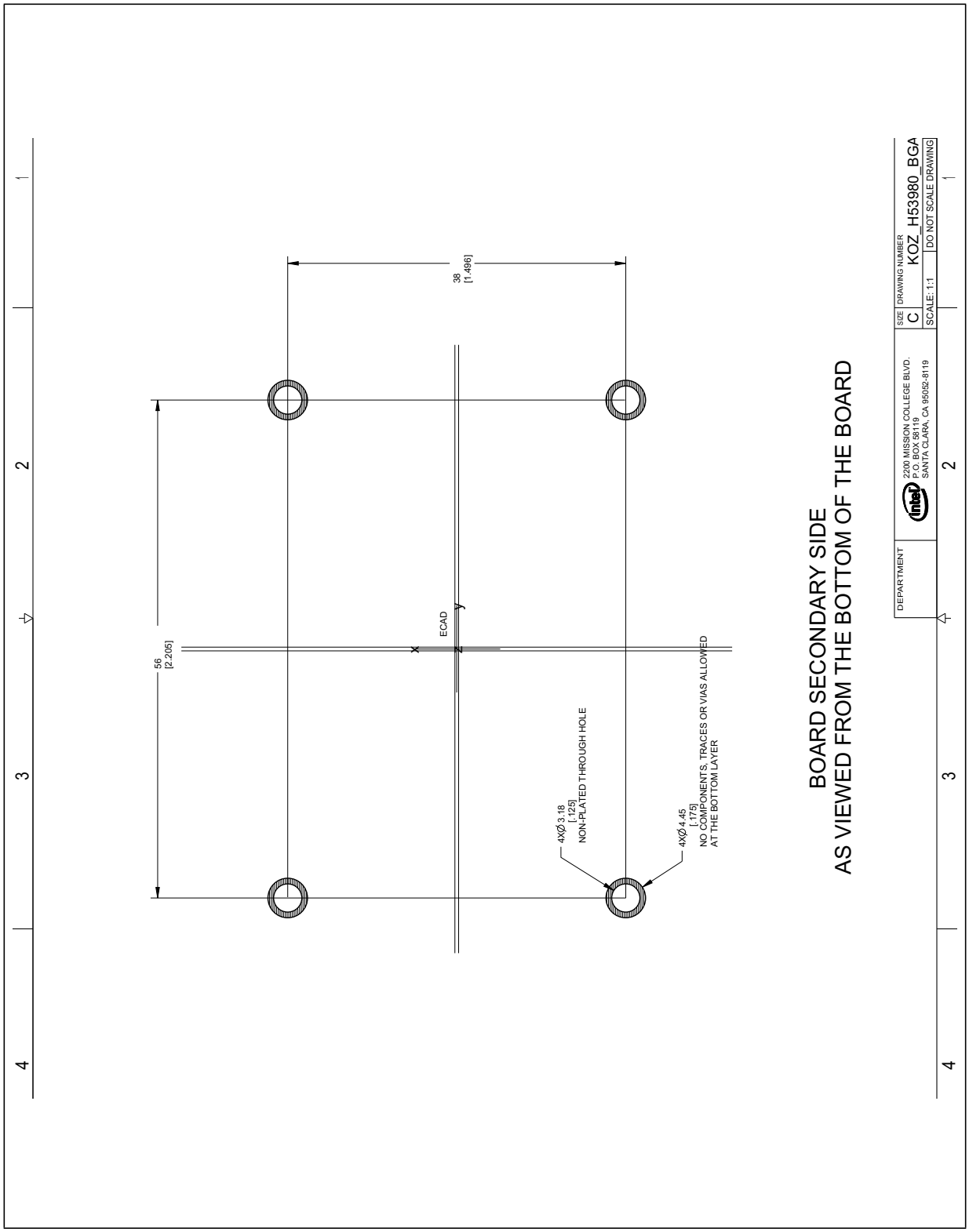


Figure B-5. PCB Mechanical Keep-out Drawing - 2 Hole Heatsink (Sheet 1 of 2)

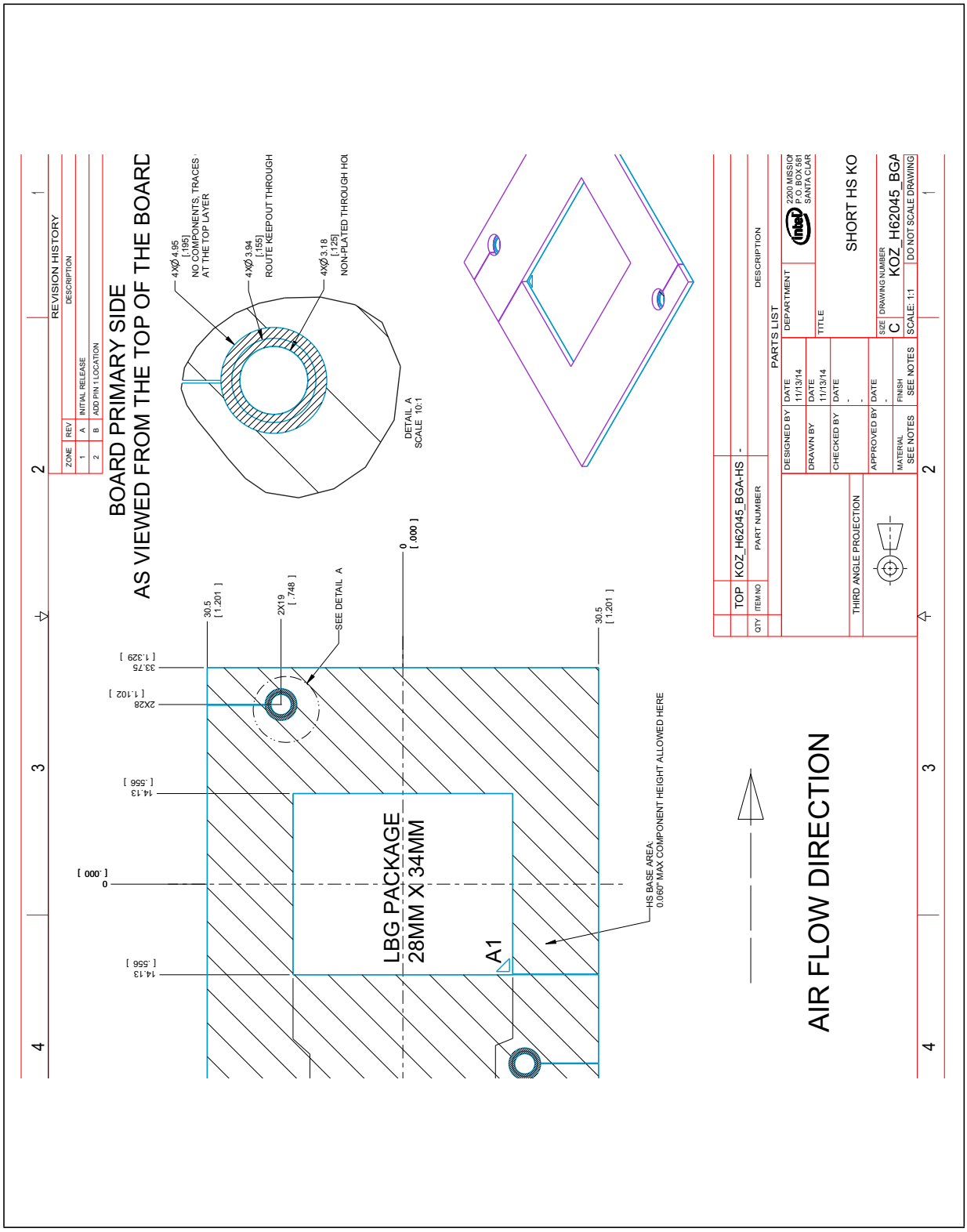


Figure B-6. PCB Mechanical Keep-out Drawing - 2 Hole Heatsink (Sheet 2 of 2)

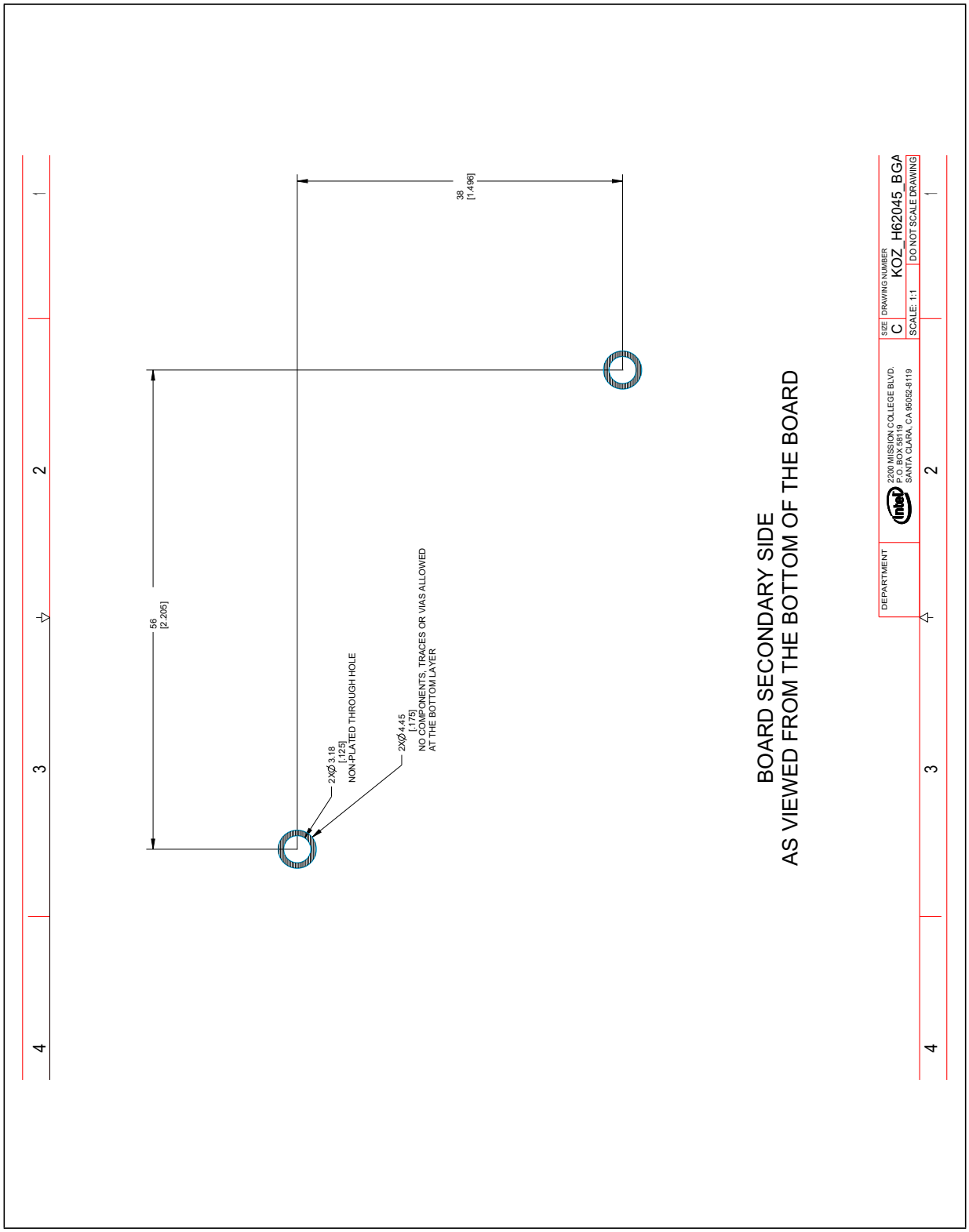


Figure B-7. H53980 - Reference Heatsink Assembly Drawing - Sheet 1 of 2

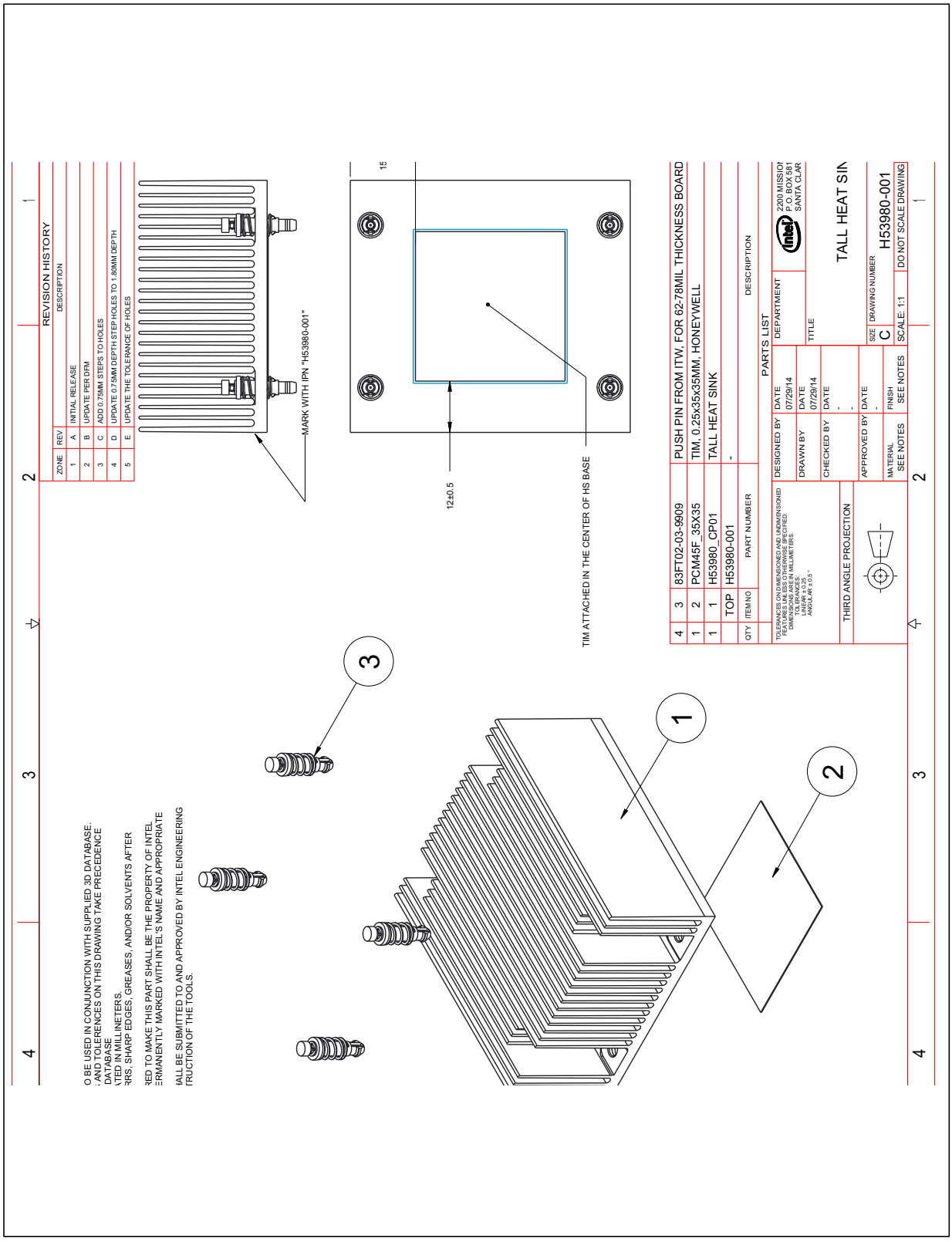


Figure B-8. H53980 - Reference Heatsink Assembly Drawing - Sheet 2 of 2

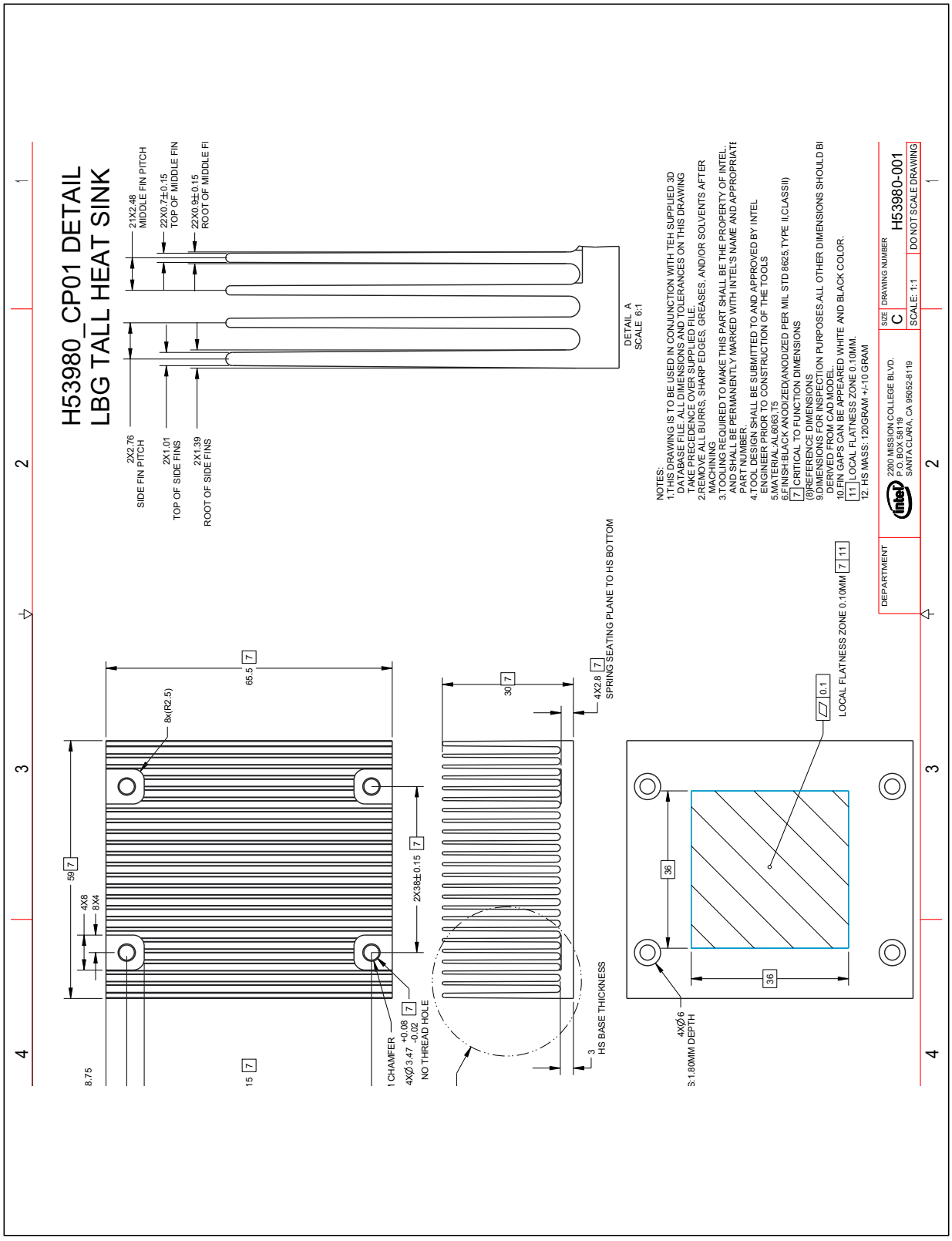


Figure B-9. H54219 - Reference Heatsink Assembly Drawing - Sheet 1 of 2

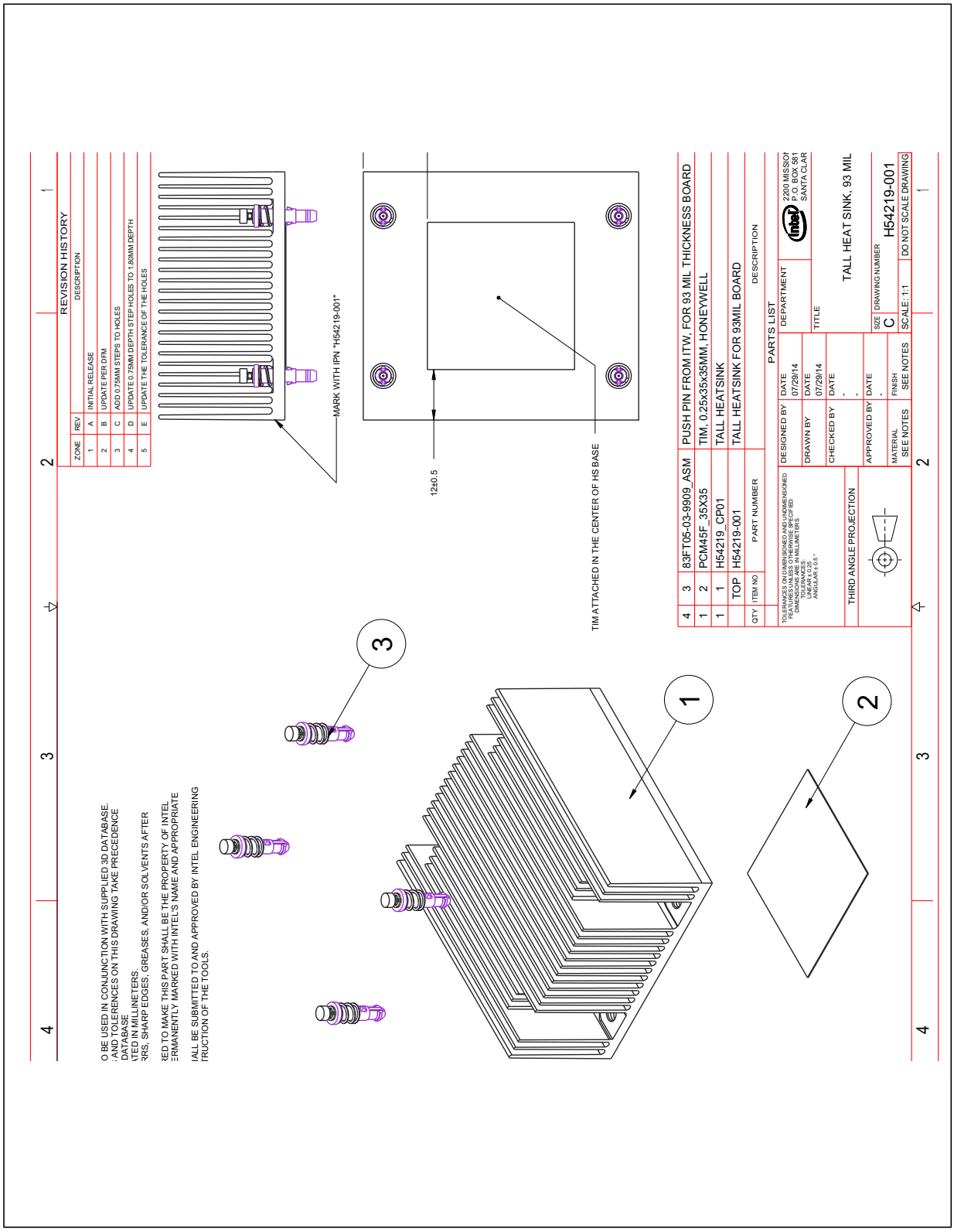


Figure B-10. H54219 - Reference Heatsink Assembly Drawing - Sheet 2 of 2

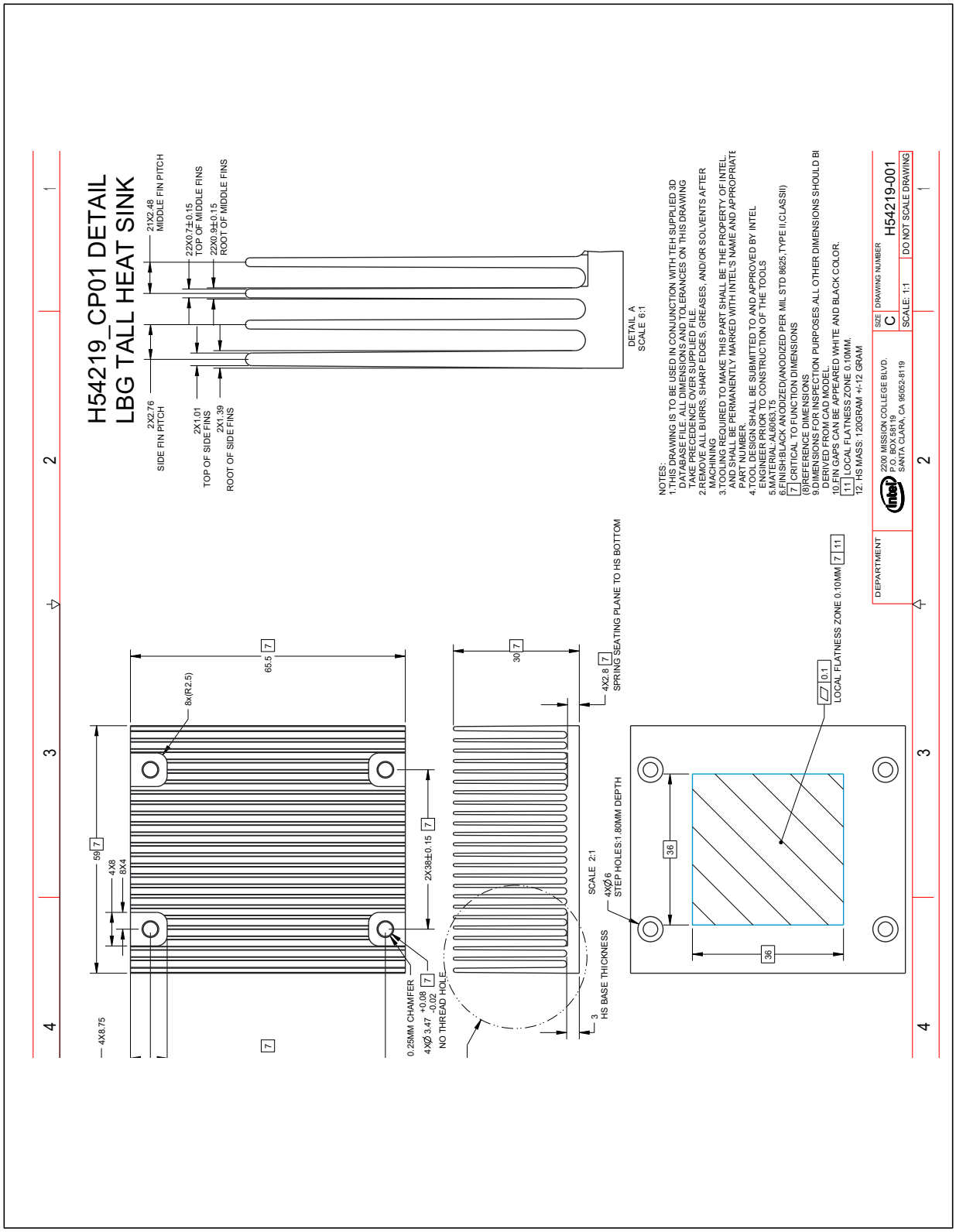


Figure B-11. H73752 - Reference Heatsink Assembly Drawing - Sheet 1 of 2

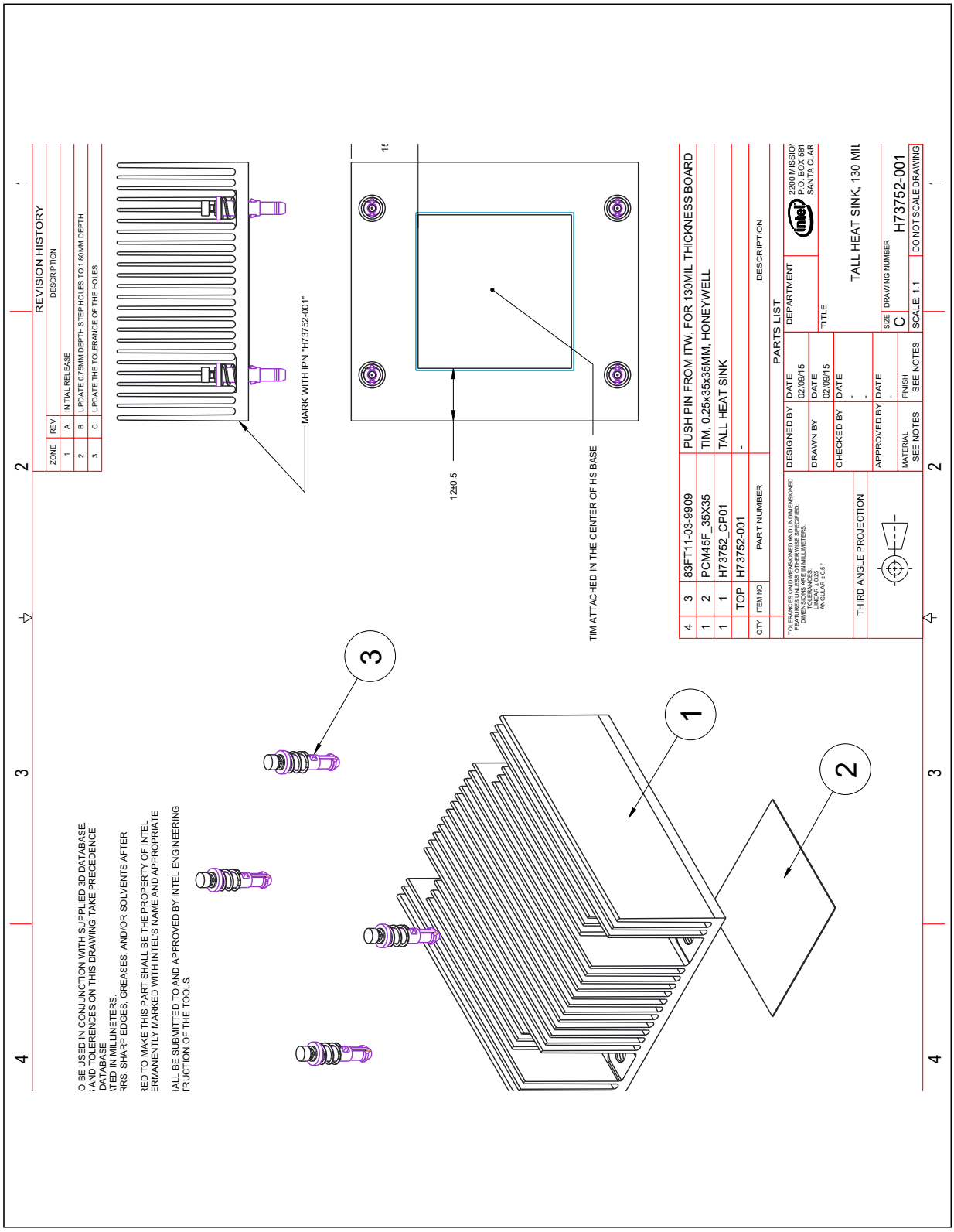


Figure B-12. H73752 - Reference Heatsink Assembly Drawing - Sheet 2 of 2

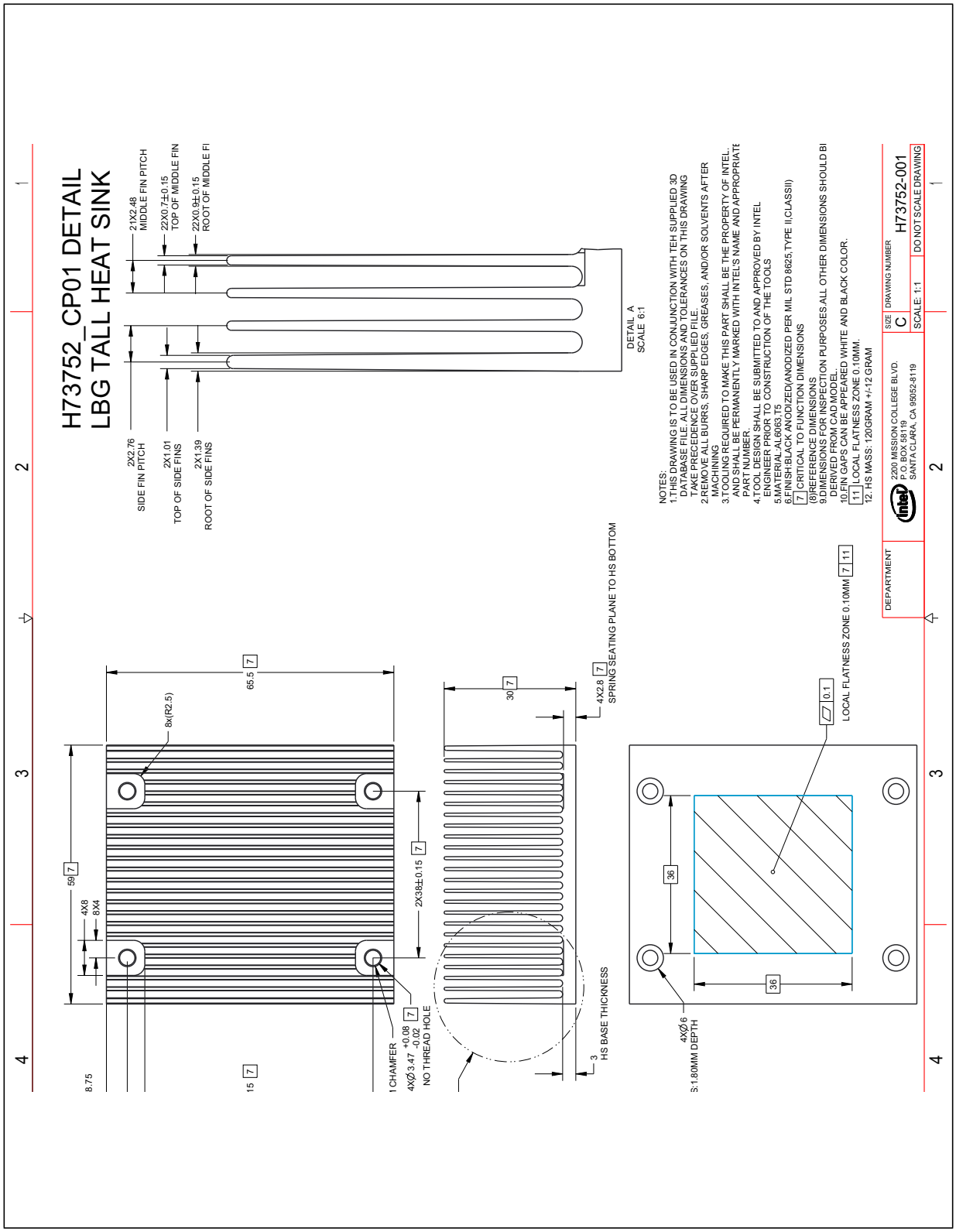


Figure B-13. H62045 - Reference Heatsink Assembly Drawing - Sheet 1 of 2

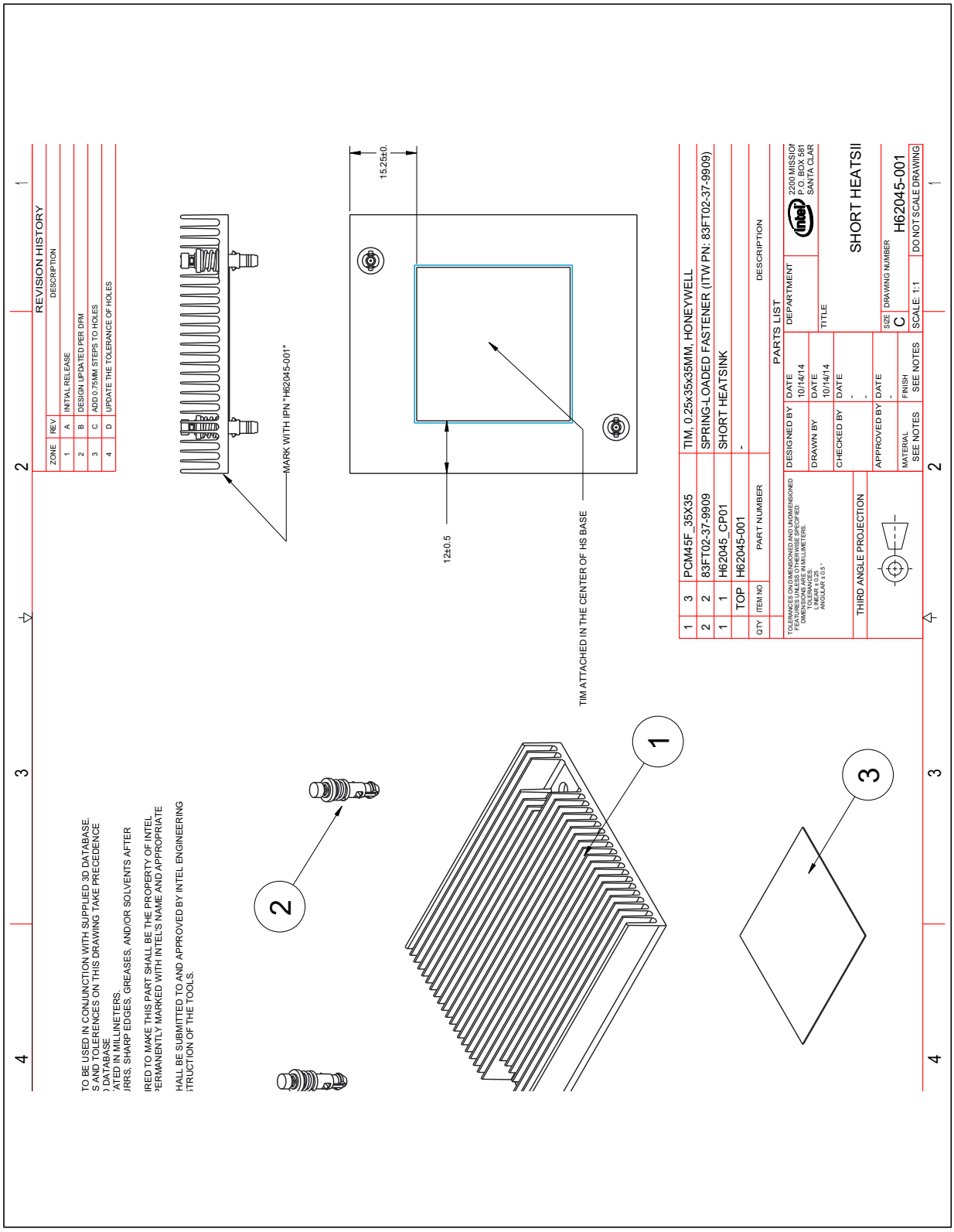
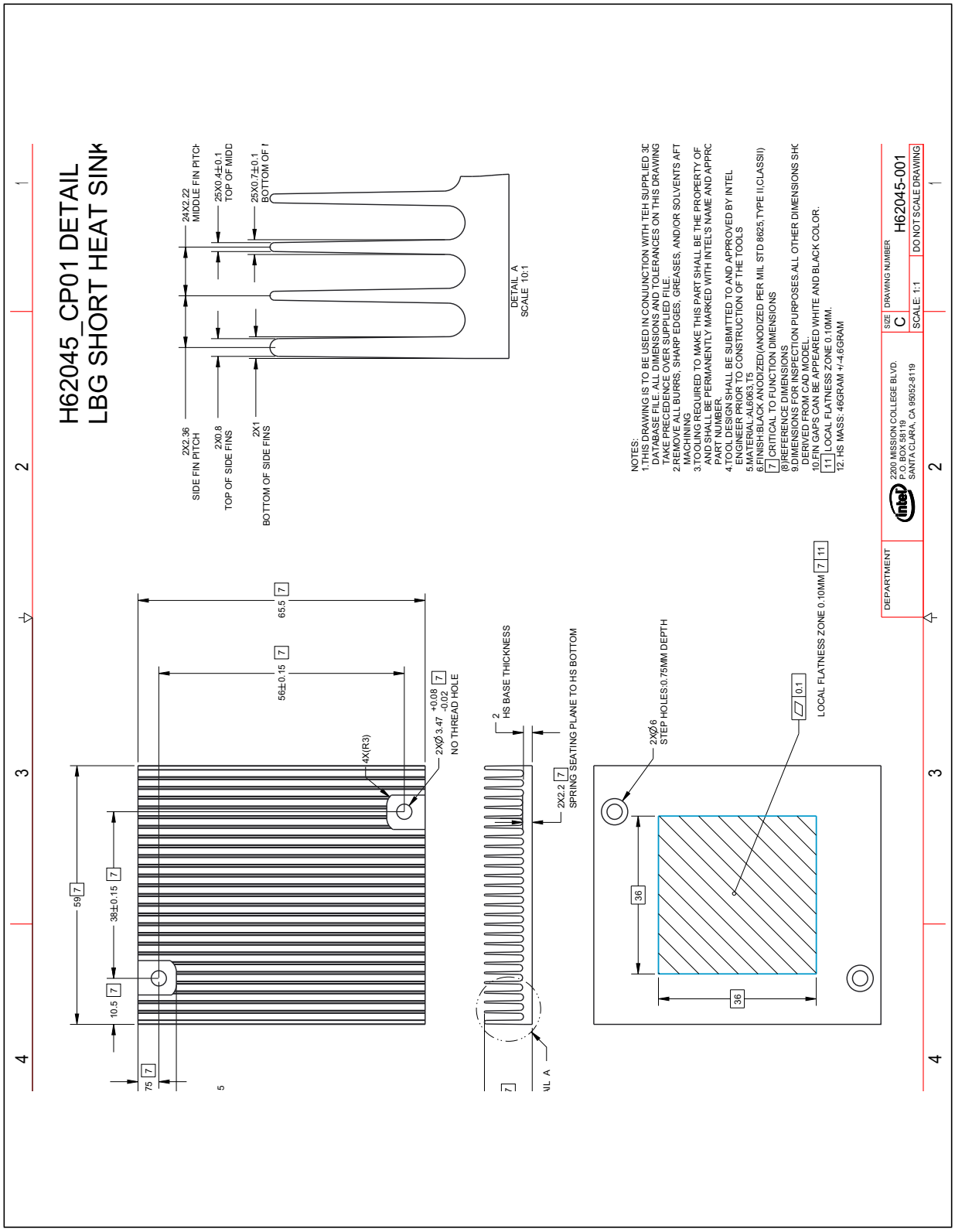


Figure B-14. H62045 - Reference Heatsink Assembly Drawing - Sheet 2 of 2



C Thermal Metrology

C.1 Thermocouple Attachment

The thermocouple must be calibrated before measurements are taken. Measurement error can be reduced by improving the thermal contact between the thermocouple and the measured surface and by minimizing the heat loss by conduction and radiation through the thermocouple leads. To minimize the measurement errors, it is recommended that the following approach be used:

1. Use 36-gauge or finer diameter K, T, or J type thermocouples. Intel's laboratory testing is usually done with type **T** thermocouples made by Omega (part number: 5SRTC-TT-T-36-72).
2. Attach the thermocouple bead or junction to the package top surface at the location define in the product Thermal-Mechanical Specification and Design Guide.
3. Using a heatsink with a metal base, the thermocouple should be attached at zero degree angle (parallel to package IHS surface).

C.2 Zero Degree Angle Attach Methodology

IHS Preparation:

1. Mill a 0.38 mm [15 mil] wide and 0.38 mm [0.15 mil] deep slot on the surface of the IHS starting at the centered package toward the edge IHS. The slot should be at least 1 mm (40 mil) in length and parallel to the heatsink fins.
2. Mill a second slot 0.79 mm [30 mil] wide and 0.51 mm [20 mil] deep in-line with the previous slot reaching the edge of the IHS. This slot should start or end at 1.02 mm [40 mil] from the center of the package.

Thermocouple Attachment:

1. Clean the IHS groove with IPA and a lint free cloth removing all residues prior to thermocouple attachment.
2. Place the thermocouple wire inside the groove letting the exposed wire and bead extend about 3.2 mm [125 mil] past the end of groove. Secure it with Kapton* tape as in Figure C-2, “Thermocouple Attachment” on page 49.
3. Lift the wire at the middle of groove with tweezers and bend the front of wire to place the thermocouple in the channel ensuring the tip is in contact with the end of the channel grooved in the IHS.
4. Press the wire down about 6mm [0.125"] from the thermocouple bead using the tweezers. Place a piece of Kapton* tape to hold the wire inside the groove. It is critical that the thermocouple bead makes contact with the IHS.
5. Measure resistance from thermocouple end wires (hold both wires to a DMM probe) to the IHS surface. This should be the same value as measured during the thermocouple conditioning.
6. Place a small amount of Loctite* 498 adhesive in the groove where the bead is installed. Using a fine point device, spread the adhesive in the groove around the needle, the thermocouple bead and the thermocouple wires already installed in the groove. Avoid moving the thermocouple bead during this step.

7. Allow time for the Loctite to cure.
   a. Allow the thermocouple attach set in open-air for at least 30 minutes. It is not recommended to use any curing accelerator, such as Loctite* Accelerator 7452 for this step, as rapid contraction of the adhesive during curing may weaken bead attach on the IHS.
   b. Remove the Kapton* tape, straighten the wire in the groove so it lays flat all the way to the end of the groove.
   c. Use a blade to shave excess adhesive above the IHS surface.
   d. Install new Kapton* tape to hold the thermocouple wire down and fill the rest of groove with adhesive. Make sure the wire and insulation is entirely within the groove and below the IHS surface.
   e. Curing time for the rest of the adhesive in the groove can be reduced using Loctite* Accelerator 7452.
   f. Repeat step 'c.' to remove any access adhesive to ensure flat IHS for proper mechanical contact to the heatsink surface.
8. Measure the resistance from the thermocouple end wires again using the DMM and verify the bead is still properly contacting the IHS.

Figure C-1. IHS Groove Dimensions

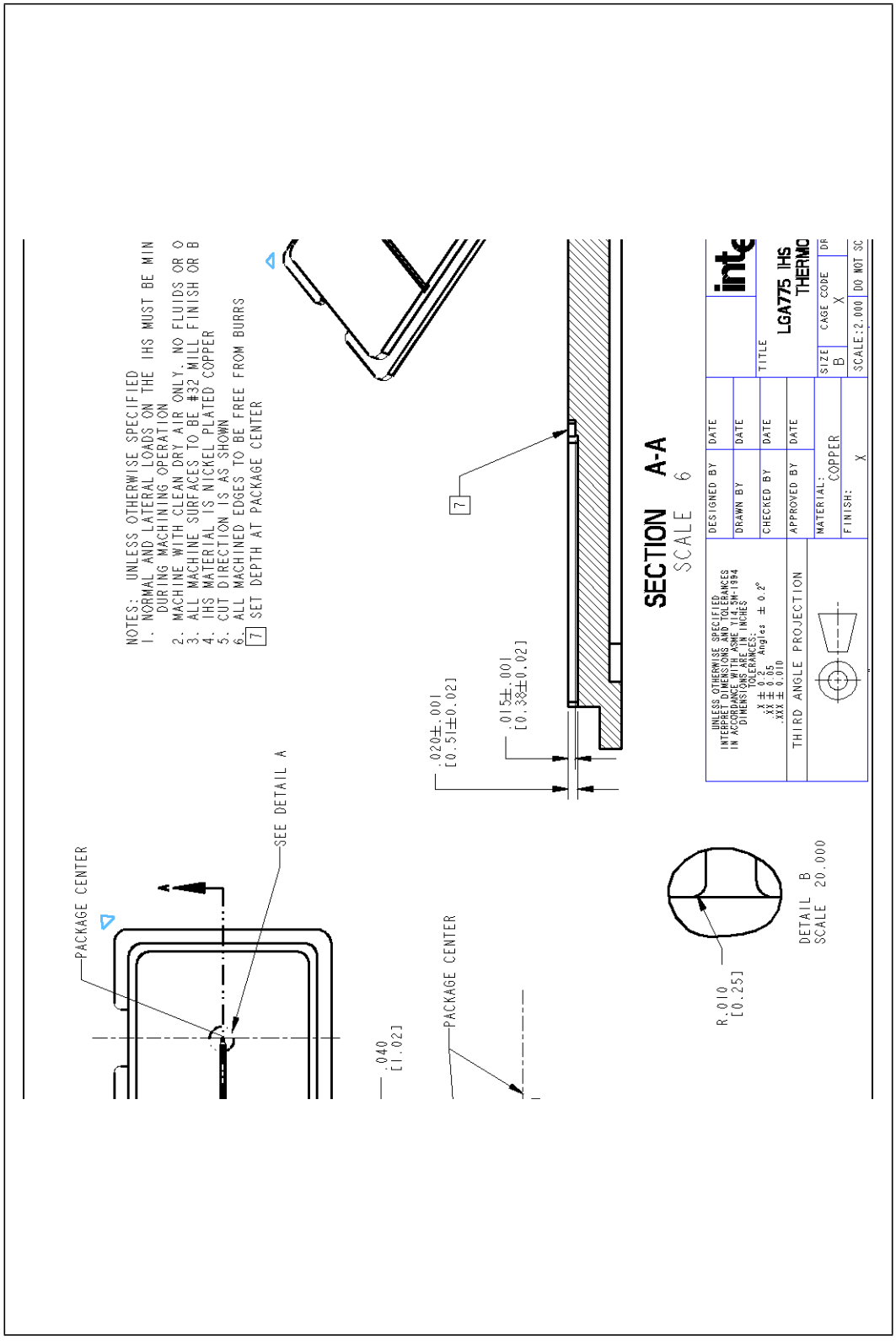
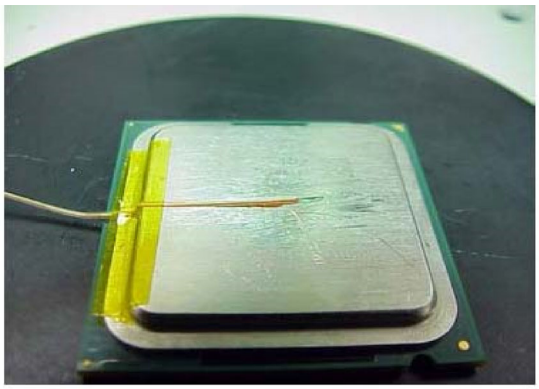
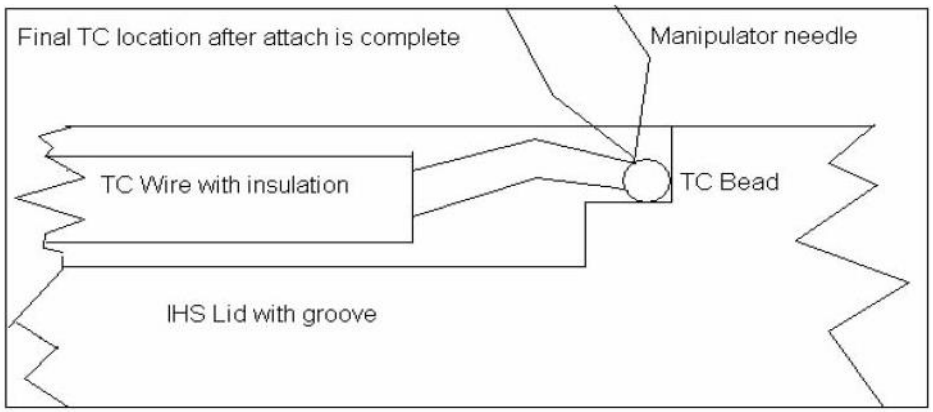


Figure C-2. Thermocouple Attachment



Note: Package from factor used in the illustration is only an example and may be different than the package described in this document.

Figure C-3. TC Bead Location



Note: Not to scale.

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