

4th Generation Intel[®] Core[™] Processor with Mobile Intel[®] QM87 Chipset Development Kit based on Small Form Factor

Development Kits User Guide

December 2013



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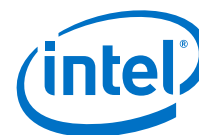
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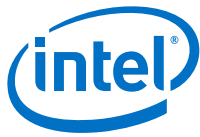


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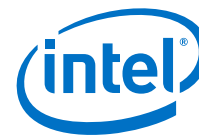
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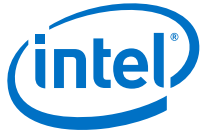
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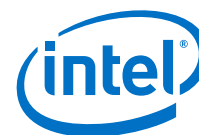


Revision History

Date	Revision	Description
December 2013	001	Initial release



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1.0 About This Development Kit

1.1 Introduction

The 4th Generation Intel® Core™ Processor with Mobile Intel® QM87 Chipset Development Kit is a dual-channel DDR3 mobility platform. It is designed to support the 4th Generation Intel® Core™ processor BGA and the Intel® 8 Series Chipset family Platform Controller Hub (PCH).

The development kit is based on Intel® Intelligent System Extended (ISX) Form Factor Reference Design. The Intel® ISX uses a new 4 × 4 inch form factor, a full performance computing platform in the smallest form factor possible that is able to support the 4th Generation Intel® Core™ processor. The Modular Board Design (MBD) of the Intel® ISX completes the critical signal paths for the processor and the supporting components according to Intel Design Guidelines.

This development kit provides you with the necessary materials to enable you to customize the board design to suit your requirements. Alternatively, for faster time to market, the board design can be used as is out of the box.

Note: The 4th Generation Intel® Core™ Processor was formerly known as Haswell CPU, the Intel® 8 Series Chipset family was formerly known as Lynx Point/Haswell PCH, and Haswell Platform was formerly known as Shark Bay Platform.

1.2 Terminology

Table 1. Terminology (Sheet 1 of 2)

Term	Definition
BIOS	Basic Input Output System
CMOS	Refers to the non-volatile configuration memory in the PCH
CPU	Central Processing Unit
DDR3	Double Data Rate Synchronous Dynamic Random Access Memory third generation
DP	Display Port
DVI	Digital Visual Interface
eDP	Embedded Display Port
GND	Signal Ground
HDD	Hard disk drive
HDMI	High Definition Multimedia Interface
LAN	Local Area Network
LED	Light Emitting Diode
LPC	Low Pin Count
mDP	Mini Display Port
ME	Intel Management Engine
OS	Operating System
PCH	Platform Controller Hub
PCI	Peripheral Component Interface
PCIe	Peripheral Component Interface Express
POST	Power-On Self Test

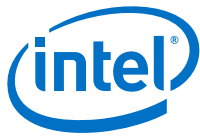


Table 1. Terminology (Sheet 2 of 2)

Term	Definition
RTC	Real Time Clock
S3	"Save to RAM" Sleep State
S5	"Soft Off" Sleep State
SATA	Serial - Advanced Technology Attachment
SIO	Super Input Output
SLP	Sleep
SO-DIMM	Small Outline Dual In-line Memory Module
SSD	Solid State Drive
USB	Universal Serial Bus
VCC	Used to signify circuit logic voltage
VDDQ	Used to signify DIMM logic supply voltage
VID	Voltage Identification
VTT	Used to signify signal termination voltage

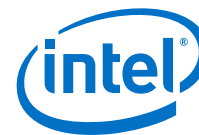
1.3 Development Board Parts

The development board includes the following parts listed in Table 2 unless stated otherwise.

Table 2. List of Development Board Parts

Development Board Parts	Model	Quantity
2GB (256M×64) 204-PIN PC3-12800 DDR3 SDRAM Unbuffered SODIMM	UG25U6411N8SU-BDO-000-00	2
mSATA SSD-64G (half-size mPCIe)	SDSA5FK-064G	1
Antenna (support 3G and WiFi)	Techship 10033	2
Intel WiFi module	Intel 6300 633AN.HMWG	1
mPCIe half to full-size extender bracket	SC2MPCIEEXT0B1100P	1
3G/WiFi Mini PCIe card (half-size mPCIe) ¹	Option/GTM671W	1

1. Optional and would require a separate order



2.0 Getting Started

2.1 Introduction

Before using the development kit, verify that all the items listed in this section are received and that the development board is functioning by going through the following:

- Check the contents of the development kit
- Inspect the development board for any defects
- Power-on the development board and verify that it is functioning correctly

2.2 Before You Begin

Verify the contents of the development kit and the condition of the development board. If any of the items is missing or if the development board is damaged, contact Intel before you proceed.

2.2.1 Check the Contents of the Development Kit

The 4th Generation Intel[®] Core™ Processor with Mobile Intel[®] QM87 Chipset Development Kit contains the following items:

- 4th Generation Intel[®] Core™ Processor with Mobile Intel[®] QM87 Chipset Development Kit System
- 12V@7.5A DC Power Brick
- System Drivers + Development Kits User Guide (CD)
- Safety Flyer
- Quick Start Guide
- China RoHS Declaration
- WCL
- Intel[®] Development Vehicles Terms and Condition

2.2.2 Inspect the Development Board

To check the development board for damages, set it on an anti-static surface and inspect the development board to ensure that the components are not missing, bent, or cracked.

Warning: The development board may be damaged if it is not placed on an anti-static surface.



2.2.3 Power-on the Development Board

After you determine that the development board is free from any visible defects, power-on the development board and verify that the development board is functioning correctly using the following steps:

1. Connect the supplied DC power brick to the development board (use only the DC power brick supplied with the development kit).
2. Press the power button.
3. Press the **Del** key as the system boots to enter the BIOS setup screen.
4. Check the time, date, and configuration settings. The default settings should be sufficient for most users with the exception of Intel SpeedStep® Technology. This feature is disabled by default and can be enabled in setup.
5. Save and exit the BIOS setup.

The system will reboot and would then be ready for use.

Note: The development board can be powered down using one of the following methods:

- Use the Windows **Start** menu (or equivalent) shutdown option
- Press the power button to begin the power-down process
- If the above does not work, hold down the power button for 4 seconds to asynchronously shut down the system (not recommended)

2.3 Reference Documents

Table 3. Technical Reference Documents

Document Description	Document Number/Location
<i>Quick Start Guide for the 4th Generation Intel® Core™ Processor with Mobile Intel® QM87 Chipset Development Kit</i>	538674
<i>External Design Specification (EDS) for the 4th Generation Intel® Core™ Processor Mobile</i>	487246
<i>EDS for the Intel 8 Series/C220 Series Chipset Family Platform Controller Hub (PCH)</i>	486708
<i>Modular Board Design (MBD) Schematic and Board File for the 4th Generation Intel® Core™ Processor with Mobile Intel® QM87 Chipset Development Kit</i>	538668
<i>BIOS for the 4th Generation Intel® Core™ Processor with Mobile Intel® QM87 Chipset Development Kit</i>	538679
<i>User Guide for the Modular Board Design (MBD)</i>	538664

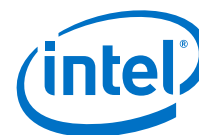


Table 4. Drivers and Utilities

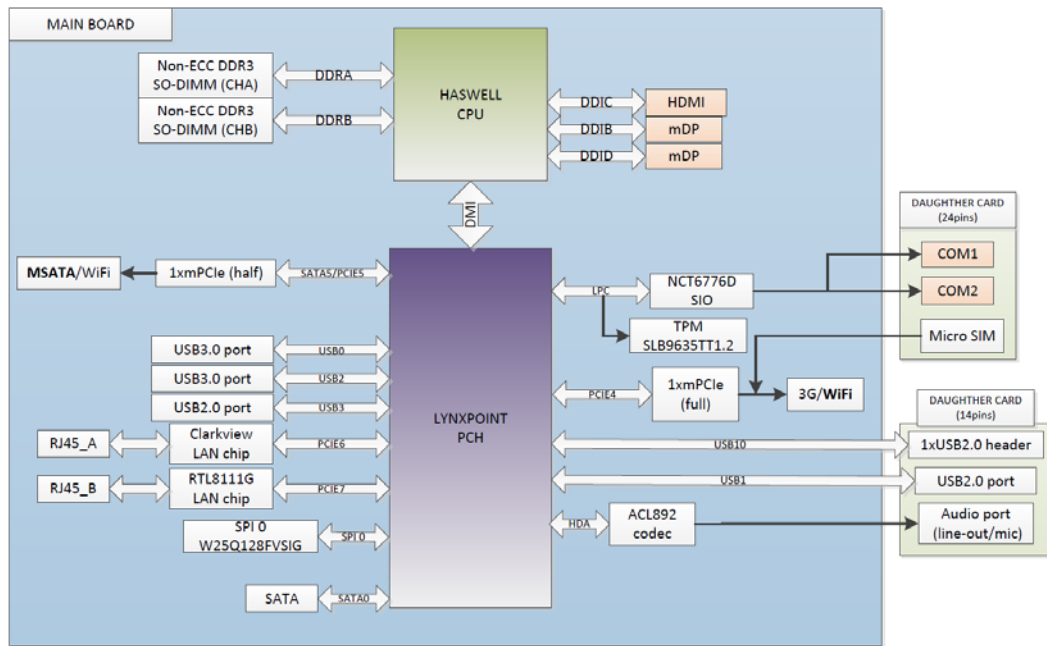
Drivers & Utilities Description	Source
Core drivers	https://platformsw.intel.com OR http://clientdownload.intel.com/SitePages/Sharkbay.aspx
Intel® Chipset.inf Driver	
Intel® HD Graphics & Audio Driver	
Intel® Wired LAN Driver (i217LM)	
Intel® USB 3.0 eXtensible Host Controller Driver	
Intel® Management Engine 9.0 (1.5MB & 5 MB SKU)	
Wireless LAN Driver (Intel 6300)	http://www.intel.com/support/wireless/wlan/sb/CS-010623.htm
Realtek Wired LAN Driver (RTL8111)	http://www.realtek.com.tw/downloads/downloadsView.aspx?Langid=1&PNid=5&PFid=5&Level=5&Conn=4&DownTypeID=3&GetDown=false#2
Realtek Audio Codec Driver (ALC892)	http://www.realtek.com.tw/downloads/downloadsView.aspx?Langid=1&PNid=24&PFid=24&Level=4&Conn=3&DownTypeID=3&GetDown=false

Note: If you have any questions please contact your Intel FAE.

3.0 Development Kit Overview

3.1 Block Diagram

Figure 1. Block Diagram of the Development Kit



3.2 Features and Specifications

Table 5. Features and Specifications (Sheet 1 of 2)

Features	Specifications	Details
CPU	Family Model Package type TDP	Haswell Mobile 4th Generation Intel® Core™ i5/i3 Processor BGA 1364 Maximum up to 37W
Memory	RAM type Maximum RAM size Maximum RAM speed RAM slot	DDR3 (1.5V) 16GB 1600MT/s 2
PCH	Family Model Package type	Lynx Point-M Mobile Intel® QM87 Chipset BGA 695
BIOS	SPI model	W25Q128FV; 128M-bit SOIC-8 serial flash memory
SIO	LPC Super SIO model	NCT6776D

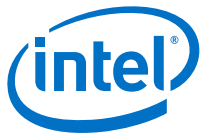


Table 5. Features and Specifications (Sheet 2 of 2)

Features	Specifications	Details
Display	Graphic type Integrated audio Maximum resolution Display option Others	Integrated Supported 3840 × 2160 @60Hz 2 × Mini DisplayPort connector 1 × Standard HDMI connector 3 Display supported
Storage	mSATA (default) HDD/SSD	Half-size Mini PCIe slot ¹ Standard SATA 3.0 connector (optional) ²
Audio	Integrated HD Audio Codec Codec model Port	Supported Realtek ALC892 1 × 3.5mm jack with line out and mic
USB	USB 3.0 USB 2.0	2 × USB 3.0 port 2 × USB 2.0 port; 1 × USB 2.0 port (header)
Network	Gigabit LAN port Intel LAN controller model 2nd LAN controller model 3G + WiFi WiFi (optional)	2 × RJ45 port Clarksville (i217-LM) with Intel® AMT support Realtek (RTL8111G) 1 × full-size Mini PCIe slot + 1 × Micro SIM slot 1 × half-size Mini PCIe slot ¹
Serial Port	COM port header	2 × RS-232 header
Power Supply	Mobile DC power brick	12V @7.5A input DC power
Others	Clocks RTC Processor VR TPM	Fully integrated clocking Battery-backed real-time clock TPS51631; Intel VR12.5 Serial VID (SVID) compliant SLB9635TT; TPM ver 1.2
System Form Factor Dimension	System Form Factor	4.6" × 7.9"
PCB Dimensions	Board Form Factor Board Z-height System Z-height PCB layer count	4.4" × 4.6" 0.53" 0.90" 10 layers

1. The half-size Mini PCIe slot can support either SATA (mSATA) or PCIe (WiFi). It is automatically detected without any extra settings. By default, the 4th Generation Intel® Core™ Processor with Mobile Intel® QM87 Chipset Development Kit uses SandDisk mSATA.

2. This feature's part is not populated on the development kit system.



3.3 Power Management States

Table 6 lists the power management states that have been defined for the platform. The Controller Link (CL) operates at various power levels called M-states.

Table 6. Power Management States Description

State	Description
G0/S0	Full on. System up and running.
G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot is not supported by the processor).
G1/S4	Suspend-to-Disk (STD). All power lost (except wakeup on PCH).
G2/S5	Soft off. All power lost (except wakeup on PCH). Total system reboot.
G3	Mechanical off. All power source (AC and battery) removed from the system.

The voltage of the development board power nets at different activity states is shown in Table 7.

Table 7. Development Board Power States

POWER NET	VOLTAGE	POWER WELL	ACTIVITY STATES
VCC12_A	12V	ALWAYS ON	S0-S5
VCC12	12V	CORE	S0
VCC5_A	5V	ALWAYS ON	S0-S5
VCC3P3_A	3.3V	ALWAYS ON	S0-S5
VCC1P05_A	1.05V	ALWAYS ON	S0-S5
VCC5	5V	CORE	S0
VCC3P3	3.3V	CORE	S0
VCC1P05	1.05V	CORE	S0
VCC3P3_M_LAN	3.3V	LAN	S0-S5
VCC3P3_M	3.3V	ME	S0-S5
VCC1P05_M	1.05V	ME	S0-S5
VCCIN	1.5-1.85V	CORE	S0
VDDQ	1.5V	DDR	S0-S3
VTT_DDR	0.75V	DDR	S0



4.0 Development Kit Setup

4.1 Introduction

This section provides the following details:

- Lists the major components and their locations on the development board, front panel and back panel
- Describes the pinouts of the headers
- Lists the LED indicator location and colors for different power states
- Provides the configuration settings for the Mobile Intel[®] QM87 Chipset

4.2 Layout of the Board, Front Panel, and Back Panel

The following figures show the development board, front panel, and back panel layout and the location of each major components.

Figure 2. Development Board Top Layer

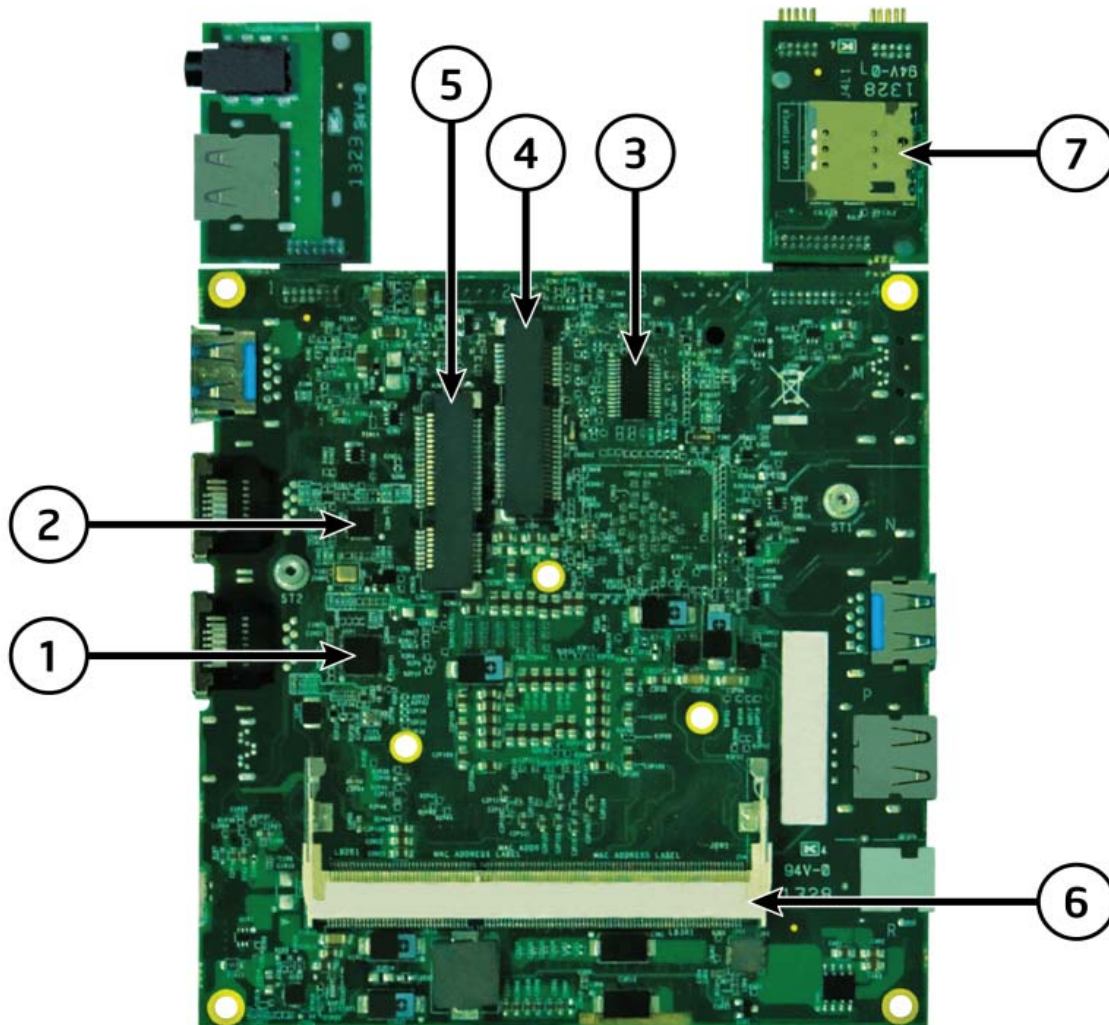


Figure 3. Development Board Bottom Layer

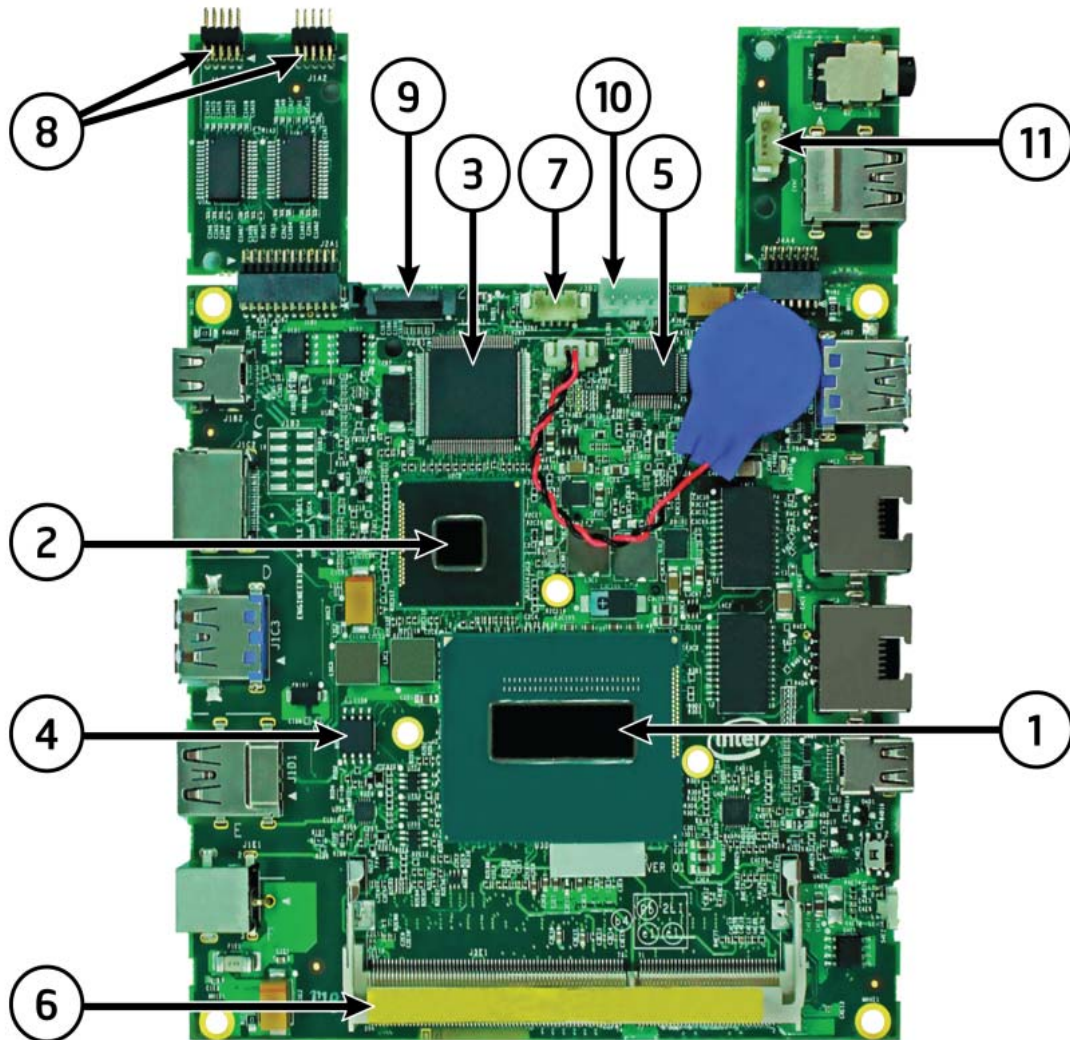


Figure 4. Front Panel

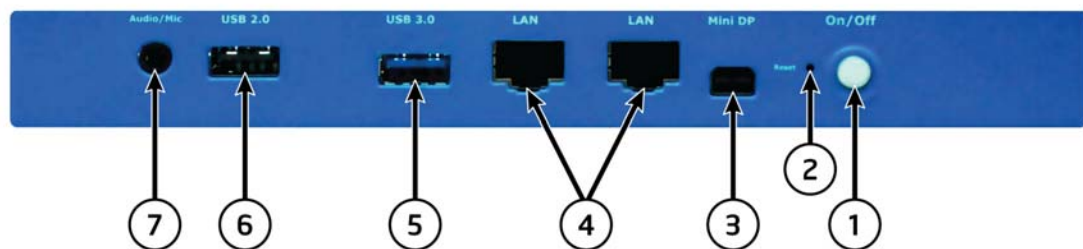
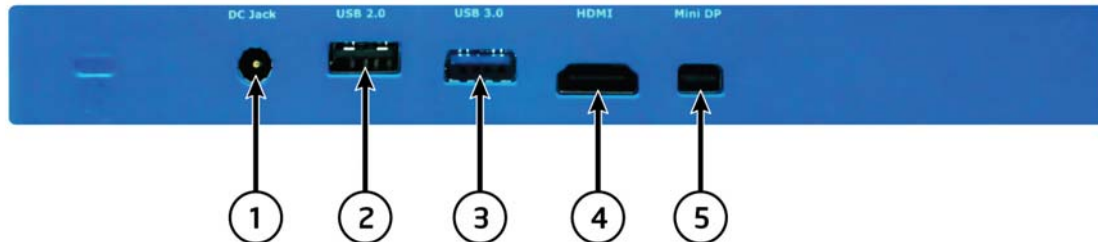


Figure 5. Back Panel



4.3 List of Components

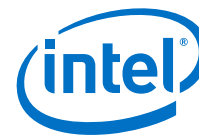
The following tables list the major components and the reference designator of the development board, front panel, and back panel.

Table 8. Development Board Top Layer

Item Number	Description	Reference Designator
1	GbE controller 1 (I127LM)	U1P1
2	GbE controller 2 (RTL8111G)	U1N1
3	TPM (SLB9635TT)	U3M1
4	Mini PCIe connector (full size)	J2M1
5	Mini PCIe connector (half size)	J2N2
6	Non-ECC DDR3 SODIMM connector (CH B)	J2R1
7	Micro SIM slot	J4L1

Table 9. Development Board Bottom Layer

Item Number	Description	Reference Designator
1	CPU (Haswell)	U3D1
2	PCH (Lynx Point)	U2C2
3	SIO (NCT6776D)	U2B1
4	SPI chip (W25Q128FV)	U1D1
5	Audio Codec (ALC892)	U3B1
6	Non-ECC DDR3 SODIMM connector (CH A)	J3E1
7	4-pin fan blower header	J3B3
8	Serial Port header (COM 1) Serial Port header (COM 2)	J1A2 J1A1
9	SATA 3.0 connector	J2B1
10	SATA power header	J3B2
11	USB 2.0 header	J4A1

**Table 10. Front Panel**

Item Number	Description	Reference Designator
1	Power button	S4E2
2	Reset button	S4E1
3	Mini DisplayPort	J4D1
4	Single LAN RJ45 connector 1 Single LAN RJ45 connector 2	J4C3 J4C2
5	USB 3.0 single connector	J4B2
6	USB 2.0 single connector	J4A3
7	Single port audio jack	J4A2

Table 11. Back Panel

Item Number	Description	Reference Designator
1	Power jack	J1E1
2	USB 2.0 single connector	J1D1
3	USB 3.0 single connector	J1C3
4	HDMI connector	J1C2
5	Mini DisplayPort connector	J1B2

4.4 Header Pinout Configuration

4.4.1 Development Board Header Pinout

The following tables list the pinout configuration for the headers, and their corresponding signal names, on the development board.

Table 12. Fan Blower Header (J3B3)

Pin	Signal Name
1	PWM
2	TACHO
3	12V
4	GND

Table 13. SATA Power Header (J3B2) — Optional

Pin	Signal Name
1	12V
2	GND
3	GND
4	5V

Note: This part is not populated in the development kit system.



Table 14. LPC Debug Header (J1B3) – Optional

Pin	Signal Name
1	LPC_AD0
2	PLTRST
3	LPC_AD1
4	LFRAME
5	LPC_AD2
6	3.3V
7	LPC_AD3
8	GND
9	CLK_33MHz
10	GND

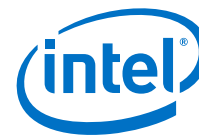
Note: This part is not populated in the development kit system. For debugging purpose only.

4.4.2 Daughter Cards Header Pinout

The following tables list the pinout configuration for the headers, and their corresponding signal names, on the daughter cards.

Table 15. Daughter Card Female Header 1 (24 Pin) (Sheet 1 of 2)

Pin	Signal Name
1	VCC5_A
2	VCC5_A
3	SIM_CLK
4	SIM_VCC
5	SIM_IO
6	SIM_RST
7	GND
8	GND
9	COM2_RTS_L
10	COM1_RI_N
11	COM2_DCD_N
12	COM1_CTS_N
13	COM2_RXD
14	COM1_RTS_N
15	COM2_TXD
16	COM1_DCD_N
17	COM2_DSR_N
18	COM1_RXD
19	COM2_DTR_N
20	COM1_TXD
21	COM2_RI_N

**Table 15. Daughter Card Female Header 1 (24 Pin) (Sheet 2 of 2)**

Pin	Signal Name
22	COM1_DSR_N
23	COM2_CTS_N
24	COM1_DTR_N

Table 16. Daughter Card Female Header 2 (14 Pin)

Pin	Signal Name
1	VCC5_USB10
2	VCC5_USB0_1
3	GND
4	FRONT_SENSE_A
5	GND
6	CONN_P_MIC1
7	GND
8	AGND
9	USB_PN10
10	CONN_P_FRONT_L
11	USB_PP10
12	CONN_P_FRONT_R
13	USB_C_PP1
14	USB_C_PN1

Table 17. Daughter Card 1 (24 Pin): Serial Port Header (RS-232)

- COM1: J1A2
- COM2: J1A1

Pin	Signal Name
1	DCD#
2	RXD
3	TXD
4	DTR#
5	GND
6	DSR#
7	RTS#
8	CTS#
9	RI#
10	NC

**Table 18. Daughter Card 2 (14 Pin): USB 2.0 Header (J4A1)**

Pin	Signal Name
1	5V
2	USB_DATA-
3	USB_DATA+
4	GND

4.5 Push-Buttons and LED Indicators

4.5.1 Power-On and Reset Buttons

The development kit system has two push-buttons: POWER and RESET. The POWER button enables or disables power to the entire development kit system causing it to boot or shut down. The RESET button forces the system to warm reset.

The locations of the POWER and RESET buttons are shown in [Table 19](#).

Table 19. Push-Buttons Location Table

Description	Reference Designator
Power button	S4E2
Reset button	S4E1

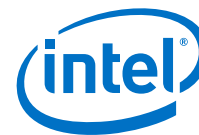
4.5.2 LED Indicators

There are two LED indicators in the development kit system: power button LED and standby LED. The power button LED is located at the POWER button (S4E2) while the standby LED is located at DS4B1.

The location, power state, and color of the LED indicators are shown in [Table 20](#).

Table 20. LED Indicators

Description	Reference Designator	Power State	Color
Standby LED	DS4B1	S4/S5	Yellow
Power button LED	S4E2	S0	Blue



4.6 Mobile Intel® QM87 Chipset Configuration Settings

4.6.1 R2B7 — Clear/Keep CMOS Settings

Clearing the contents of the CMOS and all BIOS settings will restore the development kit system to factory default values.

Note: R2B7 is open by default.

To restore the BIOS settings:

1. Turn off the development kit system and unplug the power cord.
2. Short two solder pads at R2B7 for a few seconds by using a tweezer or a blue wire (that is, connect pin 1 and pin 2), and then leave it open. Take note that these pins are not shorted by default.
3. Turn on the development kit system.

4.6.2 R2B12 — Clear/Keep ME Settings

Clearing the contents of the ME settings will restore the development kit system to factory default values.

Note: R2B12 is open by default.

To restore the ME settings:

1. Turn off the development kit system and unplug the power cord.
2. Short two solder pads at R2B12 for a few seconds by using a tweezer or a blue wire (that is, connect pin 1 and pin 2), and then leave it open. Take note that these pins are not shorted by default.
3. Turn on the development kit system.

