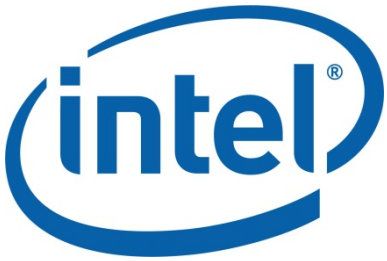

Intel® Ethernet Controller X540 Frequently Asked Questions

Networking Division (ND)

September 2013

Revision 2.6

Legal

Revisions

Date	Revision	Notes
11/03/2010	0.9	Initial Release.
1/11/2011	1.0	Pre-PRQ Release.
1/16/2012	1.2	Post-PRQ Release.
1/24/2012	1.3	Combined Technical/Design FAQ v0.8 from PAE and Intel customer support FAQ.
1/25/2012	1.31	Typo on Wake n LAN, swapped sections 2 and 3, removed PXE question.
1/27/2012	1.4	Feedback for PXE Option ROM, also rolled in PME feedback, refreshed TOC.
1/30/2012	1.5	Fixed typos in sections 2.7, 2.13, and 2.31. Revised Updated section 2.31.
1/30/2012	2.0	Initial public release.
2/2/2012	2.1	Added new minimum cable length FAQ, updated TOC
2/15/2012	2.2	Added single port branding string
3/1/2012	2.3	Corrected RFI spelling by auto correction
8/17/2012	2.4	Added NVM shared flash update note
12/14/2012	2.5	Revised sections: 2.10, 2.11, 2.25, 2.29, 2.35 and 3.9.
September 2013	2.6	Revised sections 1.2, 2.48, and 4.1.

1 Summary

This document contains a list of Technical and Design Frequently Asked Questions (FAQs) and Sales and Marketing FAQs for the Intel® Ethernet Controller X540. It consolidates two separate FAQ lists into one.

1.1 Product Branding Strings

- Intel® Ethernet Controller X540 (for software release 18.7 and beyond)
- Intel® Ethernet Controller X540-AT2 (for software release 18.6 and below)

1.2 Background

The Intel® Ethernet Controller X540 is the next generation of 10 Gb Ethernet controllers from Intel. Using a 40 nm manufacturing process, the X540 is the first 40 nm dual-port integrated Media Access Controller/Physical Layer (MAC/PHY) single chip designed for reduced power and package size that is very attractive for use as a LAN on Motherboard (LOM) network controller.

1.3 Key Messages

- 10GBASE-T is the Physical interface for 10 Gigabit Ethernet (GbE) LOM, standalone servers, and workstations – widely implemented Cat 6A cables, up to 100 m reach, and backwards compatible with existing 1 GbE infrastructure.
- The world's first fully integrated single chip 10GBASE-T Ethernet Controller specifically optimized to bring 10 GbE networking to server boards as a LOM.
- Provides industry leading features for I/O Virtualization and Storage over Ethernet.
- Low power <12.5 W, in a small package 25 x 25 mm, and is designed using the latest 40 nm PHY technology with industry leading integrated Electrical Mechanical Interference/Radio Frequency Interference (EMI/RFI) filters.
- MOW link: http://www.intel.com/cd/edesign/library/asmo-na/eng/443604.htm

1.4 Intel® Ethernet Unified Networking Principles

Intel has delivered high quality Ethernet products for over 30 years and our Unified Networking solutions are built on the original principles that made us successful in Ethernet:

- Open architecture integrates networking with the server, enabling Information Technology (IT) managers to reduce complexity and overhead while enabling a flexible and scalable data center network.
- Intelligent offloads lower cost and power while delivering the application performance that customers expect.
- Proven Ethernet unified networking is built on trusted Intel Ethernet technology, enabling customers to deploy Fiber Channel over Ethernet (FCoE) or Internet Small Computer System Interface (iSCSI) while maintaining the quality of their traditional Ethernet networks.

Intel's unified networking solutions are enabled through a combination of standard Intel® Ethernet products along with trusted network protocols integrated in the operating systems. Thus, unified networking is available on every server either through LOM implementation or

via an add-in Network Interface Card (NIC).

2 Technical and Design FAQ

The intended audience for this section is targeted for technical support and design engineers.

Note that the following FAQ entries are not listed in any particular order or priority.

2.1 Why can't I access some of these hyperlinks? How do I find all the X540 collateral?

Some collateral is only available on Intel Business Link/ Intel Business Portal (IBL/IBP), which is protected under a Non-Disclosure Agreement (NDA). Other collateral is available to the general public. Contact your Intel Field Representative for access to NDA content.

2.2 Can any magnetics, RJ-45, or MagJack be used on X540?

No. The electrical requirements for the X540 are significantly different than previous generation 1000BASE-T components. 10GBASE-T technology works at a higher frequency range than 1000BASE-T. See the latest 10GBASE-T Magnetics Specification posted on IBL/IBP for electrical and mechanical requirements.

2.3 How long does it take to enable a new RJ-45, magnetic, or MagJack?

As of this publication it takes approximately six to nine months to enable a new vendor.

2.4 Is the 5th channel required to work? What is it used for?

Yes. It's used for sensing and canceling common-mode noise. It is very similar to the receivers on typical 4 channels, with the exception that it does not have a driver and only receives.

2.5 Where can I get recommended Bill of Material (BOM) list?

The Intel® Ethernet Controller X540 Datasheet (section 13.13) lists the recommended components to use with the X540. The list contracts and expands over time even after product launch because some components end-of-life and new components are newly tested.

2.6 Can I use Cat 5e cable with X540?

Use of Cat 5e cabling for 10GBASE-T operation is not advised; however, Cat 5e can be used for operation in 100BASE-TX and 1000BASE-T modes. Throughput performance and cable distance are significantly degraded when using Cat 5e in 10GBASE-T mode.

2.7 Can I mix and match cable type and vendors?

It's not advised. The cable should be of same type and manufacturer throughout its topology to its link partner.

2.8 Can I create my own length of cables?

For 10GBASET-T operation it is advised to buy pre-made length cables from the manufacturer.

2.9 What is the cable reach for the X540?

The X540 complies with the 10GBASE-T (IEEE 802.3an) specification, supporting 55 meter reach over Category 6 (Cat 6) cabling, 100 meter reach over Augmented Category 6 (Cat 6A), and Cat 7.

2.10 What is the minimum cable length that can be used for the X540?

It's recommended to use at least a 1 meter cable in non-external loopback applications. For example, connecting Port0 to Port1 of the same X540, connecting to a link partner, connecting to a switch, etc.

2.11 Is external loopback (Tx-to-Rx on the same port of the X540) supported?

Yes. Required components to use external loopback are: v4.3 or later NVM, build 16.8 or newer LANCONF, and a A RJ-45 dongle. A Cat 5e or Cat 6A cable with a maximum length of 0.076 meters (3 inches) can also be used. Contact your Intel Field Representative for access to these tools.

2.12 What is the maximum and typical power of the X540?

SKU JLX540AT2 has a maximum power (dual ports) of 12.5 W and typical power (dual ports) of 11.5 W. For power of difference usages see the Intel® Ethernet Controller X540 Datasheet (section 12.4.1).

2.13 What power saving technologies does the X540 support?

In addition to the use of the 40 nm manufacturing process, the X540 adjusts power according to cable length. The X540 supports three power states for less than 10 meters, less than 30 meters, and over 30 meters.

2.14 What power supplies does the X540 require?

3.3V, 2.5V, 1.2V, 0.8V, and 0.67V

2.15 Which power rails are sourced from main power?

All X540 power should be derived from AUX power if designed for Wake on LAN (WoL) and Manageability.

2.16 Does the X540 require start-up and shut-down power rail requirements?

Starting with B0 stepping, power rail start-up requirements do exist. See the latest Intel® Ethernet Controller X540 Datasheet for additional details. There are currently no power-down rail requirements.

2.17 Is X540 backward pin compatible with other Ethernet controllers?

Yes. The X540 is backward compatible with two port versions of Intel's I350 1 GbE LAN controller. There is an Application Note Intel® Ethernet Controller X540 I350 Pin Compatibility – Application Note posted on IBL/IBP that is helpful.

2.18 Does Intel provide design review support?

Yes. The Intel LAN Access Division (LAD) Platform Application Engineer (PAE) group can provide schematic and Computer Aided Design (CAD) layout support. Submit your design review request through Intel Premier Support (QuAD) against the X540 product.

2.19 Does X540 support backplane applications?

Not at time of this publication.

2.20 Does the X540 support Non-Volatile Memory (NVM)-less (EEPROMless) designs?

No. The X540 requires an NVM for proper operation.

2.21 Does the X540 need to be reset after updating bits in the NVM or upgrading to a completely new NVM?

Yes. The power cord should be removed for ~20 seconds and a cold reboot needs to occur to reset the X540 and re-read the external NVM contents into its internal registers.

2.22 What speeds does the X540 support?

10 GbE, 1 GbE, and 100 Mb/s. For 100 Mb/s speed, only auto-negotiation full-duplex is supported.

2.23 Is Management Component Transport Protocol (MCTP) supported?

Not at this time. We are waiting for the DMTF standard to be release before validating and releasing support for MCTP.

2.24 Are the MAC addresses still automatically calculated like on the 82576?

No. Each MAC address must be programmed individually just like other Intel 10 GbE devices (82599 and 82598).

2.25 What are the PCI Device IDs for the X540?

The current and future Specification Update section 1.1 Product Code and Device Identification lists the device IDs.

X540 Device ID Code	Vendor ID	Device ID	Revision ID
Intel® Ethernet Controller X540-AT2	8086	1528	0
Intel® X540 Virtual Function (Mailbox Communication)	8086	1515	0
Intel® X540 Virtual Function (Microsoft* Hyper-V)	8086	1530	0

2.26 Why do I see two devices, all with the same device ID?

Each port of the X540 is considered a unique device, and has its own device ID. A device with both ports configured, will show two device IDs; both with the same value.

2.27 Can I get full bandwidth when connecting the X540 to PCI Express* (PCIe*) Gen3 x4?

No. X540 is only capable of Gen2. It is highly recommended to connect all 8 lanes to the X540 to achieve line rate on both ports.

2.28 Is there any side effect to connect the X540 to PCIe Gen2 x8 of Intel® C600 Chipset?

Connecting the X540 to the C600's PCIe interface introduces additional memory read/write latencies compared to connecting to the Ivy Bridge or Sandy Bridge PCIe interface.

2.29 Does the Intel device driver support the 1588 protocol standard?

Yes, the X540 supports the IEEE 1588 protocol standard. Currently, only Linux has operating system support and driver support for 1588 at this time. Linux kernel version 3.5 and forward have code support level for the X540. For earlier kernel versions, please use driver version 3.11.33 and later, available at:

http://sourceforge.net/projects/e1000/files/ixgbe%

2.30 Can I/O addressing be disabled in the X540?

Yes. The X540 has a disable I/O mode feature for disabling allocation of I/O port resources for use in systems and environments (such as Windows and UEFI). This is where the feature is either not desirable or not supported. Legacy environment components (such as DOS, PXE and iSCSI Boot, which previously required I/O port access) can now either use I/O mode if available or an alternate mechanism if I/O mode is disabled.

2.31 Does the X540 support pre-boot?

Yes. It supports iSCSI*, PXE* and UEFI*, and FCoE*.

2.32 Where does pre-boot (PXE, iSCSI, FCoE, UEFI) Option ROM code reside?

Option ROMs can reside in one of two areas depending on system design. For LOM designs,

typically but not always, option ROMs reside with the BIOS in the server board Flash/NVM device. For NIC designs, the option ROMs always resides in the combined Flash/NVM device attached to the X540 FLSH I/O interface. IBA Build and Boot Util are two software tools used to manage the option ROMs.

2.33 How can Original Design Manufacturer/Original Equipment Manufacturers (ODM/OEMs) upgrade the X540 NVM after production launch in the event future interoperability issues arise with new/future 10GBASE-T link partners?

LANCONF or EEUPDATE are provided tools to enable NVM updates at ODM/OEM environments. These tools are not for non-NDA customers.

2.34 Does the X540 support WoL?

Yes; however, the complete WoL solution is complex and the system design engineer needs to assure all platform stack ingredients (BIOS, power delivery, software, NVM) interacting with the X540 are implemented correctly.

2.35 Can I monitor the X540 temperature through the THERM_D1_x pins?

Yes. The THERM_D1_P and THERM_D1_N pins can be used to measure temperature. As noted in section 12.5 of the Intel® Ethernet Controller X540 Datasheet, there is a -10 °C offset from the Tj at the center of the die that needs to be comprehended. It is imperative that you have an external thermal sensor implemented in your X540 design, and that your product monitors the X540 thermal diode to ensure appropriate action by the BMC to prevent overheating problems.

2.36 What are the X540 SMBus slave addresses?

For NVM images that support SMBus manageability, SMBus addresses are defined as:

SMBus 0 Slave Address 0x63

SMBus 1 Slave Address 0x62

See NVM settings in Intel® Ethernet Controller X540 Datasheet section 6.5.5.4 titled "*SMBus Slave Address – Offset 0x03*" for additional details.

2.37 How long can the Ethernet MDI trace lengths be?

In general, the X540 Ethernet trace lengths can be up to eight inches. This is dependent upon the actual design and layout. Refer to Intel® Ethernet Controller X540 Datasheet table 13-1 "MDI Routing Summary" for additional details.

2.38 How do I interpret the chip markings on my X540?

See the section "Marking Diagram" in the Specification Update document.

2.39 Does the X540 have any Electro Static Discharge (ESD) suppression on the MDI lines?

Yes, ESD suppression is built-in.

2.40 Can the latest NVM images be used on early engineering sample A-stepping silicon?

No. Production NVM DevStarter v4.3 or newer cannot used on older si stepping A1, A3, A4, or A5. Support for older A stepping silicon has concluded.

2.41 Why is the Sample Validation Kit (SVK) not being updated?

When the X540 is production ready, the SVK ingredients are delivered to different customer downloadable locations, thus the SVK process terminates. The software tools and NVM images continue to be available on IBL/IBP as separate deliverables and the software drivers are available to public at the Intel Download center.

2.42 Where do I find the latest software driver for X540?

Intel Download center. The software drivers linked from this page are generic versions, and can be used for general purposes. However, OEMs might have altered the features, incorporated customizations, or made other changes to the software or software packaging they provide. To avoid any potential installation incompatibilities on your OEM system, Intel recommends that you check with your OEM and use the software provided via your system manufacturer. Intel or the OEM might not provide technical support for some or all issues that could arise from the usage of this generic version of software drivers

2.43 What are the clocks and operation frequencies of the X540?

X540 requires a 50 MHz crystal for its core logic and 100 MHz for its PCI logic. 10GBASE-T operating frequencies are 800 M symbol/sampling rate and ~450 MHz used bandwidth.

2.44 Does the X540 support MAC-to-MAC communication?

No. Each MAC on the X540 is independent of the other MACs. There is no MAC-to-MAC communication path.

2.45 Will the X540 function if only 4x PCIe lanes are routed to it?

Yes, the X540 complies with the PCIe specification so it runs on less than x8 lanes; however with significant throughput performance (~70%) limitations when both ports are enabled. Intel recommends using x8 lanes of PCIe for optimal X540 performance.

2.46 Where can I get technical support?

Technical support is provided by the computer vendor. You can use the following links for Intel® Desktop Board and Intel® Server Board support information.

Intel® Desktop Board support
Intel® Server Board support

Intel develops network components used in motherboards and network adapters sold by OEMs such as Dell*, HP*, Gateway*, or IBM*). Network controllers that are built into the motherboard or network adapters sold by an OEM are supported by the OEM. Intel does not provide support for OEM integrated network controllers or OEM adapters.

2.47 Where can I find product briefs, datasheets, application notes, design guides, and other resources for developers?

Product information on Intel® Ethernet Controllers

For those who have access to Electronic Design Kits (EDKs), the X540 has additional information posted in collateral listing.

Intel offers a complete line of industry-leading, single- and multi-port 10 GbE, 1 GbE, and fast Ethernet LAN controllers with integrated MAC and PHY, providing high performance, low power consumption, and a smaller footprint. Offering 10 GbE, 1 GbE, and 100 Mb/s LAN controllers, PCIe, PCI, PCI-X, or LCI bus interfaces, 16-, 32- or 64-bit architecture, Intel produces Ethernet LAN controllers that enable faster, smaller, and simpler designs.

2.48 How to update the NVM in LANCONF

When updating the shared NVM in LANCONF, make sure to select "Program Shared Flash" or "Program NVM Image" (depending on your LANCONF version), as opposed to selecting EEPROM/Flash Menu →Raw EEPROM → F4-Load From File.

The X540 uses a new concept of Shared Flash. Shared Flash is a means of storing legacy EEPROM content, as well as firmware, Option ROM, and PHY data in a single Flash component. Only a bin file (as opposed to txt, epp, or hex files) is required to update the entire Shared Flash component.

3 Sales and Marketing FAQ

The intended audience for this section is targeted for sales, marketing, and management. Note that the following FAQ entries are not listed in any particular order or priority.

3.1 When did the Intel® Ethernet Controller X540 start shipping?

The X540 started shipping in January 2012, time to market with the next-generation server platforms. The X540 was publically demonstrated at IDF 2010 running both ports at full-line rate and is now shipping as a LOM, Network Daughter Card (NDC) or PCIe adapter.

3.2 How can I purchase the Intel® Ethernet Controller X540?

Books are open for Intel® Ethernet Controller X540-AT2 – MM# 917469. Orders should be placed with an Intel® Authorized Distributor or through your Intel contact.

3.3 What is the product name?

It is marketed as the Intel® Ethernet Controller X540. Adapters from Intel are known as the Intel® Ethernet Converged Network Adapter X540. Note that 10 GbE wording is not used in the product name since the Roman numeral "X" already denotes the 10 GbE speed.

3.4 Why did the naming convention change?

The Intel Ethernet Controller X540 follows the new product naming convention that LAD products are using going forward. The new naming convention makes it easier to tell what type of product it is. The "X" is the Roman numeral for 10 denoting 10 GbE speed, likewise, if the first letter is a Roman numeral "I" it is a 1 GbE product. The next number is the series and then the version of the product. The X540 is the follow-on product and feature set in the 500 series of products. The Intel® 82599 10 GbE Ethernet Controller uses the old naming but the adapters are known as the Intel® Ethernet Converged Network Adapter X520 series.

3.5 Is there an EDK and Collateral List for the X540?

Yes, the link is Intel Networking and Comms Ethernet: Intel® Ethernet Controller X540

Note: 10GBASE-T technology introduces new and unique design challenges. LAD's Platform Application Engineering group provides services such as: schematic and layout reviews which inform and assist designers about these new challenges.

3.6 Is the X540 a Converged Network Adapter (CNA)?

The X540 supports both network and storage traffic over the same wire, including QoS features like the Data Center Bridging (DCB) suite of standards. Adapters using the X540 are branded as Intel Ethernet CNAs but the X540 does not use the term CNA in the product brand name. See FAQ "Does the X540 support FCoE?" for further details.

3.7 What is the price of the X540?

When the X540 is integrated into a server, the price is included in the price of that server. Pricing is available through Intel approved resellers, or by contacting your Intel sales contact. The list price for the Intel® Ethernet Converged Network Adapter X540 is $599.

3.8 Whose PHY is integrated?

Intel worked with a leading 10GBASE-T PHY vendor to provide the world's first dual-port integrated 10GBASE-T MAC/PHY 40 nm Ethernet controller. The X540's PHY is built to Intel specifications and fully supported by Intel.

3.9 What 10GBASE-T switches are shipping today?

10GBASE-T switches and modules are shipping from several switch vendors, including Cisco*, Extreme Networks*, Dell*, SMC Networks*, and Arista Networks*. These switches were tested for interoperability during a multi-day event in Taiwan in November 2012 where multiple X540-based server designs were tested.

3.10 Does the X540 support FCoE?

Yes, the X540 does support FCoE. We are aggressively working with switch vendors to provide FCoE support and link partners for 10GBASE-T.

3.11 Does the X540 support FCoE and iSCSI offloads?

The X540 uses stateless offloads for data path offloading that works in conjunction with the operating system native initiators to provide scalable and high performance in multiple operating systems and Hypervisors. Additionally, similar to the Intel® 82599 (Niantic), the X540 supports both FCoE and iSCSI boot. The use of stateless offload and native software initiators provides the use of the operating system and Hypervisor-based storage and bandwidth management tools, as opposed to having a fully offloaded stack that might not be compatible with management tools.

3.12 Does the X540 support Energy Efficient Ethernet (EEE)?

The X540 has not implemented EEE at this time. The overall power strategy for the X540 is to focus on overall platform power reductions taking advantage of Intel® Direct Data I/O and reducing power based on cable length.

3.13 Does the X540 support any offloads?

Yes, the X540 supports multiple stateless offloads and several different filtering and queuing technologies. For specific details see the Intel® Ethernet Controller X540 Datasheet.

3.14 What virtualization technologies does the X540 support?

The X540 supports Intel® Virtualization Technology for connectivity (Intel VT-c) delivers I/O virtualization and Quality of Service (QoS) features designed directly into the X540 controller's silicon. Intel® I/O virtualization advances network connectivity models used in today's servers to more efficient models by providing Flexible Port Partitioning (FPP), multiple Rx/Tx queues, Tx queue rate limiting and on-controller QoS functionality that can be used in both virtual and non-virtual server deployments. VMDq and the PCI-SIG Single Root I/O Virtualization and Sharing (SR-IOV) specifications support 64 virtual functions / queues per port.

3.15 What is FPP?

By taking advantage of the PCI-SIG Single Root I/O Virtualization and Sharing (SR-IOV) specification, Intel Ethernet products provide FPP. With FPP, virtual Ethernet controllers can be used directly by the Linux* host and/or assigned directly to virtual machines to provide hypervisor virtual switch by-pass. FPP enables the assignment of up to 64 Linux host processes or virtual machines per port to virtual. This enables an administrator to control the partitioning of their 10 GbE bandwidth across multiple dedicated network resources, ensuring balanced QoS by giving each assigned virtual controller equal access to 10Gbs of bandwidth.

3.16 What security technologies does the X540 support?

The X540 supports MACsec (IEEE 802.1AE) and IPSec offload with 1024 128-bit AES keys per port.

3.17 What QoS features does the X540 support?

In addition to the various I/O virtualization QoS features, the X540 supports DCB to provide traffic class prioritization with DCB: Priority Grouping (ETS); Priority Flow Control, and DCBX.

3.18 What management interfaces are on the X540?

The X540 supports SMBus and NC-SI interfaces with Operating System to Baseboard Management Controller (OS2BMC), MCTP and WoL support.

3.19 What is the OS2BMC feature on the X540?

Previously, server management software must implement a local communication method (using chipset-based registers) to interact with the local Management Controller (MC) of the platform. Intel has added a filtering method to enable the server management software to communicate with the MC via the networking interface (using standard network protocols – such as TCP/IP) rather than a chipset-specific interface

4 Other Information

4.1 Product IDs

Vendor ID	Device ID	Sub Device ID	Code Name	Media	Branding String
8086	1528	*	Twinville	Copper	Intel® Ethernet Controller X540-AT2
8086	1560	*	Twinville (using single port NVM)	Copper	Intel® Ethernet Controller X540
8086	1528	00A2	Twin Pond (OEM-Gen single port)	Copper	Intel® Ethernet Converged Network Adapter X540-T1
8086	1528	0002	Twin Pond (Retail single port)	Copper	Intel® Ethernet Converged Network Adapter X540-T1
8086	1528	0001	Twin Pond (Retail)	Copper	Intel® Ethernet Converged Network Adapter X540-T2
8086	1528	001A	Twin Pond (OEM-Gen)	Copper	Intel® Ethernet Converged Network Adapter X540-T2
8086	1515	*	N/A	Copper	Intel® X540 Virtual Function (Mailbox Communication)
8086	1530	*	N/A	Copper	Intel® X540 Virtual Function (Microsoft* Hyper-V)

4.2 Product Identifiers

Production MM#	SPEC Code	Part # Product	Top Marking
917469	SLJEJ	G30773-001	JLX540AT2