Contents

1 Introduction .................................................................................................................. 9
  1.1 References .............................................................................................................. 10
  1.2 Definition of Terms ............................................................................................. 10

2 LGA1356 Socket ......................................................................................................... 13
  2.1 Board Layout .......................................................................................................... 15
  2.2 Attachment to Motherboard ................................................................................ 16
  2.3 Socket Components ............................................................................................. 16
      2.3.1 Socket Body Housing ................................................................................... 16
      2.3.2 Solder Balls ................................................................................................. 16
      2.3.3 Contacts ........................................................................................................ 17
      2.3.4 Pick and Place Cover ................................................................................... 17
  2.4 Package Installation / Removal ............................................................................. 18
      2.4.1 Socket Standoffs and Package Seating Plane ............................................... 19
  2.5 Durability .............................................................................................................. 19
  2.6 Markings .............................................................................................................. 19
  2.7 Component Insertion Forces ............................................................................... 20
  2.8 Socket Size .......................................................................................................... 20
  2.9 LGA1356 Socket NCTF Solder Joints ..................................................................... 20

3 Independent Loading Mechanism (ILM) and Back Plate ............................................. 23
  3.1 Design Concept ...................................................................................................... 23
      3.1.1 ILM Assembly Design Overview .................................................................. 23
      3.1.2 ILM Back Plate Design Overview ............................................................... 24
      3.1.3 Durability ....................................................................................................... 24
  3.2 Assembly of ILM to a Motherboard ...................................................................... 25
  3.3 ILM Cover ............................................................................................................. 27

4 LGA1356 Socket, ILM and Back Plate Electrical, Mechanical, and Environmental
   Specifications .............................................................................................................. 29
  4.1 Component Mass .................................................................................................... 29
  4.2 Package/Socket Stackup Height ........................................................................... 29
  4.3 Socket Maximum Temperature ............................................................................ 29
  4.4 Loading Specifications ......................................................................................... 30
  4.5 Electrical Requirements ...................................................................................... 30
  4.6 Environmental Requirements .............................................................................. 31

5 Thermal Solutions ...................................................................................................... 33
  5.1 Boundary Conditions ............................................................................................ 33
  5.2 Assembly .............................................................................................................. 35
      5.2.1 Thermal Interface Material (TIM) ................................................................. 36
  5.3 Structural Considerations ..................................................................................... 36
  5.4 Thermal Design .................................................................................................... 36
      5.4.1 Thermal Characterization Parameter ........................................................... 36
  5.5 Fan Speed Control ............................................................................................... 37
      5.5.1 Fundamentals ............................................................................................. 37
  5.6 Thermal Features .................................................................................................. 37
      5.6.1 TCONTROL and DTS Relationship ............................................................ 38
      5.6.2 Short Duration TCC Activation and Catastrophic Thermal
           Management for Intel® Xeon® Processor E5-2400 Product Family ................. 39
      5.6.3 Intel® Turbo Boost Technology ................................................................... 40
  5.7 Thermal Guidance ................................................................................................ 40
      5.7.1 Thermal Excursion ....................................................................................... 40
      5.7.2 Absolute Processor Temperature ................................................................. 40
B-2  Board Keepin / Keepout Zones (Sheet 2 of 4) ......................................................... 53
B-3  Board Keepin / Keepout Zones (Sheet 3 of 4) .......................................................... 54
B-4  Board Keepin / Keepout Zones (Sheet 4 of 4) .......................................................... 55
B-5  1U Reference Heatsink Assembly (Sheet 1 of 2) ...................................................... 56
B-6  1U Reference Heatsink Assembly (Sheet 2 of 2) ...................................................... 57
B-7  1U Reference Heatsink Fin and Base (Sheet 1 of 2) .................................................. 58
B-8  1U Reference Heatsink Fin and Base (Sheet 2 of 2) .................................................. 59
B-9  Heatsink Shoulder Screw (1U, 2U and Tower) ....................................................... 60
B-10 Heatsink Compression Spring (1U, 2U and Tower) ................................................ 61
B-11 Heatsink Retaining Ring (1U, 2U and Tower) ......................................................... 62
B-12 Heatsink Load Cup (1U, 2U and Tower) ................................................................. 63
B-13 2U Collaborative Heatsink Assembly (Sheet 1 of 2) ................................................ 64
B-14 2U Collaborative Heatsink Assembly (Sheet 2 of 2) ................................................ 65
B-15 2U Collaborative Heatsink Volumetric (Sheet 1 of 2) ............................................. 66
B-16 2U Collaborative Heatsink Volumetric (Sheet 2 of 2) ............................................. 67
B-17 Tower Collaborative Heatsink Assembly (Sheet 1 of 2) .......................................... 68
B-18 Tower Collaborative Heatsink Assembly (Sheet 2 of 2) .......................................... 69
B-19 Tower Collaborative Heatsink Volumetric (Sheet 1 of 2) ....................................... 70
B-20 Tower Collaborative Heatsink Volumetric (Sheet 2 of 2) ....................................... 71
B-21 1U Reference Heatsink Assembly with TIM (Sheet 1 of 2) ...................................... 72
B-22 1U Reference Heatsink Assembly with TIM (Sheet 2 of 2) ...................................... 73
B-23 2U Reference Heatsink Assembly with TIM (Sheet 1 of 2) ..................................... 74
B-24 2U Reference Heatsink Assembly with TIM (Sheet 2 of 2) ..................................... 75
B-25 Tower Reference Heatsink Assembly with TIM (Sheet 1 of 2) ............................. 76
B-26 Tower Reference Heatsink Assembly with TIM (Sheet 2 of 2) ............................. 77
B-27 25.5 mm Reference Heatsink Assembly (Sheet 1 of 2) ......................................... 78
B-28 25.5 mm Reference Heatsink Assembly (Sheet 2 of 2) ......................................... 79
B-29 25.5 mm Reference Heatsink Fin and Base (Sheet 1 of 2) ..................................... 80
B-30 25.5 mm Reference Heatsink Fin and Base (Sheet 2 of 2) ..................................... 81
B-31 25.5 mm Reference Heatsink Assembly with TIM (Sheet 1 of 2) ......................... 82
B-32 25.5 mm Reference Heatsink Assembly with TIM (Sheet 2 of 2) ......................... 83
C-1  Socket Mechanical Drawing (Sheet 1 of 4) ............................................................ 86
C-2  Socket Mechanical Drawing (Sheet 2 of 4) ............................................................ 87
C-3  Socket Mechanical Drawing (Sheet 3 of 4) ............................................................ 88
C-4  Socket Mechanical Drawing (Sheet 4 of 4) ............................................................ 89
D-1  Processor Installation Tool ..................................................................................... 92
E-1  ATCA Heatsink Performance Curves ..................................................................... 94
E-2  NEBS Thermal Profile .......................................................................................... 95
E-3  ATCA Reference Heat Sink Assembly (Sheet 1 of 2) ............................................. 97
E-4  ATCA Reference Heat Sink Assembly (Sheet 2 of 2) ............................................. 98
E-5  ATCA Reference Heatsink Fin and Base (Sheet 1 of 2) ......................................... 99
E-6  ATCA Reference Heatsink Fin and Base (Sheet 2 of 2) ......................................... 100

Tables

1-1  Reference Documents .......................................................................................... 10
1-2  Terms and Descriptions ..................................................................................... 10
4-1  Component Mass ............................................................................................... 29
4-2  1356-land Package and LGA1356 Socket Stackup Height ...................................... 29
4-3  Socket and ILM Mechanical Specifications ......................................................... 30
4-4  Electrical Requirements for LGA1356 Socket .................................................... 31
5-1  Values Used to Generate Processor Thermal Specifications ............................... 33
5-2  Performance Expectations in Compact Electronics Bay (CEB) ......................... 34
Revision History

<table>
<thead>
<tr>
<th>Document Number</th>
<th>Revision Number</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>327250</td>
<td>-001</td>
<td>Initial release of the document.</td>
<td>May 2012</td>
</tr>
</tbody>
</table>
1 Introduction

This document provides guidelines for the design of thermal and mechanical solutions for server and workstation processors in the Intel® Xeon® Processor E5-2400 Product Family platform. The processors covered include those listed in the Intel® Xeon® Processor E5-2400 Product Family Datasheet - Volume One. The components described in this document include:

- The processor thermal solution (heatsink) and associated retention hardware.
- The LGA1356 socket, the Independent Loading Mechanism (ILM) and back plate.

Figure 1-1. Intel® Xeon® Processor E5-2400 Product Family Platform Socket Stack

The goals of this document are:

- To assist board and system thermal mechanical designers.
- To assist designers and suppliers of processor heatsinks.

Thermal profiles and other processor specifications are provided in the appropriate Datasheet.
1.1 References

Material and concepts available in the following documents may be beneficial when reading this document.

Table 1-1. Reference Documents

<table>
<thead>
<tr>
<th>Document</th>
<th>Number</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>European Blue Angel Recycling Standards</td>
<td></td>
<td>2</td>
</tr>
<tr>
<td>Intel® Xeon® Processor E5-2400 Product Family Datasheet - Volume One</td>
<td>327248</td>
<td>1</td>
</tr>
<tr>
<td>Platform Environment Control Interface (PECI) Specification</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td>Intel® Xeon® Processor E5-2400 Processor Product Family Mechanical Model</td>
<td>327322</td>
<td>1</td>
</tr>
<tr>
<td>Intel® Xeon® Processor E5-2400 Processor Product Family Thermal Model</td>
<td>327321</td>
<td>1</td>
</tr>
<tr>
<td>Manufacturing With Intel Components Using Lead-Free Technology</td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>Platform Digital Thermal Sensor (DTS) Based Thermal Specifications and Overview</td>
<td></td>
<td>4</td>
</tr>
</tbody>
</table>

Notes:
4. Contact your local Intel Field Sales Representative.

1.2 Definition of Terms

Table 1-2. Terms and Descriptions (Sheet 1 of 2)

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bypass</td>
<td>Bypass is the area between a passive heatsink and any object that can act to form a duct. For this example, it can be expressed as a dimension away from the outside dimension of the fins to the nearest surface.</td>
</tr>
<tr>
<td>DTS</td>
<td>Digital Thermal Sensor reports a relative die temperature as an offset from TCC activation temperature.</td>
</tr>
<tr>
<td>FSC</td>
<td>Fan Speed Control</td>
</tr>
<tr>
<td>IHS</td>
<td>Integrated Heat Spreader: a component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.</td>
</tr>
<tr>
<td>ILM</td>
<td>Independent Loading Mechanism provides the force needed to seat the 1356-LGA land package onto the socket contacts.</td>
</tr>
<tr>
<td>LGA1356 socket</td>
<td>The processor mates with the system board through this surface mount, 1356-contact socket.</td>
</tr>
<tr>
<td>PECI</td>
<td>The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices.</td>
</tr>
<tr>
<td>$\Psi_{CA}$</td>
<td>Case-to-ambient thermal characterization parameter (psi). A measure of thermal solution performance using total package power. Defined as $(T_{CASE} - T_{LA}) / Total Package Power$. Heat source should always be specified for $\Psi$ measurements.</td>
</tr>
<tr>
<td>$\Psi_{CS}$</td>
<td>Case-to-sink thermal characterization parameter. A measure of thermal interface material performance using total package power. Defined as $(T_{CASE} - T_{S}) / Total Package Power$.</td>
</tr>
<tr>
<td>$\Psi_{SA}$</td>
<td>Sink-to-ambient thermal characterization parameter. A measure of heatsink thermal performance using total package power. Defined as $(T_{S} - T_{LA}) / Total Package Power$.</td>
</tr>
</tbody>
</table>
### Table 1-2. Terms and Descriptions (Sheet 2 of 2)

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>T\text{CASE}</td>
<td>The case temperature of the processor measured at the geometric center of the topside of the IHS.</td>
</tr>
<tr>
<td>T\text{CASE_MAX}</td>
<td>The maximum case temperature as specified in a component specification.</td>
</tr>
<tr>
<td>T\text{C}</td>
<td>Thermal Control Circuit: Thermal monitor uses the TCC to reduce the die temperature by using clock modulation and/or operating frequency and input voltage adjustment when the die temperature is very near its operating limits.</td>
</tr>
<tr>
<td>T\text{CONTROL}</td>
<td>T\text{CONTROL} is a static value below TCC activation used as a trigger point for fan speed control.</td>
</tr>
<tr>
<td>T\text{D}</td>
<td>Thermal Design Power: Thermal solution should be designed to dissipate this target power level. TDP is not the maximum power that the processor can dissipate.</td>
</tr>
<tr>
<td>Thermal Monitor</td>
<td>A power reduction feature designed to decrease temperature after the processor has reached its maximum operating temperature.</td>
</tr>
<tr>
<td>Thermal Profile</td>
<td>Line that defines the temperature specification of a processor at a given power level.</td>
</tr>
<tr>
<td>TIM</td>
<td>Thermal Interface Material: The thermally conductive compound between the heatsink and the processor case. This material fills the air gaps and voids, and enhances the transfer of the heat from the processor case to the heatsink.</td>
</tr>
<tr>
<td>T\text{LA}</td>
<td>The measured ambient temperature locally surrounding the processor. The ambient temperature should be measured just upstream of a passive heatsink or at the fan inlet for an active heatsink.</td>
</tr>
<tr>
<td>T\text{SA}</td>
<td>The system ambient air temperature external to a system chassis. This temperature is usually measured at the chassis air inlets.</td>
</tr>
<tr>
<td>U</td>
<td>A unit of measure used to define server rack spacing height. 1U is equal to 1.75 in, 2U equals 3.50 in, etc.</td>
</tr>
</tbody>
</table>
This chapter describes a surface mount, LGA (Land Grid Array) socket intended for processors in the E5-2400 Product Family Platform. The socket provides I/O, power and ground contacts. The socket contains 1356 contacts arrayed about a cavity in the center of the socket with lead-free solder balls for surface mounting on the motherboard.

The socket has 1356 contacts with 1.016 mm X 1.016 mm pitch (X by Y) in a 43x41 grid array with 21x17 grid depopulation in the center of the array and selective depopulation elsewhere.

The socket must be compatible with the package (processor) and the Independent Loading Mechanism (ILM). The design includes a back plate which is a key contributor in producing a uniform load on the socket solder joints. Socket loading specifications are listed in Section 4.4.

**Figure 2-1.** LGA1356 Socket with Pick and Place Cover Removed
Figure 2-2. LGA1356 Socket Contact Numbering (Top View of Socket)
2.1 Board Layout

The land pattern for the LGA1356 socket is 40 mils X 40 mils (X by Y). Note that there is no round-off (conversion) error between socket pitch (1.016 mm) and board pitch (40 mil) as these values are equivalent.

In general, metal defined (MD) pads perform better than solder mask defined (SMD) pads under thermal cycling, and SMD pads perform better than MD pads under dynamic stress. At this time, complete recommendations for pad definition and pad size do not exist for the LGA1356 socket. See Section 2.9 for more information on pad definition and pad size.

Figure 2-3. LGA1356 Socket Land Pattern (Top View of Board)
2.2 **Attachment to Motherboard**

The socket is attached to the motherboard by 1356 solder balls. There are no additional external methods (that is, screw, extra solder, adhesive, and so on) to attach the socket.

As indicated in Figure 2-4, the Independent Loading Mechanism (ILM) is not present during the attach (reflow) process.

![Figure 2-4. Attachment to Motherboard](image)

2.3 **Socket Components**

The socket has two main components, the socket body and Pick and Place (PnP) cover, and is delivered as a single integral assembly. Refer to Appendix C for detailed drawings.

2.3.1 **Socket Body Housing**

The housing material is thermoplastic or equivalent with UL 94 V-0 flame rating capable of withstanding 260 °C for 40 seconds (typical reflow/rework). The socket coefficient of thermal expansion (in the XY plane), and creep properties, must be such that the integrity of the socket is maintained for the conditions listed in the LGA1366 Socket Validation Reports, and the LGA1356 Addendum.

The color of the housing will be dark as compared to the solder balls to provide the contrast needed for pick and place vision systems.

2.3.2 **Solder Balls**

A total of 1356 solder balls corresponding to the contacts are on the bottom of the socket for surface mounting with the motherboard.

The socket has the following solder ball material:

- Lead free SAC (SnAgCu) solder alloy with a silver (Ag) content between 3% and 4% and a melting temperature of approximately 217 °C. The alloy must be
compatible with immersion silver (ImAg) motherboard surface finish and a SAC alloy solder paste.

The co-planarity (profile) and true position requirements are defined in Appendix C.

### 2.3.3 Contacts

Base material for the contacts is high strength copper alloy.

For the area on socket contacts where processor lands will mate, there is a 0.381 μm [15 μinches] minimum gold plating over 1.27 μm [50 μinches] minimum nickel underplate.

No contamination by solder in the contact area is allowed during solder reflow.

### 2.3.4 Pick and Place Cover

The cover provides a planar surface for vacuum pick up used to place components in the Surface Mount Technology (SMT) manufacturing line. The cover remains on the socket during reflow to help prevent contamination during reflow. The cover can withstand 260 °C for 40 seconds (typical reflow/rework profile) and the conditions listed in the LGA1366 Socket Validation Reports, and LGA1356 Addendum, without degrading. Reports are available from socket suppliers listed in Appendix A.

As indicated in Figure 2-5, the Pick and Place cover remains on the socket during ILM installation. Use of the ILM cover can mitigate against bent socket contacts associated with reinstalling the Pick and Place cover. A cover should remain on whenever possible to help prevent damage to the socket contacts. See Section 3.2 and Section 3.3 for additional information on the ILM cover.

Pick and Place cover retention must be sufficient to support the socket weight during lifting, translation, and placement (board manufacturing), and during board and system shipping and handling.

Pick and Place covers are designed to be interchangeable between socket suppliers. As indicated in Figure 2-5, a Pin1 indicator on the Pick and Place cover provides a visual reference for proper orientation with the socket.

**Figure 2-5. Pick and Place Cover**
2.4 Package Installation / Removal

As indicated in Figure 2-6, access is provided to facilitate manual installation and removal of the package.

To assist in package orientation and alignment with the socket:

- The package Pin1 triangle and the socket Pin1 chamfer provide visual reference for proper orientation.

- The package substrate has orientation notches along two opposing edges of the package, offset from the centerline. The socket has two corresponding orientation posts to physically prevent mis-orientation of the package. These orientation features also provide initial rough alignment of package to socket.

- As shown in Figure 2-7, the package substrate has a “-2” mark near the orientation notch on the Pin 1 side. Similarly, space has been reserved for a “-2” mark on the motherboard in the Board Keepin / Keepout Zones in Figure B-1 and Figure B-2. These matching marks help prevent system assemblers from installing the incorrect processor into the socket.

- The socket has alignment walls at the four corners to provide final alignment of the package.

See Appendix D for information regarding a tool designed to provide mechanical assistance during processor installation and removal.

Figure 2-6. Package Installation / Removal Features
2.4.1 Socket Standoffs and Package Seating Plane

Standoffs on the bottom of the socket base establish the minimum socket height after solder reflow and are specified in Appendix C.

Similarly, a seating plane on the topside of the socket establishes the minimum package height. See Section 3.2 for the calculated IHS height above the motherboard.

2.5 Durability

The socket must withstand 30 cycles of processor insertion and removal. The max chain contact resistance from Table 4-4 must be met when mated in the 1st and 30th cycles.

The socket Pick and Place cover must withstand 15 cycles of insertion and removal.

2.6 Markings

There are three markings on the socket:

- LGA1356: Font type is Helvetica Bold - minimum 6 point (2.125 mm).
- Manufacturer's insignia (font size at supplier's discretion).
- Lot identification code (allows traceability of manufacturing date and location).

All markings must withstand 260 °C for 40 seconds (typical reflow/rework profile) without degrading, and must be visible after the socket is mounted on the motherboard.

LGA1356 and the manufacturer's insignia are molded or laser marked on the side wall.
2.7 Component Insertion Forces

Any actuation must meet or exceed SEMI S8-95 Safety Guidelines for Ergonomics/Human Factors Engineering of Semiconductor Manufacturing Equipment, example Table R2-7 (Maximum Grip Forces). The socket must be designed so that it requires no force to insert the package into the socket.

2.8 Socket Size

Socket information needed for motherboard design is given in Appendix C.

This information should be used in conjunction with the reference motherboard keepout drawings provided in Appendix B to ensure compatibility with the reference thermal mechanical components.

2.9 LGA1356 Socket NCTF Solder Joints

Intel has defined selected solder joints of the socket as non-critical to function (NCTF) for post environmental testing. The processor signals at NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality. Figure 2-8 identifies the NCTF solder joints.

Since corner pads are often more susceptible to solder joint damage, NCTF locations are often placed in the corners. When possible, larger pads may be chosen at NCTF locations to further mitigate against solder joint damage. At this time, complete recommendations for pad definition and pad size do not exist at NCTF locations. CTF and NCTF locations are 18mil solder mask defined on Intel reference designs.
Figure 2-8. LGA1356 NCTF Solder Joints
3 Independent Loading Mechanism (ILM) and Back Plate

The Independent Loading Mechanism (ILM) provides the force needed to seat the 1356-LGA land package onto the socket contacts. The ILM is physically separate from the socket body. The assembly of the ILM to the board is expected to occur after wave solder. The exact assembly location is dependent on manufacturing preference and test flow.

*Note:* The ILM has two critical functions: deliver the force to seat the processor onto the socket contacts and distribute the resulting compressive load evenly through the socket solder joints.

*Note:* The mechanical design of the ILM is a key contributor to the overall functionality of the LGA1356 socket. Intel performs detailed studies on integration of processor package, socket and ILM as a system. These studies directly impact the design of the ILM. The Intel reference ILM will be “build to print” from Intel controlled drawings. Intel recommends using the Intel Reference ILM. Custom non-Intel ILM designs do not benefit from Intel’s detailed studies and may not incorporate critical design parameters.

3.1 Design Concept

The ILM and back plate are assemblies and can be procured from the enabled vendors.

3.1.1 ILM Assembly Design Overview

The ILM assembly consists of four major pieces: load lever, load plate, frame and the captive fasteners.

The load lever and load plate are stainless steel. The frame and fasteners are high carbon steel with appropriate plating. The fasteners are fabricated from a high carbon steel. The frame provides the hinge locations for the load lever and load plate.

The ILM assembly design ensures that once assembled to the back plate and the load lever is closed, the only features touching the board are the captive fasteners. The nominal gap of the frame to the board is ~1 mm when the load plate is closed on the empty socket or when closed on the processor package.

When closed, the load plate applies two point loads onto the IHS at the “dimpled” features shown in Figure 3-1. The reaction force from closing the load plate is transmitted to the frame and through the captive fasteners to the back plate. Some of the load is passed through the socket body to the board inducing a slight compression on the solder joints.
3.1.2 ILM Back Plate Design Overview

The unified back plate consists of a flat steel back plate with threaded studs for ILM attach, and internally threaded nuts for heatsink attach. The threaded studs have a smooth surface feature that provides alignment for the back plate to the motherboard for proper assembly of the ILM around the socket. A clearance hole is located at the center of the plate to allow access to test points and backside capacitors. An additional cut-out on two sides provides clearance for backside voltage regulator components. An insulator is pre-applied. To stay within the temperature limit of the insulator, remove the back plate prior to board component rework.

3.1.3 Durability

The ILM durability requirement is 30 processor cycles. 1 processor cycle = install processor, close load plate, latch load lever, unlatch load lever, open load plate.

The ILM durability requirement is 6 assembly cycles. See Section 3.2 for assembly procedure. 1 assembly cycle = fasten the ILM assembly to the back plate with the four captive screws, torque to 9 ± 1 inch-pounds, unfasten ILM assembly from the back plate.
3.2 Assembly of ILM to a Motherboard

The ILM design allows a bottoms up assembly of the components to the board. In step 1 (see Figure 3-3), the back plate is placed in a fixture. Holes in the motherboard provide alignment to the threaded studs.

In step 2, the ILM assembly is placed over the socket and threaded studs. The Intel Reference Design ILM cover is not designed to nest over the Pick and Place cover. This feature helps prevent reinstallation of the Pick and Place cover, a step that can lead to socket bent contacts.

To prevent the ILM cover from popping off during ILM assembly, the load plate can be unlatched from the load lever when the fasteners are torqued as shown is Step 3. Using a T20 Torx® driver, fasten the ILM assembly to the back plate with the four captive fasteners. Torque to 9 ± 1 inch-pounds.

The Pick and Place cover can then be removed as shown in Step 4, and the load plate can then closed and latched as shown in Step 5.

The length of the threaded studs accommodate board thicknesses from 0.062” to 0.100”.
Figure 3-3. ILM Assembly

Step 1: With socket body reflowed on board, and back plate in fixture, align board holes to back plate studs.

Step 2: With back plate against bottom of board, align ILM assembly to back plate studs.

Step 3

Step 4

Step 5
As indicated in Figure 3-4, socket protrusion and ILM key features prevent 180-degree rotation of ILM assembly with respect to the socket. The result is a specific Pin 1 orientation with respect to the ILM lever.

**Figure 3-4. Pin1 and ILM Lever**

---

### 3.3 ILM Cover

As indicated in Table A-4, ILM covers are available as discrete components and pre-assembled to the ILM load plate.

The ILM cover will interfere with a processor and pop off if the ILM is closed with a processor in the socket.

The ILM cover is designed to be interchangeable between different suppliers validated by Intel. Performance of the pop off feature may decline if the ILM cover supplier is different than the ILM supplier. The ILM cover can be removed manually if the pop off feature is not desirable, or not functional.

The ILM cover has UL94 V-0 flammability rating.

The ILM cover durability requirement is 20 cycles (1 cycle = install and remove).
4 LGA1356 Socket, ILM and Back Plate Electrical, Mechanical, and Environmental Specifications

This chapter describes the electrical, mechanical, and environmental specifications for the LGA1356 socket, Independent Loading Mechanism and Back Plate.

4.1 Component Mass

Table 4-1. Component Mass

<table>
<thead>
<tr>
<th>Component</th>
<th>Mass</th>
</tr>
</thead>
<tbody>
<tr>
<td>Socket Body, Contacts and PnP Cover</td>
<td>15 gm</td>
</tr>
<tr>
<td>ILM Assembly</td>
<td>43 gm</td>
</tr>
<tr>
<td>Back Plate</td>
<td>100 gm</td>
</tr>
</tbody>
</table>

4.2 Package/Socket Stackup Height

Table 4-2 provides the stackup height of a processor in the 1356-land LGA package and LGA1356 socket with the ILM closed and the processor fully seated in the socket.

Table 4-2. 1356-land Package and LGA1356 Socket Stackup Height

| Integrated Stackup Height (mm) From Top of Board to Top of IHS | 7.753 ± 0.262 mm |

Notes:
1. This data is provided for information only, and is derived from: (a) the height of the socket seating plane above the motherboard after reflow, given in Appendix C, (b) the height of the package, from the package seating plane to the top of the IHS, and accounting for its nominal variation and tolerances that are given in the corresponding processor EDS and expected values for the follow-on processor.
2. This value is a RSS calculation.

4.3 Socket Maximum Temperature

The power dissipated within the socket is a function of the current at the pin level and the effective pin resistance. To ensure socket long term reliability, Intel defines socket maximum temperature using a via on the underside of the motherboard. Exceeding the temperature guidance may result in socket body deformation, or increases in thermal and electrical resistance which can cause a thermal runaway and eventual electrical failure. The guidance for socket maximum temperature is listed below:

- Via temperature under socket < 96 °C
4.4 Loading Specifications

The socket will be tested against the conditions listed in the LGA1366 Socket Validation Reports, and LGA1356 Addendum, with heatsink, ILM and back plate attached, under the loading conditions outlined in this chapter.

Table 4-3 provides load specifications for the LGA1356 socket with the ILM and back plate installed. The maximum limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Exceeding these limits during test may result in component failure. The socket body should not be used as a mechanical reference or load-bearing surface for thermal solutions.

Table 4-3. Socket and ILM Mechanical Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static compressive load from ILM to processor</td>
<td>445 N [100 lbf]</td>
<td>623 N [140 lbf]</td>
<td>3, 4</td>
</tr>
<tr>
<td>IHS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Solution Static Compressive Load</td>
<td>0 N [0 lbf]</td>
<td>266 N [60 lbf]</td>
<td>1, 2, 3</td>
</tr>
<tr>
<td>Total Static Compressive Load (ILM plus Heatsink)</td>
<td>445 N (100 lbf)</td>
<td>890 N (200 lbf)</td>
<td>3, 4</td>
</tr>
<tr>
<td>Dynamic Compressive Load (with heatsink installed)</td>
<td>N/A</td>
<td>890 N (200 lbf)</td>
<td>1, 3, 5, 6</td>
</tr>
<tr>
<td>Target Pick and Place Cover allowable removal force</td>
<td>N/A</td>
<td>4.45 - 6.68 N [1.0 - 1.5 lbf]</td>
<td></td>
</tr>
<tr>
<td>Load Lever actuation force</td>
<td>N/A</td>
<td>38.3 N [8.6 lbf] in the vertical direction 10.2 N [2.3 lbf] in the lateral direction.</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
2. This is the minimum and maximum static force that can be applied by the heatsink and its retention solution to maintain the heatsink to IHS interface. This does not imply the Intel reference TIM is validated to these limits. TIM load range is documented in Section 5.2 for the Intel Reference Design.
3. Loading limits are for the LGA1356 socket.
4. This minimum limit defines the compressive force required to electrically seat the processor onto the socket contacts.
5. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
6. Test condition used a heatsink mass of 550 gm [1.21 lb] with 50 g acceleration measured at heatsink mass. The dynamic portion of this specification in the product application can have flexibility in specific values, but the ultimate product of mass times acceleration should not exceed this dynamic load.

4.5 Electrical Requirements

LGA1356 socket electrical requirements are measured from the socket-seating plane of the processor to the component side of the socket PCB to which it is attached. All specifications are maximum values (unless otherwise stated) for a single socket contact, but includes effects of adjacent contacts where indicated.
Table 4-4. **Electrical Requirements for LGA1356 Socket**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mated loop inductance, Loop</td>
<td>&lt;3.9 nH</td>
<td>The inductance calculated for two contacts, considering one forward conductor and one return conductor. These values must be satisfied at the worst-case height of the socket.</td>
</tr>
<tr>
<td>Maximum mutual capacitance, C.</td>
<td>&lt;1 pF</td>
<td>The capacitance between two contacts</td>
</tr>
<tr>
<td>Socket Average Contact Resistance (EOL)</td>
<td>15.2 mΩ</td>
<td>The socket average contact resistance target is derived from average of every chain contact resistance for each part used in testing, with a chain contact resistance defined as the resistance of each chain minus resistance of shorting bars divided by number of lands in the daisy chain. The specification listed is at room temperature and has to be satisfied at all time. <strong>Socket Contact Resistance</strong>: The resistance of the socket contact, solderball, and interface resistance to the interposer land.</td>
</tr>
<tr>
<td>Max Individual Contact Resistance (EOL)</td>
<td>≤ 100 mΩ</td>
<td>The specification listed is at room temperature and has to be satisfied at all time. <strong>Socket Contact Resistance</strong>: The resistance of the socket contact, solderball, and interface resistance to the interposer land; gaps included.</td>
</tr>
<tr>
<td>Bulk Resistance Increase</td>
<td>≤ 3 mΩ</td>
<td>The bulk resistance increase per contact from 24 °C to 107 °C</td>
</tr>
<tr>
<td>Dielectric Withstand Voltage</td>
<td>360 Volts RMS</td>
<td></td>
</tr>
<tr>
<td>Insulation Resistance</td>
<td>800 MΩ</td>
<td></td>
</tr>
</tbody>
</table>

### 4.6 Environmental Requirements

The reliability targets in this chapter are based on the expected field use environment for these products. The test sequence for the LGA1356 socket was developed using the knowledge-based reliability evaluation methodology, which is acceleration factor dependent. A simplified process flow of this methodology can be seen in Figure 4-1. Since the LGA1356 socket is very similar to the LGA1366 socket, the LGA1356 socket is expected to perform similarly and full validation for the LGA1356 socket is avoided.
A detailed description of this methodology can be found at:

This section describes a 1U reference heatsink and thermal design guidelines for the Intel® Xeon® Processor E5-2400 Product Family.

5.1 Boundary Conditions

Table 5-1 provides values for boundary conditions and performance targets used to generate processor thermal specifications and to provide guidance for heatsink design.

### Table 5-1. Values Used to Generate Processor Thermal Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Altitude, system ambient temp</td>
<td>Sea level, 35°C</td>
</tr>
<tr>
<td>TDP</td>
<td>50W (4-core)</td>
</tr>
<tr>
<td></td>
<td>60W</td>
</tr>
<tr>
<td></td>
<td>70W</td>
</tr>
<tr>
<td></td>
<td>80W (4-core)</td>
</tr>
<tr>
<td></td>
<td>95W</td>
</tr>
<tr>
<td></td>
<td>80W (2-core, 1 socket)</td>
</tr>
<tr>
<td>$\Psi_{CA}^1$</td>
<td>0.312°C/W</td>
</tr>
<tr>
<td></td>
<td>0.296°C/W</td>
</tr>
<tr>
<td></td>
<td>0.296°C/W</td>
</tr>
<tr>
<td></td>
<td>0.315°C/W</td>
</tr>
<tr>
<td></td>
<td>0.296°C/W (8-core),</td>
</tr>
<tr>
<td></td>
<td>0.298°C/W (6-core)</td>
</tr>
<tr>
<td></td>
<td>0.285°C/W</td>
</tr>
<tr>
<td>$T_{LA}^2$</td>
<td>49°C</td>
</tr>
<tr>
<td></td>
<td>48.1°C</td>
</tr>
<tr>
<td>Airflow $^3$</td>
<td>9.7 CFM @ 0.23” dP</td>
</tr>
<tr>
<td></td>
<td>13 CFM @ 0.28” dP</td>
</tr>
<tr>
<td>System height (form factor)</td>
<td>1U (EEB)$^4$</td>
</tr>
<tr>
<td></td>
<td>1U (non-specific, 1-socket)</td>
</tr>
<tr>
<td>Heatsink volumetric$^5$</td>
<td>90 x 90 x 25.5 mm (1U/SSI blade)$^6$</td>
</tr>
<tr>
<td>Heatsink technology$^7$</td>
<td>Cu base, Al fins</td>
</tr>
</tbody>
</table>

**Notes:**
1. Max target (mean + 3 sigma + offset) for thermal characterization parameter (Section 5.4.1).
2. Local ambient temperature of the air entering the heatsink.
3. Airflow through the heatsink fins with zero bypass. Max target for pressure drop (dP) measured in inches H2O.
4. Reference system configuration. Processor is downstream from memory in EEB (Entry-Level Electronics Bay).
5. Dimensions of heatsink do not include socket or processor.
6. Heatsink height + socket/processor height (Table 4-2) complies with TEB 1U Rack Height Constraints (36 mm) in EEB Specification 2011, and with Maximum Component Height (33.5 mm) in SSI Compute Blade Specification, both at http://www.ssiforum.org.
7. Passive heatsinks. PCM45F thermal interface material.

Table 5-2 provides approximate boundary conditions and approximate performance expectations in Compact Electronics Bay. These values are not used to generate processor thermal specifications, but may provide guidance for heatsink design.

### Table 5-2. Performance Expectations in Compact Electronics Bay (CEB)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Altitude, system ambient temp</td>
<td>Sea level, 35°C</td>
</tr>
<tr>
<td>TDP</td>
<td>50W</td>
</tr>
<tr>
<td></td>
<td>60W</td>
</tr>
<tr>
<td></td>
<td>70W</td>
</tr>
<tr>
<td></td>
<td>80W (4-core)</td>
</tr>
<tr>
<td></td>
<td>95W</td>
</tr>
<tr>
<td>$T_{LA}^1$</td>
<td>43.7°C</td>
</tr>
<tr>
<td></td>
<td>45.6°C</td>
</tr>
<tr>
<td></td>
<td>46.8°C</td>
</tr>
<tr>
<td></td>
<td>48.1°C</td>
</tr>
<tr>
<td></td>
<td>50.0°C (8-core), 46.6°C (6-core)</td>
</tr>
</tbody>
</table>
Table 5-2. Performance Expectations in Compact Electronics Bay (CEB)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Psi_{CA}^2$</td>
<td>0.273°C/W 0.265°C/W 0.264°C/W 0.278°C/W 0.265°C/W (8-core), 0.269°C/W (6-core)</td>
</tr>
<tr>
<td>Airflow</td>
<td>13 CFM @ 0.32&quot; dP</td>
</tr>
<tr>
<td>System height (form factor)</td>
<td>1U (CEB)</td>
</tr>
<tr>
<td>Heatsink volumetric</td>
<td>90 x 90 x 25.5 mm (1U/SSI blade)</td>
</tr>
<tr>
<td>Heatsink technology</td>
<td>Cu base, Al fins</td>
</tr>
</tbody>
</table>

Notes:
1. Local ambient temperature of the air entering the heatsink.
2. Max target (mean + 3 sigma + offset) for thermal characterization parameter (Section 5.4.1).
3. Airflow through the heatsink fins with zero bypass. Max target for pressure drop (dP) measured in inches H2O.
4. Reference system configuration. Processor is downstream from processor in CEB (Compact Electronics Bay). With the values above, the 25.5mm tall heatsink can meet the processor thermal specifications in Intel's Reference Design 10.5x12 inches CEB board. However, these CEB values are not used to generate processor thermal specifications. Ducting is utilized to direct airflow.
5. Dimensions of heatsink do not include socket or processor.
6. Heatsink height + socket/processor height (Table 4-2) complies with TEB 1U Rack Height Constraints (36 mm) in EEB Specification 2011, and with Maximum Component Height (33.5 mm) in SSI Compute Blade Specification, both at http://www.ssiforum.org.
7. Passive heatsinks. PCM45F thermal interface material.

Table 5-1 and Table 5-2 specify $\Psi_{CA}$ and pressure drop targets for specific airflows. To determine $\Psi_{CA}$ and pressure drop targets for other airflows, use Best-fit equations in Figure 5-1. Heatsink detailed drawings are in Appendix A.

Figure 5-1. Best-fit Equations

\[
\Psi_{CA} = \alpha + \beta \cdot (\text{CFM})^\gamma
\]

\[
\Delta P = a_{\text{quad}} \cdot (\text{CFM})^2 + b_{\text{linear}} \cdot (\text{CFM})
\]
5.2 Assembly

The assembly process for the 1U reference heatsink begins with application of Honeywell PCM45F thermal interface material to improve conduction from the IHS. Tape and roll format is recommended. Pad size is 35 x 35 mm, thickness is 0.25 mm.

Next, position the heatsink such that the heatsink fins are parallel to system airflow. While lowering the heatsink onto the IHS, align the four captive screws of the heatsink to the four threaded nuts of the back plate.

Using a #2 Phillips driver, torque the four captive screws to 8 inch-pounds. Fastener sequencing, in other words starting the threads on all four screws before torquing, may mitigate against cross threading.

This assembly process is designed to produce a static load of 39 - 51 lbf, for 0.062" - 0.100" board thickness respectively. Honeywell PCM45F is expected to meet the performance targets in Table 5-1 and Table 5-2 from 30 - 60 lbf. From Table 4-3, the Heatsink Static Compressive Load of 0 - 60 lbf allows for designs that vary from the 1U reference heatsink. Example: A customer's unique heatsink with very little static load (as little as 0 lbf) is acceptable from a socket loading perspective as long as the thermal specifications are met.

Compliance to Board Keepout Zones in Appendix A is assumed for this assembly process.
5.2.1 Thermal Interface Material (TIM)

TIM should be verified to be within its recommended shelf life before use.

Surfaces should be free of foreign materials prior to application of TIM.

Use isopropyl alcohol and a lint free cloth to remove old TIM before applying new TIM.

5.3 Structural Considerations

Target mass of heatsinks should not exceed 500 gm.

From Table 4-3, the Dynamic Compressive Load of 200 lbf max allows for designs that exceed 500 gm as long as the mathematical product does not exceed 200 lbf. Example: A heatsink of 2-lb mass (908 gm) x 50 g (acceleration) x 2.0 Dynamic Amplification Factor = 200 lbf. The Total Static Compressive Load (Table 4-3) should also be considered in dynamic assessments.

Direct contact between back plate and chassis pan will help minimize board deflection during shock. Placement of board-to-chassis mounting holes also impacts board deflection and resultant socket solder ball stress. Customers need to assess shock for their designs as their heatsink retention (back plate), heatsink mass and chassis mounting holes may vary.

5.4 Thermal Design

5.4.1 Thermal Characterization Parameter

The case-to-local ambient Thermal Characterization Parameter ($\Psi_{CA}$) is defined by:

Equation 5-1. $\Psi_{CA} = (T_{CASE} - T_{LA}) / TDP$

Where:

- $T_{CASE}$ = Processor case temperature (°C). For $T_{CASE}$ specification see the appropriate External Design Specification (EDS).
- $T_{LA}$ = Local ambient temperature in chassis at processor (°C).
- $TDP$ = TDP (W) assumes all power dissipates through the integrated heat spreader. This inexact assumption is convenient for heatsink design. TTVs are often used to dissipate TDP. Correction offsets account for differences in temperature distribution between processor and TTV.

Equation 5-2. $\Psi_{CA} = \Psi_{CS} + \Psi_{SA}$

Where:

- $\Psi_{CS}$ = Thermal characterization parameter of the TIM (°C/W) is dependent on the thermal conductivity and thickness of the TIM.
- $\Psi_{SA}$ = Thermal characterization parameter from heatsink-to-local ambient (°C/W) is dependent on the thermal conductivity and geometry of the heatsink and dependent on the air velocity through the heatsink fins.

Figure 5-3 illustrates the thermal characterization parameters.
5.5 Fan Speed Control

5.5.1 Fundamentals

In server platforms, processors often share airflow provided by system fans with other system components such as chipset, memory and hard drives. As such, the thermal control features in chipset, memory and other components not covered in this document, should influence system fan speed control to reduce fan power consumption and help systems meet acoustic targets.

The addition of thermal sensors placed in the system (for example, on front panel or motherboard) to augment internal device sensors (for example, in processor, chipset and memory) will improve the ability to implement need-based fan speed control. The placement of system sensors in cooling zones, where each zone has dedicated fan(s), can improve the ability to tune fan speed control for optimal performance and/or acoustics.

System events such as fan or power supply failure, device events such as TCC Activation or THERMTRIP, and maintenance events such as hot swap time allowance, need to be comprehended to implement appropriate fan speed control to prevent undesirable performance or loss of data. For more information on device events and features see the appropriate processor Datasheet.

Tcontrol and its upper and lower limits defined by hysteresis, can be used to avoid fan speed oscillation and undesirable noise variations.

5.6 Thermal Features

More information regarding processor thermal features is contained in the appropriate datasheet.
5.6.1 **T\textsubscript{CONTROL} and DTS Relationship**

Improved acoustics and lower fan power can be achieved by understanding the T\textsubscript{CONTROL} and DTS relationship, and implementing fan speed control accordingly.

### Table 5-3. T\textsubscript{CONTROL} and DTS Relationship

<table>
<thead>
<tr>
<th>Condition</th>
<th>Fan Speed Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \text{DTS} \leq T_{\text{CONTROL}} )</td>
<td>Adjust fan speed to maintain ( \text{DTS} \leq T_{\text{CONTROL}} ).</td>
</tr>
<tr>
<td>( \text{DTS} &gt; T_{\text{CONTROL}} )</td>
<td>Adjust fan speed to keep ( \text{T_{CASE}} ) at or below the ( \text{T_{CASE}} ) based thermal profile in the EDS, or adjust fan speed to keep DTS at or below the DTS based thermal profile in the EDS.</td>
</tr>
</tbody>
</table>

#### 5.6.1.1 Sign Convention and Temperature Filtering

Digital Thermal Sensor (DTS) and Tcontrol are relative die temperatures offset below the Thermal Control Circuit (TCC) activation temperature. As such, negative sign conventions are understood. While DTS and Tcontrol are available over PECI and MSR, use of these values in fan speed control algorithms requires close attention to sign convention. See Table 5-4 for the sign convention of various sources.

### Table 5-4. Sign Convention

<table>
<thead>
<tr>
<th>MSR (BWG)</th>
<th>PECI (EDS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DTS (+) using PACKAGE_THERM_STATUS (22:16, Digital Readout)</td>
<td>(-) using GetTemp()</td>
</tr>
<tr>
<td>T\textsubscript{CONTROL} (+) using TEMPERATURE_TARGET (15:8, Temperature Control Offset)</td>
<td>(+) using Temperature Target Read from RdPkgConfig()</td>
</tr>
</tbody>
</table>

Where a positive (+) sign convention is shown in Table 5-4, no sign bit is actually assigned, so writers of firmware code may mistakenly assign a positive sign convention in firmware equations. As appropriate, a negative sign should be introduced.

Where a negative (-) sign convention is shown in Table 5-4, a sign bit is assigned, so firmware code will read a negative sign convention in firmware equations, as desired.

DTS obtained thru MSR (PACKAGE\_THERM\_STATUS) is an instantaneous value. As such, temperature readings over short time intervals may vary considerably using this MSR. For this reason, DTS obtained thru PECI GetTemp() may be preferred since temperature filtering will provide the thermal trend.

#### 5.6.1.2 Tcontrol Relief

Factory configured T\textsubscript{CONTROL} values are available in the appropriate Dear Customer Letter or may be extracted by issuing a Mailbox or an RDMSR instruction. See the appropriate External Design Specification (EDS) for more information.

Due to increased thermal headroom based on thermal characterization on the latest processors, customers have the option to reduce T\textsubscript{CONTROL} to values lower than the factory configured values.

In some situations, use of T\textsubscript{CONTROL} Relief can reduce average fan power and improve acoustics. There are no plans to change Intel's specification or the factory configured T\textsubscript{CONTROL} values on individual processors.
To implement this relief, customers must re-write code to set $T_{\text{CONTROL}}$ to the reduced values provided in the table below. Implementation is optional. Alternately, the factory configured $T_{\text{CONTROL}}$ values can still be used, or some value between factory configured and Relief. Regardless of $T_{\text{CONTROL}}$ values used, BIOS needs to identify the processor type.

### Table 5-5. $T_{\text{CONTROL}}$ Relief for Intel® Xeon® Processor E5-2400 Product Family

<table>
<thead>
<tr>
<th>TDP, # Core</th>
<th>$T_{\text{CONTROL}}$ Relief</th>
<th>Max Core Frequency</th>
<th>Factory Configured</th>
</tr>
</thead>
<tbody>
<tr>
<td>95W 8C</td>
<td>-6</td>
<td>2.30 GHz or lower</td>
<td>-10</td>
</tr>
<tr>
<td>95W 6C</td>
<td>-6</td>
<td>2.40 GHz or lower</td>
<td>-10</td>
</tr>
<tr>
<td>70W 8C</td>
<td>-6</td>
<td>1.80 GHz or lower</td>
<td>-10</td>
</tr>
<tr>
<td>60W 6C</td>
<td>-6</td>
<td>2.00 GHz or lower</td>
<td>-10</td>
</tr>
<tr>
<td>80W 4C</td>
<td>-6</td>
<td>2.20 GHz or lower</td>
<td>-10</td>
</tr>
<tr>
<td>80W 2C, 1S</td>
<td>-6</td>
<td>2.80 GHz or lower</td>
<td>-10</td>
</tr>
</tbody>
</table>

In some cases, use of Tcontrol Relief as the trigger point for fan speed control may result in excessive TCC activation. To avoid this, the adjusted trigger point for fan speed control (FSC) is defined as:

$$T_{\text{control FSC}} = -T_{\text{CONTROL}} + T_{\text{control offset}}$$

$T_{\text{control offset}}$ must be chosen such that $T_{\text{control FSC}} < T_{\text{control Relief}}$. As such, $T_{\text{control FSC}}$ is an earlier trigger point for fan speed control, as compared to $T_{\text{control Relief}}$, and can be interpreted as overcooling. When overcooling to $T_{\text{control FSC}}$, margin as defined in Section 5.8.3 and Section 5.8.6 can be ignored. As compared to cooling to Tcontrol Relief, overcooling to $T_{\text{control FSC}}$:

- May increase frequency benefit from Intel TBT as defined in Section 5.6.3.
- Will increase acoustics
- May result in lower wall power

Customers must characterize a $T_{\text{control offset}}$ value for their system to meet their goals for frequency, acoustics and wall power.

### 5.6.2 Short Duration TCC Activation and Catastrophic Thermal Management for Intel® Xeon® Processor E5-2400 Product Family

Systems designed to meet thermal capacity may encounter short durations of throttling, also known as TCC activation, especially when running non-steady processor stress applications. This is acceptable and is functionally within the intended temperature control parameters of the processor. Such short duration TCC activation is not expected to provide noticeable reductions in application performance, and is typically within the normal range of processor to processor performance variation. Normal amounts of TCC activation occur at PECI values less than -0.25. Such occurrences may cause utilities or operating systems to issue error log.

$$\text{PECI} = -0.25$$

PECI command GetTemp() can be used to obtain non-integer PECI values.
5.6.3 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology (Intel® TBT), available on certain processor SKUs, opportunistically, and automatically, allows the processor to run faster than the marked frequency if the part is operating below its power, temperature and current limits.

Heatsink performance (lower $\Psi_{CA}$ as described in Section 5.4.1) is one of several factors that can impact the amount of Intel TBT frequency benefit. Intel TBT performance is also constrained by ICC, and VCC limits.

Increased IMON accuracy may provide more Intel TBT benefit on TDP limited applications, as compared to lower $\Psi_{CA}$, as temperature is not typically the limiter for these workloads.

With Intel TBT enabled, the processor may run more consistently at higher power levels (but still within TDP), and be more likely to operate above $T_{CONTROL}$, as compared to when Intel TBT is disabled. This may result in higher acoustics.

5.7 Thermal Guidance

5.7.1 Thermal Excursion

Under fan failure or other anomalous thermal excursions, Tcase may exceed the thermal profile for a duration totaling less than 360 hours per year without affecting long term reliability (life) of the processor. For more typical thermal excursions, Thermal Monitor is expected to control the processor power level as long as conditions do not allow the Tcase to exceed the temperature at which Thermal Control Circuit (TCC) activation initially occurred. Under more severe anomalous thermal excursions when the processor temperature cannot be controlled at or below this Tcase level by TCC activation, then data integrity is not assured. At some higher threshold, THERMTRIP_N will enable a shut down in an attempt to prevent permanent damage to the processor. Thermal Test Vehicle (TTV) may be used to check anomalous thermal excursion compliance by ensuring that the processor Tcase value, as measured on the TTV, does not exceed Tcase_max at the anomalous power level for the environmental condition of interest. This anomalous power level is equal to 75% of the Thermal Design Power (TDP) limit.

This guidance can be applied to 95W, 80W, 70W, 60W Standard or Basic SKUs in the Intel® Xeon® Processor E5-2400 Product Family.

5.7.2 Absolute Processor Temperature

Intel does not test any third party software that reports absolute processor temperature. As such, Intel cannot recommend the use of software that claims this capability. Since there is part-to-part variation in the TCC (thermal control circuit) activation temperature, use of software that reports absolute temperature can be misleading.

See the appropriate Datasheet for details regarding use of TEMPERATURE_TARGET register to determine the minimum absolute temperature at which the TCC will be activated and PROCHOT# will be asserted.
5.8  DTS Based Thermal Specification

5.8.1  Compliance to Tcase Based Thermal Profile

Processor heatsink design must still comply with the Tcase based thermal profile provided in the Intel® Xeon® Processor E5-2400 Product Family Datasheet - Volume One. Heatsink design compliance can be determined with thermocouple and TTV as with previous processors.

The heat sink is sized to comply with the Tcase based thermal profile. Customers have an option to either follow processor based Tcase spec or follow the DTS based thermal specification. In some situations, implementation of DTS based thermal specification can reduce average fan power and improve acoustics as compared to the Tcase based thermal profile.

When all cores are active, a properly sized heatsink will be able to meet the DTS based thermal specification. When all cores are not active or when Intel Turbo Boost Technology is active, attempting to comply with the DTS based thermal specification may drive system fans to maximum speed. In such situations, the Tcase temperature will be below the TCASE based thermal profile by design.

5.8.2  Considerations for Follow-on Processor

The follow-on processor in the platform will have new capabilities as compared to the Intel® Xeon® Processor E5-2400 Product Family. For example, the follow-on processor has a new Package Configuration Space (PCS) command to read margin (M) from the processor: RdPkgConfig(), Index 10. For the Intel® Xeon® Processor E5-2400 Product Family, margin (M) must be calculated in firmware.

In the following sections, implementation details specified for the Intel® Xeon® Processor E5-2400 Product Family can also be used for the follow-on processor.

For more information regarding the differences between the follow-on processor and the Intel® Xeon® Processor E5-2400 Product Family see Platform Digital Thermal Sensor (DTS) Based Thermal Specifications and Overview.

5.8.3  DTS Based Thermal Profile, Tcontrol and Margin for the Intel® Xeon® Processor E5-2400 Product Family

The calculation of the DTS based thermal specification is based on both Tcontrol and the DTS Based Thermal Profile ($T_{DTS}$):

$$T_{DTS} = \min[T_{LA} + \Psi_{pa} \times P \times F, T_{TARGET \_23:16} - T_{cc \_Offset}]$$

Where $T_{LA}$ and $\Psi_{pa}$ are the intercept and slope terms from the $T_{DTS}$ equations in the appropriate External Design Specification (EDS). To implement the DTS based thermal specification, these equations must be programmed in firmware. Since the equations differ with processor SKU, SKUs can be identified by TDP, Core Count and a profile identifier (CSR bits). For associated commands, see Platform Digital Thermal Sensor (DTS) Based Thermal Specifications and Overview.

Power (P) is calculated in Section 5.8.4. As power dynamically changes, the specification also changes, so power and $T_{DTS}$ calculations are recommended every 1 second.

Correction factor (F) compensates for the error in power monitoring. The current estimate for F is 0.95.
The Tcontrol portion of the DTS based thermal specification is a one time calculation:

\[ T_{\text{control\_spec}} = \text{TEMPERATURE\_TARGET}[23:16] - T_{\text{control}} + T_{\text{control\_offset}} \]

Tcontrol is defined in Section 5.6.1.1. Tcontrol_offset is defined in Section 5.6.1.2.

The final DTS based thermal specification is the maximum of both:

\[ T_{\text{DTS\_max}} = \max\{T_{\text{control\_spec}}, T_{\text{DTS}}\} \]

The margin (M) between the actual die temperature and the DTS based thermal specification is used in the fan speed control algorithm. When M < 0, increase fan speed. When M ≥ 0, fan speed may decrease.

\[ M = T_{\text{DTS\_max}} - T_{\text{sensor}} \]

OR

\[ M = T_{\text{DTS\_ave}} - T_{\text{sensor}} \]

Tsensor represents the absolute temperature of the processor as power changes:

\[ T_{\text{sensor}} = \text{TEMPERATURE\_TARGET}[23:16] + DTS \]

T_{\text{DTS\_ave}} is defined in Section 5.8.5.

TEMPERATURE\_TARGET [23:16], the temperature at which the processor thermal control circuit activates, is a one time PECI readout: RdPkgConfig(), Temperature Target Read, 23:16.

DTS, the relative temperature from thermal control circuit activation, is negative by definition, and changes instantaneously. DTS command info is given in Section 5.6.1.1.

### 5.8.4 Power Calculation for the Intel® Xeon® Processor E5-2400 Product Family

To implement DTS based thermal specification, average power over time must be calculated:

\[ P = \frac{(E2 - E1)}{(t2 - t1)} \]

Where:

\[ t1 = \text{time stamp 1} \]
\[ t2 = \text{time stamp 2} \]
\[ E1 = \text{Energy readout at time t1} \]
\[ E2 = \text{Energy readout at time t2} \]

The recommended time interval between energy readings is 1 second. This helps ensure the power calculation is accurate by making the error between time stamps small as compared to the duration between time stamps.

For details regarding energy readings, see *Platform Digital Thermal Sensor (DTS) Based Thermal Specifications and Overview*.

### 5.8.5 Averaging the DTS Based Thermal Specification for the Intel® Xeon® Processor E5-2400 Product Family

Averaging the DTS Based Thermal Specification helps keep the rate of change of the temperature specification on the same scale as the actual processor temperature, and helps avoid rapid changes in fan speed when power changes rapidly.
An exponential average of the specification can be calculated using a two time constant model:

\[ T_{DTS_f} = \alpha_f \times DT \times T_{DTS\_max} + T_{DTS_f\_previous} \times (1 - \alpha_f \times DT) \]
\[ T_{DTS_s} = \alpha_s \times DT \times T_{DTS\_max} + T_{DTS_s\_previous} \times (1 - \alpha_s \times DT) \]
\[ T_{DTS\_ave} = C \times T_{DTS_f} + (1-C) \times T_{DTS_s} \]

Where:
- \( T_{DTS\_max} \) is the instantaneous spec
- \( T_{DTS_f} \) and \( T_{DTS_s} \) are the fast and slow time averages
- \( T_{DTS\_ave} \) is the final two time constant average specification
- \( \alpha_f \) and \( \alpha_s \) are the time constant coefficients
- \( C \) is a scale factor
- \( DT \) is the scan rate and is recommended to be approximately 1 second

Table 5-6 below shows the coefficients recommended for averaging. These values may change per processor SKU. Customers should tune these coefficients based on their thermal solutions.

<table>
<thead>
<tr>
<th>Heatsink Performance</th>
<th>( \alpha_f ) (1/s)</th>
<th>( \alpha_s ) (1/s)</th>
<th>C</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>1.0</td>
<td>0.04</td>
<td>0.30</td>
<td>based on typical processor</td>
</tr>
<tr>
<td>Medium</td>
<td>1.0</td>
<td>0.07</td>
<td>0.30</td>
<td>based on typical processor</td>
</tr>
<tr>
<td>High</td>
<td>1.0</td>
<td>0.10</td>
<td>0.40</td>
<td>based on typical processor</td>
</tr>
</tbody>
</table>

### 5.8.6 Capabilities for the Follow-on Processor

For the follow-on processor, the intercept and slope terms from the \( T_{DTS} \) equations (\( T_{LA}, \Psi_{pa} \)), as defined in Section 5.8.3, are stored in the processor. This allows margin (M) to be reported by the processor. The PECI command for margin (M) will be RdPkgConfig(), Index 10.

- \( M < 0 \); gap to spec, fan speed must increase
- \( M \geq 0 \); margin to spec, fan speed may decrease

Use of RdPkgConfig(), Index 10 with the Intel® Xeon® Processor E5-2400 Product Family will return an illegal command.

For the follow-on processor, coefficients (\( \alpha_f, \alpha_s \)), scale factor (C) and correction factor (F) will be factory configured.

§
6 Quality and Reliability Requirements

6.1 Test Conditions
Test Conditions, Qualification and Visual Criteria vary by customer.

Socket Test Conditions are provided in the LGA1366 Socket Validation Reports, and LGA1356 Addendum and are available from socket suppliers listed in Appendix A.

6.2 Intel Reference Component Validation
Intel tests reference components both individually and as an assembly on mechanical test boards, and assesses performance to the envelopes specified in previous sections by varying boundary conditions.

While component validation shows that a reference design is tenable for a limited range of conditions, customers need to assess their specific boundary conditions and perform reliability testing based on their use conditions.

Intel reference components are also used in board functional tests to assess performance for specific conditions.

6.2.1 Board Functional Test Sequence
Each test sequence should start with components (baseboard, heatsink assembly, and so on) that have not been previously submitted to any reliability testing.

The test sequence should always start with a visual inspection after assembly and BIOS/Processor/memory test. The stress test should be then followed by a visual inspection and then BIOS/Processor/memory test.

6.2.2 Post-Test Pass Criteria
The post-test pass criteria are:
1. No significant physical damage to the heatsink and retention hardware.
2. Heatsink remains seated and its bottom remains mated flat against the IHS surface. No visible gap between the heatsink base and processor IHS. No visible tilt of the heatsink with respect to the retention hardware.
3. No signs of physical damage on baseboard surface due to impact of heatsink.
4. No visible physical damage to the processor package.
5. Successful BIOS/Processor/memory test.
6. Thermal compliance testing to demonstrate that the case temperature specification can be met.
6.2.3 **Recommended BIOS/Processor/Memory Test Procedures**

This test is to ensure proper operation of the product before and after environmental stresses, with the thermal mechanical enabling components assembled. The test shall be conducted on a fully operational baseboard that has not been exposed to any battery of tests prior to the test being considered.

The testing setup should include the following components, properly assembled and/or connected:

- Appropriate system baseboard.
- Processor and memory.
- All enabling components, including socket and thermal solution parts.

The pass criterion is that the system under test shall successfully complete the checking of BIOS, basic processor functions and memory, without any errors.

6.3 **Material and Recycling Requirements**

Material shall be resistant to fungal growth. Examples of non-resistant materials include cellulose materials, animal and vegetable based adhesives, grease, oils, and many hydrocarbons. Synthetic materials such as PVC formulations, certain polyurethane compositions (for example, polyester and some polyethers), plastics which contain organic fillers of laminating materials, paints, and varnishes also are susceptible to fungal growth. If materials are not fungal growth resistant, then MIL-STD-810E, Method 508.4 must be performed to determine material performance.

Any plastic component exceeding 25 gm should be recyclable per the European Blue Angel recycling standards.

The following definitions apply to the use of the terms lead-free, Pb-free, and RoHS compliant.

**Lead-free and Pb-free:** Lead has not been intentionally added, but lead may still exist as an impurity below 1000 ppm.

**RoHS compliant:** Lead and other materials banned in RoHS Directive are either (1) below all applicable substance thresholds as proposed by the EU or (2) an approved/pending exemption applies.

**Note:** RoHS implementation details are not fully defined and may change.

§
A Component Suppliers

Various suppliers have developed support components for processors in the Intel® Xeon® Processor E5-2400 Product Family-based platform. These suppliers and components are listed as a convenience to customers. Intel does not guarantee quality, reliability, functionality or compatibility of these components. The supplier list and/or the components may be subject to change without notice. Customers are responsible for the thermal, mechanical, and environmental verification of the components with the supplier.

A.1 Intel Enabled Supplier Information

Performance targets for heatsinks are described in Section 5.1. Mechanical drawings are provided in Appendix A. Mechanical models are listed in Table 1-1. Heatsinks assemble to server back plate Table A-4.

A.1.1 Intel Reference Thermal Solution

Customers can purchase the Intel reference thermal solutions from the suppliers listed in Table A-1.

<table>
<thead>
<tr>
<th>Assembly, Heat Sink, Intel Xeon processor E5-2400 product family, 1U</th>
<th>Component</th>
<th>Description</th>
<th>Supplier PN</th>
<th>Supplier Contact Info</th>
</tr>
</thead>
<tbody>
<tr>
<td>1U URS Intel Reference Heatsink p/n E32409-001</td>
<td>27 mm 1U Aluminum Fin, Copper Base, includes TIM, capable up to 95W</td>
<td>Fujikura HSA-8078 Rev A</td>
<td>Fujikura America Yuji Yasuda <a href="mailto:yuji@fujikura.com">yuji@fujikura.com</a> 408-748-6991</td>
<td></td>
</tr>
<tr>
<td>1U URS SSI Blade Reference Heatsink p/n E39069-001 refers to E22056 Rev 02 + Snap Cover</td>
<td>25.5 mm 1U Aluminum Fin, Copper Base, includes TIM and Snap Cover, capable up to 95W</td>
<td>Fujikura HSA-8083C</td>
<td>Fujikura Taiwan Branch Yao-Hsien Huang <a href="mailto:yeohsien@fujikuratw.com.tw">yeohsien@fujikuratw.com.tw</a> 886(2)8788-4959</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Thermal Interface Material</td>
<td>Honeywell PCM45F</td>
<td>Honeywell International, Inc. Judy Oles (Customer Service) <a href="mailto:Judy.Oles@Honeywell.com">Judy.Oles@Honeywell.com</a> 509-252-8605 Andrew S.K. Ho (APAC) <a href="mailto:andrew.ho@honeywell.com">andrew.ho@honeywell.com</a> (852) 9095-4593 Andy Delano (Technical) <a href="mailto:Andrew.Delano@Honeywell.com">Andrew.Delano@Honeywell.com</a> 509-252-2224</td>
<td></td>
</tr>
</tbody>
</table>

A.1.2 Intel Collaboration Thermal Solution

Customers can purchase the Intel collaboration thermal solutions from the suppliers listed in Table A-2.
A.1.3 Alternative Thermal Solution

Customers can purchase the alternative thermal solutions from the suppliers listed in Table A-3.

| Assembly, Heatsink, Intel Xeon processor E5-2400 product family, 2U | 2U URS Heatsink | Supplier Designed Solution with Intel-specified retention, includes TIM, up to 95W capable | Foxconn PN 1A016500 | Ray Wang
| Assembly, Heatsink, Intel Xeon processor E5-2400 product family, Pedestal | Tower URS Heatsink | Supplier Designed Solution with Intel-specified retention, includes TIM, up to 95W capable | Chaun-Choung Technology Corp (CCI) PN 0007029401 | Monica Chih

Table A-3. Suppliers for the Alternative Thermal Solution  (Sheet 1 of 3)

| Assembly, Heat Sink, 1U | 1U SSI Blade (25.5mm) Alternative URS Heatsink | Standard | TaiSol Corporation 1A1-9031000960-A www.Taisol.com | not capable for 80W (2-core, 1 socket); capable for all other SKUs up to 95W |
| Assembly, Heat Sink, 1U | 1U SSI Blade (25.5mm) Alternative URS Heatsink | Standard | Thermaltake CL-P0484 www.Thermaltake.com | not capable for 80W (2-core, 1 socket); capable for all other SKUs up to 95W |
## Table A-3. Suppliers for the Alternative Thermal Solution (Sheet 2 of 3)

<table>
<thead>
<tr>
<th>Assembly</th>
<th>Component</th>
<th>Description</th>
<th>Supplier PN</th>
<th>Thermal Capability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assembly, Heatsink, 1U</td>
<td>Standard</td>
<td>Heatsink, 1U</td>
<td>CoolerMaster S1N-PJFCS-07-GP <a href="http://www.CoolerMaster.com">www.CoolerMaster.com</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td></td>
<td>Standard</td>
<td></td>
<td>Aavid Thermalloy 050073 <a href="http://www.AavidThermalloy.com">www.AavidThermalloy.com</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td></td>
<td>Performance</td>
<td></td>
<td>Aavid Thermalloy 050231 <a href="http://www.AavidThermalloy.com">www.AavidThermalloy.com</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td></td>
<td>Performance</td>
<td></td>
<td>Aavid Thermalloy 050232 <a href="http://www.AavidThermalloy.com">www.AavidThermalloy.com</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td></td>
<td>Standard</td>
<td></td>
<td>CoolJag JYC0B39CTA <a href="http://www.CoolJag.com">www.CoolJag.com</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td></td>
<td>Performance</td>
<td></td>
<td>Taiwan Microloops 99-520040-M03 <a href="http://www.Microloops.com">www.Microloops.com</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td></td>
<td>Performance</td>
<td></td>
<td>Asia Vital Components SQ42H00001 <a href="http://www.avc.com.tw">www.avc.com.tw</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td></td>
<td>Performance</td>
<td></td>
<td>Dynatron G218 <a href="http://www.Dynatron-Corp.com">www.Dynatron-Corp.com</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td></td>
<td>Performance</td>
<td></td>
<td>Delta Electronics DHS-B9090-20 <a href="http://www.deltawww.com">www.deltawww.com</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td></td>
<td>Performance</td>
<td></td>
<td>Celsia Technologies 01IN001 <a href="http://www.celsiatechnologies.com">www.celsiatechnologies.com</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td>Assembly, Heatsink, 2U</td>
<td>Standard</td>
<td>Heatsink, 2U</td>
<td>Asia Vital Components SR40400001 <a href="http://www.avc.com.tw">www.avc.com.tw</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td></td>
<td>Standard</td>
<td></td>
<td>Asia Vital Components SR41400002 <a href="http://www.avc.com.tw">www.avc.com.tw</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td></td>
<td>Standard</td>
<td></td>
<td>Thermaltake CL-P0486 <a href="http://www.Thermaltake.com">www.Thermaltake.com</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td></td>
<td>Standard</td>
<td></td>
<td>CoolerMaster S2N-PJMHS-07-GP <a href="http://www.CoolerMaster.com">www.CoolerMaster.com</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td></td>
<td>Standard</td>
<td></td>
<td>TaiSol Corporation 1A0-9041000960-A <a href="http://www.Taisol.com">www.Taisol.com</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td></td>
<td>Low Cost</td>
<td></td>
<td>Dynatron Corporation (Top Motor/Dynaeon) G520 <a href="http://www.Dynatron-Corp.com">www.Dynatron-Corp.com</a></td>
<td>not capable for 80W (2-core, 1 socket); capable for all other SKUs up to 95W</td>
</tr>
<tr>
<td></td>
<td>Low Cost</td>
<td></td>
<td>CoolJag JAC0B40A <a href="http://www.CoolJag.com">www.CoolJag.com</a></td>
<td>not capable for 80W (2-core, 1 socket); capable for all other SKUs up to 95W</td>
</tr>
</tbody>
</table>
Table A-3. Suppliers for the Alternative Thermal Solution (Sheet 3 of 3)

<table>
<thead>
<tr>
<th>Assembly, Heatsink, Tower</th>
<th>Component</th>
<th>Description</th>
<th>Supplier PN</th>
<th>Thermal Capability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assembly, Heatsink</td>
<td>Tower</td>
<td>Standard</td>
<td>TaiSol Corporation 1A0-905100960-A <a href="http://www.Taisol.com">www.Taisol.com</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td>Assembly, Heatsink</td>
<td>Alternative URS Heatsink</td>
<td>Standard</td>
<td>Thermaltake CL-P0485 <a href="http://www.Thermaltake.com">www.Thermaltake.com</a></td>
<td>up to 95W capable</td>
</tr>
<tr>
<td>Assembly, Heatsink</td>
<td>Pedestal/2U Active Heatsink</td>
<td>Standard</td>
<td>Asia Vital Components SS40W00001 <a href="http://www.avc.com.tw">www.avc.com.tw</a></td>
<td>up to 95W capable</td>
</tr>
</tbody>
</table>

Notes:
1) Standard - Design and technology similar to Intel Reference or Collaboration designs, however, may not meet thermal requirements for all processor SKUs.
2) Performance - 1U Heatsink designed with premium materials or technology expected to provide optimum thermal performance for all processor SKUs.
3) Low Cost - 2U Cost-Optimized Heatsink, expected to meet thermal targets for lower power processor SKUs.

A.1.4 Socket, ILM and Back Plate

The LGA1356 Socket, ILM and Back Plate are described in Chapter 2 and Chapter 3, respectively. Socket mechanical drawings are provided in Appendix C. Mechanical models are listed in Table 1-1.

Table A-4. LGA1356 Socket, ILM and Back Plate

<table>
<thead>
<tr>
<th>Item</th>
<th>Intel PN</th>
<th>Foxconn</th>
<th>Tyco</th>
<th>Molex</th>
</tr>
</thead>
<tbody>
<tr>
<td>ILM Assembly</td>
<td>D92428-003</td>
<td>PT44L13-4102</td>
<td>1554105-1</td>
<td>475939000</td>
</tr>
<tr>
<td>ILM Assembly with ILM Cover</td>
<td>G13666-001</td>
<td>PT44L13-4111</td>
<td>1-1554105-1</td>
<td>475939070</td>
</tr>
<tr>
<td>ILM Cover</td>
<td>G14954-001</td>
<td>012-1000-5776</td>
<td>1-2134711-1</td>
<td>475930403</td>
</tr>
<tr>
<td>Back Plate</td>
<td>D92433-002</td>
<td>PT44P12-4104</td>
<td>1981467-2</td>
<td>475937000</td>
</tr>
<tr>
<td>LGA1356 Socket</td>
<td>E81085-001</td>
<td>PE135627-4371-01H</td>
<td>1554116-1</td>
<td>475943001</td>
</tr>
</tbody>
</table>

Supplier Contact Info
- Julia Jiang juliaj@foxconn.com 408-919-6178
- Billy Hsieh billy.hsieh@tycoelectronics.com +81 44 844 8292
- Carol Liang carol.liang@molex.com Tel #: +86-21-5048-0889 ext 3301
## B Mechanical Drawings

<table>
<thead>
<tr>
<th>Description</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Board Keepin / Keepout Zones (Sheet 1 of 4)</td>
<td>Figure B-1</td>
</tr>
<tr>
<td>Board Keepin / Keepout Zones (Sheet 2 of 4)</td>
<td>Figure B-2</td>
</tr>
<tr>
<td>Board Keepin / Keepout Zones (Sheet 3 of 4)</td>
<td>Figure B-3</td>
</tr>
<tr>
<td>Board Keepin / Keepout Zones (Sheet 4 of 4)</td>
<td>Figure B-4</td>
</tr>
<tr>
<td>1U Reference Heatsink Assembly (Sheet 1 of 2)</td>
<td>Figure B-5</td>
</tr>
<tr>
<td>1U Reference Heatsink Assembly (Sheet 2 of 2)</td>
<td>Figure B-6</td>
</tr>
<tr>
<td>1U Reference Heatsink Fin and Base (Sheet 1 of 2)</td>
<td>Figure B-7</td>
</tr>
<tr>
<td>1U Reference Heatsink Fin and Base (Sheet 2 of 2)</td>
<td>Figure B-8</td>
</tr>
<tr>
<td>Heatsink Shoulder Screw (1U, 2U and Tower)</td>
<td>Figure B-9</td>
</tr>
<tr>
<td>Heatsink Compression Spring (1U, 2U and Tower)</td>
<td>Figure B-10</td>
</tr>
<tr>
<td>Heatsink Retaining Ring (1U, 2U and Tower)</td>
<td>Figure B-11</td>
</tr>
<tr>
<td>Heatsink Load Cup (1U, 2U and Tower)</td>
<td>Figure B-12</td>
</tr>
<tr>
<td>2U Collaborative Heatsink Assembly (Sheet 1 of 2)</td>
<td>Figure B-13</td>
</tr>
<tr>
<td>2U Collaborative Heatsink Assembly (Sheet 2 of 2)</td>
<td>Figure B-14</td>
</tr>
<tr>
<td>2U Collaborative Heatsink Volumetric (Sheet 1 of 2)</td>
<td>Figure B-15</td>
</tr>
<tr>
<td>2U Collaborative Heatsink Volumetric (Sheet 2 of 2)</td>
<td>Figure B-16</td>
</tr>
<tr>
<td>Tower Collaborative Heatsink Assembly (Sheet 1 of 2)</td>
<td>Figure B-17</td>
</tr>
<tr>
<td>Tower Collaborative Heatsink Assembly (Sheet 2 of 2)</td>
<td>Figure B-18</td>
</tr>
<tr>
<td>Tower Collaborative Heatsink Volumetric (Sheet 1 of 2)</td>
<td>Figure B-19</td>
</tr>
<tr>
<td>Tower Collaborative Heatsink Volumetric (Sheet 2 of 2)</td>
<td>Figure B-20</td>
</tr>
<tr>
<td>1U Reference Heatsink Assembly with TIM (Sheet 1 of 2)</td>
<td>Figure B-21</td>
</tr>
<tr>
<td>1U Reference Heatsink Assembly with TIM (Sheet 2 of 2)</td>
<td>Figure B-22</td>
</tr>
<tr>
<td>2U Reference Heatsink Assembly with TIM (Sheet 1 of 2)</td>
<td>Figure B-23</td>
</tr>
<tr>
<td>2U Reference Heatsink Assembly with TIM (Sheet 2 of 2)</td>
<td>Figure B-24</td>
</tr>
<tr>
<td>Tower Reference Heatsink Assembly with TIM (Sheet 1 of 2)</td>
<td>Figure B-25</td>
</tr>
<tr>
<td>Tower Reference Heatsink Assembly with TIM (Sheet 2 of 2)</td>
<td>Figure B-26</td>
</tr>
<tr>
<td>25.5 mm Reference Heatsink Assembly (Sheet 1 of 2)</td>
<td>Figure B-27</td>
</tr>
<tr>
<td>25.5 mm Reference Heatsink Assembly (Sheet 2 of 2)</td>
<td>Figure B-28</td>
</tr>
<tr>
<td>25.5 mm Reference Heatsink Fin and Base (Sheet 1 of 2)</td>
<td>Figure B-29</td>
</tr>
<tr>
<td>25.5 mm Reference Heatsink Fin and Base (Sheet 2 of 2)</td>
<td>Figure B-30</td>
</tr>
<tr>
<td>25.5 mm Reference Heatsink Assembly with TIM (Sheet 1 of 2)</td>
<td>Figure B-31</td>
</tr>
<tr>
<td>25.5 mm Reference Heatsink Assembly with TIM (Sheet 2 of 2)</td>
<td>Figure B-32</td>
</tr>
</tbody>
</table>
Figure B-1. Board Keepin / Keepout Zones (Sheet 1 of 4)
Figure B-2. Board Keepin / Keepout Zones (Sheet 2 of 4)
Figure B-3. Board Keepin / Keepout Zones (Sheet 3 of 4)
Figure B-4. Board Keepin / Keepout Zones (Sheet 4 of 4)
Figure B-6. 1U Reference Heatsink Assembly (Sheet 2 of 2)
Figure B-7. 1U Reference Heatsink Fin and Base (Sheet 1 of 2)
Figure B-9. Heatsink Shoulder Screw (1U, 2U and Tower)
Figure B-10. Heatsink Compression Spring (1U, 2U and Tower)
Figure B-11. Heatsink Retaining Ring (1U, 2U and Tower)
Figure B-12. Heatsink Load Cup (1U, 2U and Tower)
Figure B-13. 2U Collaborative Heatsink Assembly (Sheet 1 of 2)
Figure B-15. 2U Collaborative Heatsink Volumetric (Sheet 1 of 2)
Figure B-16. 2U Collaborative Heatsink Volumetric (Sheet 2 of 2)
Figure B-20. Tower Collaborative Heatsink Volumetric (Sheet 2 of 2)
Figure B-21. 1U Reference Heatsink Assembly with TIM (Sheet 1 of 2)
Figure B-22. 1U Reference Heatsink Assembly with TIM (Sheet 2 of 2)

Thermal Interface Application

PROTECTIVE LINER NOT SHOWN.

INSTALL PER MANUFACTURER'S RECOMMENDATION. SEE PARTS LIST, SHEET 1, ITEM 2

SEE NOTE 9
Figure B-24. 2U Reference Heatsink Assembly with TIM (Sheet 2 of 2)
Figure B-25. Tower Reference Heatsink Assembly with TIM (Sheet 1 of 2)
THERMAL INTERFACE APPLICATION

PROTECTIVE LINER NOT SHOWN.
INSTALL PER MANUFACTURER'S RECOMMENDATION. SEE PARTS LIST, SHEET 1, ITEM 2.

SEE NOTE 9
Figure B-27. 25.5 mm Reference Heatsink Assembly (Sheet 1 of 2)
Figure B-28. 25.5 mm Reference Heatsink Assembly (Sheet 2 of 2)
Figure B-31. 25.5 mm Reference Heatsink Assembly with TIM (Sheet 1 of 2)
Figure B-32. 25.5 mm Reference Heatsink Assembly with TIM (Sheet 2 of 2)
Table C-1 lists the mechanical drawings included in this appendix.

Table C-1. Mechanical Drawing List

<table>
<thead>
<tr>
<th>Drawing Description</th>
<th>Figure Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>&quot;Socket Mechanical Drawing (Sheet 1 of 4)&quot;</td>
<td>Figure C-1</td>
</tr>
<tr>
<td>&quot;Socket Mechanical Drawing (Sheet 2 of 4)&quot;</td>
<td>Figure C-2</td>
</tr>
<tr>
<td>&quot;Socket Mechanical Drawing (Sheet 3 of 4)&quot;</td>
<td>Figure C-3</td>
</tr>
<tr>
<td>&quot;Socket Mechanical Drawing (Sheet 4 of 4)&quot;</td>
<td>Figure C-4</td>
</tr>
</tbody>
</table>
Figure C-1. Socket Mechanical Drawing (Sheet 1 of 4)
Figure C-2. Socket Mechanical Drawing (Sheet 2 of 4)
Figure C-4. Socket Mechanical Drawing (Sheet 4 of 4)
The following optional tool is designed to provide mechanical assistance during processor installation and removal.

Contact the supplier for details regarding this tool:

Billy Hsieh
billy.hsieh@tycoelectronics.com
+81 44 844 8292
Figure D-1. Processor Installation Tool
Embedded Server SKU’s target higher case temperatures and/or NEBS thermal profiles for embedded communications server and storage form factors. This section describes reference heatsinks for NEBS (Network Equipment Building Systems) compliant ATCA (Advanced Telecommunications Computing Architecture) systems. These higher case temperature processors are sufficient for any form factor that needs to meet NEBS requirements.

### E.1 Performance Targets

Table E-1 provides boundary conditions and performance targets for 1U and ATCA heatsinks. These values are used to generate processor thermal specifications and to provide guidance for heatsink design.

#### Table E-1. 8-Core/6-Core Processor Reference Thermal Boundary Conditions

<table>
<thead>
<tr>
<th>TDP</th>
<th>Heatsink Technology</th>
<th>(\Psi_{ca}^{2} (\circ C/W))</th>
<th>(T_{LA}^{1, 4} (\circ C))</th>
<th>Heatsink Volumetric (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LV70W (8-core)</td>
<td>ATCA Cu base Al fins</td>
<td>0.466</td>
<td>45/60</td>
<td>90x90x13.3</td>
</tr>
<tr>
<td>LV60W (6-core)</td>
<td>ATCA Cu base Al fins</td>
<td>0.467</td>
<td>45/60</td>
<td>90x90x13.3</td>
</tr>
</tbody>
</table>

#### Table E-2. 4-Core Processor Reference Thermal Boundary Conditions

<table>
<thead>
<tr>
<th>TDP</th>
<th>Heatsink Technology</th>
<th>(\Psi_{ca}^{2} (\circ C/W))</th>
<th>(T_{LA}^{1, 4} (\circ C))</th>
<th>Heatsink Volumetric (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LV50W (4-core)</td>
<td>ATCA Cu base Al fins</td>
<td>0.509</td>
<td>52/67</td>
<td>90x90x13.3</td>
</tr>
</tbody>
</table>

Notes:
1. Local ambient temperature of the air entering the heatsink.
2. Max target (mean + 3 sigma + offset) for thermal characterization parameter (Section 5.4.1).
3. Dimensions of heatsink do not include socket or processor.
4. Local Ambient Temperature written X/Yo C means Xo C under Nominal conditions but Yo C is allowed for Short-Term NEBS excursions.
5. All heatsinks are Non-Direct Chassis Attach (DCA)
6. See Section 5.1 for standard 1U solutions that do not need to meet NEBS.
Detailed drawings for the ATCA reference heatsink can be found in Section E.3. Table E-1 above specifies $\Psi_{ca}$ and pressure drop targets and Figure E-1 below shows $\Psi_{ca}$ and pressure drop for the ATCA heatsink versus the airflow provided. Best-fit equations are provided to prevent errors associated with reading the graph.

**Figure E-1. ATCA Heatsink Performance Curves**

Other LGA1366 compatible thermal solutions may work with the same retention.

ATCA 13 mm heatsink performance using Intel® Xeon® processor 5500 series TTV.

### E.2 Thermal Design Guidelines

#### E.2.1 High Case Temperature Thermal Profile

Processors that offer a High case temperature thermal profile are specified in the *Intel® Xeon® Processor E5-2400 Product Family Datasheet - Volume One*.

High case temperature thermal profiles help relieve thermal constraints for Short-Term NEBS conditions. To help reliability, processors must meet the nominal thermal profile under standard operating conditions and can only rise up to the Short-Term spec for NEBS excursions (see Figure E-2). The definition of Short-Term time is clearly defined for NEBS Level 3 conditions but the key is that it cannot be longer than 360 hours per year.

Fan speed control is treated the same as standard processors. When DTS (Digital Temperature Sensor) value is less than $T_{control}$, the thermal profile can be ignored.
E.3 Mechanical Drawings and Supplier Information

See Appendix B for retention and keep out drawings.

The part number below represent Intel reference designs for a ATCA reference heatsink. Customer implementation of these components may be unique and require validation by the customer. Customers can obtain these components directly from the supplier below.

<table>
<thead>
<tr>
<th>Table E-3. Embedded Heatsink Component Suppliers</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Component</strong></td>
</tr>
<tr>
<td>ATCA Reference Heatsink</td>
</tr>
<tr>
<td>Intel P/N E65918-001</td>
</tr>
</tbody>
</table>
## Table E-4. Mechanical Drawings List

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATCA Reference Heat Sink Assembly (Sheet 1 of 2)</td>
<td>Figure E-3</td>
</tr>
<tr>
<td>ATCA Reference Heat Sink Assembly (Sheet 2 of 2)</td>
<td>Figure E-4</td>
</tr>
<tr>
<td>ATCA Reference Heatsink Fin and Base (Sheet 1 of 2)</td>
<td>Figure E-5</td>
</tr>
<tr>
<td>ATCA Reference Heatsink Fin and Base (Sheet 2 of 2)</td>
<td>Figure E-6</td>
</tr>
</tbody>
</table>
Figure E-3. ATCA Reference Heat Sink Assembly (Sheet 1 of 2)
Figure E-4. ATCA Reference Heat Sink Assembly (Sheet 2 of 2)
Figure E-6. ATCA Reference Heatsink Fin and Base (Sheet 2 of 2)