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## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Comments</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>002</td>
<td>• Added 6-core Microserver SKU.</td>
<td>November 2015</td>
</tr>
<tr>
<td></td>
<td>• Added Networking, IOTG, and Storage SKUs.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Added reference heatsink information for Networking, IOTG, and Storage</td>
<td></td>
</tr>
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  – Microserver reference thermal solutions
  – Storage reference thermal solutions
  – Communications Infrastructure reference thermal solutions
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Introduction

This document provides specifications and guidelines for the design of thermal and mechanical solutions for Intel® Xeon® Processor D-1500 Product Family for Microserver, Storage, and Communications segments.

The specifications and design guidelines apply to Intel® Xeon® Processor D-1500 Product Family in their current stage of development and *are subject to change*.

The reference thermal solutions described in this document include:

- Heatsink
- Retention hardware

The goal of this document is to enable board and system thermal mechanical designers and suppliers of SoC heatsinks to design thermal solutions for Intel® Xeon® Processor D-1500 Product Family.

The Intel® Xeon® Processor D-1500 Product Family SKU summary is located [here](#).
<table>
<thead>
<tr>
<th>Document</th>
<th>Reference</th>
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</thead>
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<td>Intel® Xeon® Processor D-1500 Product Family Datasheet - Volume 1 of 4: Integrated Platform Controller Hub</td>
<td>332050</td>
<td>1</td>
</tr>
<tr>
<td>Intel® Xeon® Processor D-1500 Product Family Datasheet - Volume 2 of 4: Registers</td>
<td>332051</td>
<td>1</td>
</tr>
<tr>
<td>Intel® Xeon® Processor D-1500 Product Family Datasheet - Volume 3 of 4: Electrical</td>
<td>332052</td>
<td>1</td>
</tr>
<tr>
<td>Intel® Xeon® Processor D-1500 Product Family Datasheet - Volume 4 of 4: Intel® Xeon® Processor D-1500 Product Family LAN Controller</td>
<td>332053</td>
<td>1</td>
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<tr>
<td>Storage Bridge Bay Specification</td>
<td></td>
<td></td>
</tr>
<tr>
<td>System Mechanical Design Guidance for Dynamic Events - Application Notes /Briefs</td>
<td>383578</td>
<td></td>
</tr>
<tr>
<td>Board Flexure Initiative (BFI) - Manufacturing Advantage Service (MAS)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Server Systems Infrastructure (SSI) - Microserver Micromodule Specification</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PICMG Specifications (AdvancedTCA, AdvancedMC, etc.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Form Factor Specifications (Motherboard, Power Supply, Riser, etc.)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. Contact your Field Sales Representative for the latest version of this document.
## Definition of Terms

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATCA</td>
<td>Advanced Telecommunications Computing Architecture</td>
</tr>
<tr>
<td>Bypass</td>
<td>Bypass is the area between a passive heatsink and any object that can act to form a duct. For this example, it can be expressed as a dimension away from the outside dimension of the fins to the nearest surface.</td>
</tr>
<tr>
<td>CPCI</td>
<td>Compact Peripheral Component Interconnect</td>
</tr>
<tr>
<td>DTS</td>
<td>Digital Thermal Sensor</td>
</tr>
<tr>
<td>FSC</td>
<td>Fan Speed Control</td>
</tr>
<tr>
<td>IHS</td>
<td>Integrated Heat Spreader</td>
</tr>
<tr>
<td>IOTG</td>
<td>Internet of Things Group</td>
</tr>
<tr>
<td>PECI</td>
<td>The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between SoC and chipset components to external monitoring devices</td>
</tr>
<tr>
<td>$\Psi_{ca}$</td>
<td>Case-to-ambient thermal characterization parameter (psi). A measure of thermal solution performance using Total Package Power. Defined as $(T_{CASE} - TLA) / (TDP)$. Heat source should always be specified for Y measurements.</td>
</tr>
<tr>
<td>$\Psi_{cs}$</td>
<td>Case-to-sink thermal characterization parameter. A measure of thermal interface material performance using Total Package Power. Defined as $(T_{CASE} - T_{SINK}) / (TDP)$.</td>
</tr>
<tr>
<td>SoC</td>
<td>System On a Chip.</td>
</tr>
<tr>
<td>$T_{CASE}$</td>
<td>The case temperature of the SoC measured at the geometric center of the topside of the IHS.</td>
</tr>
<tr>
<td>$T_{CASE-MAX}$</td>
<td>The maximum case temperature as specified in a component specification.</td>
</tr>
</tbody>
</table>
## Definition of Terms Continued

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCC</td>
<td>Thermal Control Circuit: thermal monitor uses the TCC to reduce the die temperature by using clock modulation and/or operating frequency and input voltage adjustment when the die temperature is very near its operating limits.</td>
</tr>
<tr>
<td>TDP</td>
<td>Thermal Design Power: thermal solution should be designed to dissipate this target SOC power level. TDP is not the maximum power that the SoC can dissipate.</td>
</tr>
<tr>
<td>Thermal Monitor</td>
<td>A power reduction feature designed to decrease temperature after the SoC has reached its maximum operating temperature.</td>
</tr>
<tr>
<td>TIM</td>
<td>Thermal Interface Material: The thermally conductive compound between the heatsink and the SoC integrated heat spreader (IHS). This material fills the air gaps and voids, and enhances the transfer of the heat from the SoC case to the heatsink.</td>
</tr>
<tr>
<td>T_{LA}</td>
<td>The measured ambient temperature locally surrounding the SoC. The ambient temperature should be measured just upstream of a passive heatsink or at the fan inlet for an active heatsink.</td>
</tr>
<tr>
<td>T_{SA}</td>
<td>The system ambient air temperature external to a system chassis. This temperature is usually measured at the chassis air inlets.</td>
</tr>
<tr>
<td>TTV</td>
<td>Thermal Test Vehicle</td>
</tr>
<tr>
<td>KOZ</td>
<td>Keep Out Zone</td>
</tr>
<tr>
<td>SJR</td>
<td>Solder Joint Reliability</td>
</tr>
<tr>
<td>SRO</td>
<td>Solder Resist Opening</td>
</tr>
</tbody>
</table>
PACKAGE INFORMATION
# Intel® Xeon® Processor D-1500 Product Family Package

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Intel® Xeon® Processor D-1500 Product Family</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>1667 Ball FCBGA</td>
</tr>
<tr>
<td>Solder Ball Diameter&lt;sup&gt;1&lt;/sup&gt;</td>
<td>0.462 mm</td>
</tr>
<tr>
<td>Solder Ball Pitch</td>
<td>0.7 mm, Variable</td>
</tr>
<tr>
<td>Substrate Size&lt;sup&gt;1&lt;/sup&gt;</td>
<td>37.5 mm x 37.5 mm</td>
</tr>
<tr>
<td>Substrate Thickness&lt;sup&gt;1&lt;/sup&gt;</td>
<td>1.222 mm</td>
</tr>
<tr>
<td>Integrated Heat Spreader Height&lt;sup&gt;1&lt;/sup&gt;</td>
<td>2.08 mm</td>
</tr>
<tr>
<td>Package Height&lt;sup&gt;1,2&lt;/sup&gt;</td>
<td>3.556 mm</td>
</tr>
<tr>
<td>Min/ Max Static Loading – with backplate</td>
<td>0 Lbf min, 35 Lbf max</td>
</tr>
<tr>
<td>Min/ Max Static Loading – without backplate</td>
<td>0 Lbf min, 15 Lbf max</td>
</tr>
<tr>
<td>Non-Critical to Function solder balls</td>
<td>114</td>
</tr>
</tbody>
</table>

Notes:
1. All dimensions are nominal
2. Package height is from the top of Integrated Heat Spreader (IHS) to bottom of the solder balls, Pre-SMT
Intel® Xeon® Processor D-1500 Product Family
Mechanical Drawing

Symbol | Nominal (mm) | Tolerance (mm)
--- | --- | ---
B1 | 37.5 | ± 0.05
B2 | 37.5 | ± 0.05
C1 | 30.7 | ± 0.05
C2 | 33 | ± 0.05
D1 | 0.154 | N/A
F2 | 2.08 | ± 0.078
F5 | 3.556 | ± 0.076

See Appendix A for Detailed Mechanical Drawing
SoC Thermal Specifications

The SoC requires a thermal solution to maintain temperatures within operating limits. Any attempt to operate the SoC outside these limits may result in permanent damage to the SoC and potentially other components within the system. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks in contact with the SoC integrated heat spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting.

To allow optimal operation and long-term reliability of Intel SoC-based systems, the SoC must remain within the case temperature ($T_{CASE}$) specifications as defined in [here](#).
## Intel® Xeon® Processor D-1500 Product Family Thermal, Power and SKU Summary – **Microserver**

<table>
<thead>
<tr>
<th>Core Count</th>
<th>TDP (W)</th>
<th>Non-Uniform Power Correction Factor¹ (C/W)</th>
<th>( T_{\text{CASE_MAX}} ) (°C)</th>
<th>( T_{\text{CASE_MIN}} ) (°C)</th>
<th>DTSmax (°C)</th>
<th>Tcontrol (°C)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>45</td>
<td>0.05</td>
<td>80</td>
<td>0</td>
<td>96</td>
<td>10</td>
<td>1,2,3,4,5,6</td>
</tr>
<tr>
<td>6</td>
<td>45</td>
<td>0.05</td>
<td>80</td>
<td>0</td>
<td>99</td>
<td>10</td>
<td>1,2,3,4,5,6</td>
</tr>
<tr>
<td>4</td>
<td>45</td>
<td>0.04</td>
<td>80</td>
<td>0</td>
<td>102</td>
<td>10</td>
<td>1,2,3,4,5,6</td>
</tr>
</tbody>
</table>

Notes
1. CF is the non-uniform heating correction factor in °C/W is defined as: CF = \( \Psi_{\text{CA\_SoC}} - \Psi_{\text{CA\_uniform\_heating\_TTV\_model}} \). It should be used to adjust \( \Psi_{\text{CA}} \) calculations or measurements based on the TTV thermal model/hardware that Intel provides to account for power density effect of operational silicon.
2. \( T_{\text{CASE}} \) is measured at the geometric center at the top surface of the Integrated Heat Spreader.
3. Thermal Design Power (TDP) should be used as a target for SoC thermal solution design at maximum \( T_{\text{CASE}} \). SoC power may exceed TDP for short durations. Please see Intel® Turbo Boost Technology for details.
4. These specifications are based on initial pre-silicon simulations, which will be updated as further characterization data becomes available.
5. Power specifications are defined at all VIDs found in the Intel® Xeon® Processor D-1500 Product Family SoC Datasheet. SoCs may have multiple VIDs for each frequency.
Intel® Xeon® Processor D-1500 Product Family Thermal, Power and SKU Summary – Networking, IOTG, and Storage

<table>
<thead>
<tr>
<th>Core Count</th>
<th>TDP (W)</th>
<th>Non-Uniform Power Correction Factor¹ (C/W)</th>
<th>$T_{CASE_MAX}$ (°C)</th>
<th>$T_{CASE_MIN}$ (°C)</th>
<th>DTSmax (°C)</th>
<th>Tcontrol (°C)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>45</td>
<td>0.05</td>
<td>89</td>
<td>0</td>
<td>104</td>
<td>22</td>
<td>1,2,3,4,5</td>
</tr>
<tr>
<td>8</td>
<td>35</td>
<td>0.05</td>
<td>92</td>
<td>-40</td>
<td>0</td>
<td>104</td>
<td>22</td>
</tr>
<tr>
<td>6</td>
<td>35</td>
<td>0.06</td>
<td>88</td>
<td>0</td>
<td>104</td>
<td>22</td>
<td>1,2,3,4,5</td>
</tr>
<tr>
<td>4</td>
<td>35</td>
<td>0.06</td>
<td>85</td>
<td>0</td>
<td>104</td>
<td>22</td>
<td>1,2,3,4,5</td>
</tr>
<tr>
<td>4</td>
<td>25</td>
<td>0.05</td>
<td>93</td>
<td>-40</td>
<td>0</td>
<td>104</td>
<td>22</td>
</tr>
<tr>
<td>2</td>
<td>25</td>
<td>0.04</td>
<td>92</td>
<td>0</td>
<td>104</td>
<td>22</td>
<td>1,2,3,4,5</td>
</tr>
<tr>
<td>2</td>
<td>20</td>
<td>0.04</td>
<td>96</td>
<td>0</td>
<td>106</td>
<td>22</td>
<td>1,2,3,4,5</td>
</tr>
</tbody>
</table>

Notes
1. CF is the non-uniform heating correction factor in °C/W is defined as: $CF = Y_{CA\_SoC} - Y_{CA\_uniform\_heating\_TTV\_model}$. It should be used to adjust $Y_{CA}$ calculations or measurements based on the TTV thermal model/hardware that Intel provides to account for power density effect of operational silicon.
2. $T_{CASE}$ is measured at the geometric center at the top surface of the Integrated Heat Spreader.
3. Thermal Design Power (TDP) should be used as a target for SoC thermal solution design at maximum $T_{CASE}$. SoC power may exceed TDP for short durations. Please see Intel® Turbo Boost Technology for details.
4. These specifications are based on initial pre-silicon simulations, which will be updated as further characterization data becomes available.
5. Power specifications are defined at all VIDs found in the Intel® Xeon® Processor D-1500 Product Family SoC Datasheet. SoCs may have multiple VIDs for each frequency.
6. SKU configuration available as an eTEMP (Extended Temperature) or a Standard Temperature Part.
7. SKUs are only validated up to 90°C of dynamic range, Intel does not guarantee that the SKU will operate properly outside this range. Dynamic range = absolute (Operating temp – Boot Temperature).
What is eTemp?

**Definition**

Extended temperature or eTEMP is a stringent operating temperature range that ensures that a electrical or mechanical component will operate reliably in a -40°C to 85°C environment.

**What does the Operating Temperature Mean?**

- Cold: The lowest local system boot temperature of the device (Cold Soak).
  - $T_{AIR} = T_{LA} = T_{Case-MIN}$
- Hot: The hottest local temperature ~1” (25mm)† upstream of the component.
  - $T_{AIR} < T_{LA} < T_{Case-MAX}$

**Does this mean that $T_{Case-MAX}$ will change for eTEMP?**

No. $T_{Case-MAX}$ is a component level specification and should not be confused with eTEMP operating temperature ranges.

**What about $T_{Case-MIN}$?**

- $T_{Case-MIN}$ will change to meet -40°C. $T_{Case-MIN}$ will be equal to the operating ambient temperature during cold soak durations. $T_{Case}$ does not need to be maintained at -40°C after boot.

†This distance may need to be reduced depending on system density and upstream components.
Tcontrol Overview

Customers are required to maintain the SoC temperature, as measured by the DTS, at or below the Tcontrol temperature to ensure long term reliability of the SoC. The Tcontrol specification is an offset from DTSmax, resulting in the following equation for calculating the Tcontrol temperature:

\[ \text{Tcontrol temperature} = \text{DTSmax} - \text{Tcontrol} \]

The SoC temperature can be calculated by the following equation:

\[ \text{DTS temperature} = \text{DTSmax} - \text{DTS offset} \]

The following actions summarize required responses to the Tcontrol temperature:

- **DTS Temperature < Tcontrol temperature**: The system can run under any desired fan speed control condition.
- **DTS Temperature = Tcontrol temperature**: Tcontrol limit attained, system must increase fan speed to reduce DTS temperature below Tcontrol temperature.
- **DTS Temperature > Tcontrol temperature**: Fan speed increase is required to maintain Tcase below Tcase-max.

*Note: SoC temperature (either Tcase or DTS) may exceed Tcontrol for a duration totalling less than 360 hours per year without affecting long term reliability (life) of the SoC.*
Thermal Management Features

The following is a list of supported features on the SoC:

• **Digital Thermal Sensor** – On-die sensor for SoC temperature monitoring.

• **Intel® Adaptive Thermal Monitor** - The Adaptive Thermal Monitor feature provides an enhanced method for controlling the SoC temperature when the SoC silicon exceeds the Thermal Control Circuit (TCC) activation temperature.

• **THERMTRIP** - In the event of catastrophic cooling failure the SoC will automatically shut down when the silicon has reached and elevated temperature. THERMTRIP_N, a non-user configurable and non-software visible signal, will go active and stay active.

• **PROCHOT_N support** - The PROCHOT_N signal is bi-directional in that it can either signal when the SoC (any core) has reached its maximum operating temperature or be driven from an external source to activate the TCC.

• **On-Demand Mode** – The SoC provides an auxiliary mechanism that allows system software to force the SoC to reduce its power consumption.

• **Memory Thermal Throttling** – The purpose is to protect DIMMs from excess temperature which can cause harm over time, as well as ensure that the proper refresh rate is achieved. Closed Loop Thermal Throttling, Open Loop Thermal Throttling and DDR01_MEMHOT_N Signal are features available.

• **Running Average Power Limit (RAPL)** - This feature allows setting a power budget on the SoC domain (a.k.a. core or package RAPL) that limits total SoC power through frequency reduction. It also allows monitoring of performance (frequency) and average SoC power for a user configurable time window ("running average" approach). This feature provides a variety of potential benefits, including meeting power budgets and maintaining thermal/power limits at the system, rack and/or data center levels.

• **Platform Environment Control Interface (PECI)** - An Intel-defined, one-wire bus interface that provides a communication channel between Intel processors and external system management devices. The interface enables an external management controller to obtain thermal data from sensors integrated into components in the system. For details on PECI implementation and commands, refer to the Platform Environment Control Interface (PECI) Specification.

Please consult the Datasheet for details.
**Tcase Metrology**

The following supplier can machine the groove and attach a thermocouple to the IHS. The supplier is listed below as a convenience to Intel's general customers and the list may be subject to change without notice. THERM-X OF CALIFORNIA Inc, 3200 Investment Blvd., Hayward, Ca 94545. George Landis +1-510-441-7566 Ext. 368 georgel@therm-x.com. The vendor part number is XTMS1565.

REFERENCE DESIGNS AND SUPPLIERS FOR EACH SEGMENT
## Reference Thermal Solution Assumptions - Standard Heatsink

<table>
<thead>
<tr>
<th>Power SKU</th>
<th>Number of nodes in-line with the direction of the airflow</th>
<th>Key Assumptions</th>
</tr>
</thead>
</table>
| 45W       | 3 nodes in-line with the direction of the airflow        | The enabling boundary conditions are based on the following assumptions:  
• ASHRAE class A2 environment.  
• Micro-module channel airflow: 30CFM.  
• Local ambient temperature at the last node assumes 85% TDP for upstream nodes.  
• Pitch between micromodules: 42mm.  
• Airflow management to maximize heatsink flow. |

### Notes:
1. Customer node density may vary.  
2. Node density changes may drive SoC temperature specification changes.  
3. Module width may vary depending on customer implementation, in this case a width between ~254 mm and ~305 mm and a height of ~119 mm was considered.
Heatsink Airflow Guidance* as a function of Nodes In-line (cont’d)

* Using conditions above. Customer implementations may vary.
# System Reference Boundary Conditions

<table>
<thead>
<tr>
<th>SoC Power Range SKU</th>
<th>Reference Heatsink Concept</th>
<th>Local ambient Temperature, $T_{la}$ (°C)</th>
<th>Airflow through Heatsink (CFM)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>45W</td>
<td>Standard</td>
<td>48.7</td>
<td>7.9</td>
<td>1</td>
</tr>
</tbody>
</table>

Notes:
1. 3 nodes in-line with the direction of the airflow

![Standard heatsink diagram](image)
Standard Height Heatsink Design - Microserver

Standard heatsink design details

• Material: Extruded aluminum heatsink

• Overall heatsink dimensions: 50mm(W) x 66mm(L) x 29.85 mm(H)

• Retention: four screws with backplate

• TIM: PCM45F
  - Min required load is **27 lbf** EOLife

• Fins: qty 20 (27.35mm tall)

• Pitch: 2.5mm

• Base thickness: 2.5mm

• Backplate is mainly used to provide higher TIM force

• Target power is >20W

See [Appendix B](#) for mechanical drawings and [Appendix H](#) for supplier info
EoLife $\Psi_{ca} = 3\sigma^* + \alpha + \beta^*(\text{CFM})^\gamma$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\alpha$</td>
<td>0.303</td>
</tr>
<tr>
<td>$\beta$</td>
<td>1.600</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>0.718</td>
</tr>
<tr>
<td>$3\sigma$</td>
<td>0.018</td>
</tr>
</tbody>
</table>

Airflow through the fins and bottom

Standard Heatsink Performance Curve

Heatsink performance ($\Psi_{ca}$, °C/W) as a function of airflow (CFM)

![Graph showing standard heatsink performance](image)
ENTERPRISE STORAGE SEGMENT REFERENCE THERMAL SOLUTION
Storage Form Factors

• Storage Bridge Bay
  – Common canister definition for Storage enclosure.
  – Refer to SBB Specification v.2.1 located at http://www.sbbwg.org/sbb_specification/

• 1U Cloud Storage
  – Low cost, 1U rack mount chassis using 3.5” hard drives.
Storage Bridge Bay Overview

- Typically two SBB canisters plug into a midplane within chassis along with HDDs and PSUs.
- Overall maximum canister dimensions: 209.55 mm (W) x 284.5 mm (L) x 38.1 mm (H)
- Clearance above board for heatsinks: 27.5 mm (for 1 mm sheetmetal thickness)
- Airflow enters chassis at connector end and exits through one of two venting configurations.

For details, refer to the SBB Specification v.2.1 located at www.sbbwg.org
SBB System Thermal Assumptions

- Chassis configuration: 2U with 24 2.5” HDDs
- Chassis external ambient: 35 °C
- Canister inlet ambient: 45 °C
- Canister airflow: 40 CFM
- Target exit temperature: 50 °C
- Vent 1 configuration – due to excessive airflow bypass of the BDX-DE heatsink, Vent 2+3 configuration is not recommended for reference heatsink implementation.
- Trabuco Canyon Customer Reference Board layout.
## System Reference Boundary Conditions

<table>
<thead>
<tr>
<th>SoC Power Range SKU</th>
<th>Reference heatsink Concept</th>
<th>Local ambient Temperature, $T_{la}$ (°C)</th>
<th>Airflow through heatsink (CFM)</th>
<th>Notes</th>
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<td>(11 mm height)</td>
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<td>25W</td>
<td>Low profile++</td>
<td>48</td>
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<td></td>
<td>(19 mm height)</td>
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<td>Low profile</td>
<td>48</td>
<td>1.5</td>
<td>1</td>
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Notes:
1. These specifications are based on initial pre-silicon simulations, which will be updated as further characterization data becomes available.

### Diagrams
- **Low Profile heatsink**: Airflow through the fins on top and bottom.
- **SBB Standard heatsink**: Airflow through the fins and bottom.
Heatsink application guidelines for Storage SKUs ≤25W

- The low profile heatsink can be used for Storage SKUs with TDP ≤20W in a SBB Canister.

- For the 25W SKU, the low profile heatsink requires increased airflow of 2.7 CFM through the heatsink. Alternatively, the heatsink height can be increased to 19 mm using same airflow rate (40 CFM canister flow).
SBB Standard Heatsink Mechanical Design - Storage

SBB Standard heatsink
- Material: Extruded aluminum heatsink
- Overall heatsink dimensions: 60mm (W) x 66mm (L) x 23.5mm (H)
- Retention: four screws with backplate
- TIM: PCM45F
  - Min required load is 27 lbf* EOLife
- #Fins: 24 (21mm tall)
- Pitch: 2.5 mm
- Base thickness: 2.5 mm
- Backplate is mainly used to provide higher TIM force
- Target power is >25W

See Appendix D for mechanical drawings, some parts can be found in Appendix B.

See Appendix H for supplier info.

*Note: design consideration for adequate thermal performance
SBB Standard Heatsink Performance Curve

Performance ($\Psi_{ca}$, °C/W) as a function of airflow (CFM)

EoLife $\Psi_{ca} + 3\sigma = \alpha + \beta^{*}(\text{CFM})^\gamma$

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<td>$\alpha$</td>
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<tr>
<td>$3\sigma$</td>
<td>0.042</td>
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SBB S-HS performance

Airflow through the fins and bottom
Low Profile Heatsink Mechanical Design – Storage

Low profile Storage heatsink
- Material: Extruded aluminum heatsink
- Overall heatsink dimensions: 50mm(W)x54mm(L)x11.35mm(H)
- Retention: Z-clip/baseboard anchors
- TIM: PCM45F
  - Min required load is 18Lbf* EOLife
- #Fins: top 20 (7.35mm tall), bottom 21 (1.5mm tall)
- Fin Pitch: 2.5mm (top and bottom)
- Base thickness: 2.5mm
- Target power is <=20W

See Appendix C for mechanical drawings and Appendix H for supplier info.

*Note: design consideration for adequate thermal performance
Low Profile Heatsink Performance Curve

Performance (C/W) as a function of airflow (CFM)

EoLife $\Psi_{ca} + 3\sigma = \alpha + \beta^{*}(CFM)^{\gamma}$

<p>| | |</p>
<table>
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<tbody>
<tr>
<td>$\alpha$</td>
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<tr>
<td>$\beta$</td>
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<tr>
<td>$\gamma$</td>
<td>0.782</td>
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<tr>
<td>$3\sigma$</td>
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Low Profile Heatsink

Airflow through the fins on top and bottom
1U Cloud Storage Overview - Example

• Low cost, high density storage using standard 1U chassis.

• Typically 15 3.5” HDDs mounted in front of chassis, with fans located mid chassis between HDDs and motherboard.

• 40 mm fans positioned for fan fail cooling scenarios.

• Rotational vibration (RV) interference from array of HDDs needs to be mitigated. Some options include:
  – Choice of HDD (Enterprise vs. Consumer, RV tolerant).
  – HDD mounting using vibration damping materials.
1U Cloud Storage Reference Heatsink Design

- The following SoC heatsink boundary conditions are assumed for typical 1U rackmount Cloud Storage systems:
  - Local ambient temperature = 50 °C
  - Flow through heatsink (through fins and under heatsink) = 4.9 CFM
  - No fan failure

- Thermal simulation results show that the Storage Bridge Bay reference heatsink is able to cool all Storage SKUs in a 1U Cloud Storage system.
  - For a fan failure of a fan directly in front the heatsink, performance may be significantly impacted.
  - Since the heatsink height was defined for the SBB form factor, additional thermal headroom can be obtained by by increasing fin height and reducing airflow bypass over the top of the heatsink.
PCIe* Storage Host Bus Adapter Overview

- Storage Host Bus Adapter (HBA) plugs into enterprise storage server PCIe* slot.
- Typically \( \frac{3}{4} \) to full length PCIe form factor.
- PCI component height specification:
  - Primary side max height = 14.47 mm
  - Secondary side max component height = 2.35 mm
PCIe* Storage Host Bus Adapter Reference Heatsink Design

• The following SoC heatsink boundary conditions are assumed for worst case PCIe* thermal environment:
  – Local ambient temperature = 55 °C
  – Airflow approach velocity = 150 LFM (linear ft/min)

• Reference heatsink design details:
  • 93 mm x 93 mm x 10.2 mm
  • Extruded aluminum
  • Four (4) brass off-the-shelf spring loaded push pins (ITW* 84FT02-129)

• Thermal simulation results show that the PCIe HBA reference heatsink is able to cool Storage SKUs with TDP below 20 W.

Note: The reference heatsink has not been validated and is presented as a concept only. Users should conduct their own thermal and mechanical validation testing prior to using in production.
PCIe* Storage Host Bus Adapter Reference

Heatsink Performance

- The following mean heatsink performance curve was derived:
  - An adjustment of +0.13 °C/W is recommended to account for 3sigma variation and TIM degradation for End Of Life.
  - The non-uniform heating correction factor provided [here](#) should be added as well.
COMMUNICATIONS SEGMENT REFERENCE THERMAL SOLUTION

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ATCA® Reference Heatsink Design

- Performance data is based on test data.
- The non-uniform heating correction factor provided [here](#) should be added as well.
- See Appendix D for detailed mechanical drawings.

**Detailed ATCA® heatsink Properties**

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<th>Material</th>
<th>Aluminum (Al), $k = 200$ W/m-K or better</th>
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<td>Fin Thickness (mm)</td>
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<td># of Fins</td>
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**ATCA® Heat Sink Performance**

\[
y = 26.209x^{-0.613} \\
R^2 = 0.9959
\]
CPCI* Reference Heatsink Design

<table>
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<tr>
<th>Detailed CPCI* Heatsink Properties</th>
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<tbody>
<tr>
<td>Material</td>
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<tr>
<td>Overall Dimensions (mm)</td>
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<tr>
<td>Base Thickness (mm)</td>
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<tr>
<td>Fin Height (mm)</td>
</tr>
<tr>
<td>Fin Thickness (mm)</td>
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<tr>
<td># of Fins</td>
</tr>
</tbody>
</table>

- Performance data is based on test data.
- The non-uniform heating correction factor provided here should be added as well.
- See Appendix E for detailed mechanical drawings.

**cPCI* Heat Sink Performance**

\[ y = 33.831x^{-0.566} \]

\[ R^2 = 0.994 \]
APPENDIX B - STANDARD HEATSINK MECHANICAL DRAWINGS
Backplate for 62 mil thick boards (56-76 mils range)
Backplate for 62 mil thick boards (56-76 mils range)

Notes: unless otherwise specified:

1. Reference Documents:
   - ASME Y14.5M-1994 - Standard Dimension and Tolerances
   - MIL-STD-1260 - Standard Dimension and Tolerances

2. Features not specified on drawing and features without specified tolerance shall be controlled by CAD database, and shall conform to sheetmetal tolerance standard (ASME B94.5).

3. Natural, may use Intel engineering approved equivalent:
   - Type: Steel, 301, 303, or C1045.
   - Tension yield strength (ASTM 0269) ~ 250 MPa
   - Ultimate tensile strength (ASTM 0269) ~ 360 MPa
   - PLATING: a) Microneters minimum electrolytic nickel.
   - Process test: 168 hours 85% humidity with no visible corrosion.

4. Dimensions are critical to function dimensions (CTF).

5. Parts shall be free of oil and debris.

6. Barh heights shall not exceed 1.25mm.

7. Sharp corners must be chamfered, or rounded to 0.25 mm MAC.

8. Parts to be flat within ±0.125 mm.

9. Torsion out: 13 in-lb (1.474 N-m) minimum.


11. Install all studs flush to this surface. ±0.000 - .25.

12. Mark part approximately where shown with the following information: 2mm high characters, color (black) or black mark or punch mark.

*Recommended Board Thickness Range: 1.42mm (0.056) to 1.938mm (0.076)

Reference Number: 332055-002
Backplate for 93 mil thick boards (76-103 mils range)
Backplate for 93 mil thick boards (76-103 mils range)
NOTES:

1. THIS DRAWING TO BE USED IN CONJUNCTION WITH SUPPLIED 3D DATABASE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED DATABASE.

2. PRIMARY DIMENSIONS STATED IN MILLIMETERS. BRACKETED DIMENSIONS STATED IN INCHES.

3. MATERIAL: SPRING STEEL OR STAINLESS STEEL

   YIELD STRENGTH (max): 90000 PSI (620 MPA)

   MODULUS OF ELASTICITY (E): 2800000 KSI (193 GPa)

   MATERIAL PROPERTIES MUST BE MET AFTER FINAL E-RING MANUFACTURING PROCESS

4. FINISH: NI PLATED IF NOT STAINLESS

5. CRITICAL TO FUNCTION DIMENSION


6. E-RING SPECIFICATION JIS B 2005 APPLIES FOR OFF THE SHELF COMPONENT COMPLIANCE.
NOTES: UNLESS OTHERWISE SPECIFIED:

1. REFERENCE DOCUMENTS
   96-0007-001 - INTEL WORKMANSHIP STANDARD - SYSTEMS MANUFACTURING
   18-1201 - INTEL ENVIRONMENTAL PRODUCT CONTENT SPECIFICATION FOR
   SUPPLIERS & OUTSOURCED MANUFACTURERS (FOUND ON
   EHS WEBSITE - https://supplier.intel.com/static/EHS/)

   FEATURES NOT SPECIFIED ON DRAWING SHALL BE CONTROLLED BY 3D CAD
   DATABASE. IF PROVIDED, MEASUREMENTS SHOULD REFERENCE DATUM
   PRIMARY, DATUM B SECONDARY, AND C TERTIARY.

3. MATERIAL MAY USE INTEL ENGINEERING APPROVED EQUIVALENT.
   ALL SUBSTANCES IN THIS PART MUST CONFORM TO INTEL ENVIRONMENTAL
   PRODUCT SPECIFICATION (BS-MTN-001).
   A) DELRIN ACETAL RESIN, SOP NO910.
   B) PIGMENT: EAGLE 7058 (1%)
   C) COLOR: BLACK

4. PART MUST COMPLY WITH INTEL WORKMANSHIP STANDARD (96-0007-001).
   PART SHALL BE FREE OF OIL AND DEBRIS.
   FINISH: UNSPECIFIED SURFACES MUST CONFORM WITH CLASS 6 REQUIREMENTS.

5. CRITICAL TO FUNCTION DIMENSION (CTD).

6. NO GATING ALLOWED ON THESE COMPONENT MATING SURFACES.

---

PARTS LIST

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DEPARTMENT 2200 MISSION COLLEGE BLVD.
P.O. BOX 58110  SANTA CLARA, CA 95052-58110

TITLE

WASHER, HEATSINK, DELRIN

SHEET 1 OF 1

DO NOT SCALE DRAWING
APPENDIX C – LOW PROFILE STORAGE HEATSINK MECHANICAL DRAWINGS
APPENDIX D – SBB STANDARD STORAGE HEATSINK MECHANICAL DRAWINGS
APPENDIX E – ATCA* REFERENCE HEATSINK MECHANICAL DRAWINGS
NOTES:
1) UNITS ARE IN MM [IN]
2) REFERENCE THERMAL SOLUTION SHALL BE CENTERED ABOUT PACKAGE CENTER
3) MOUNTING HOLE PLATING PRESENT ON PRIMARY AND SECONDARY SIDES
APPENDIX F – CPCI* REFERENCE HEATSINK MECHANICAL DRAWINGS
NOTE:
1. UNITS: MILLIMETERS (INCHES)
2. MATERIAL: ALUMINUM, k = 200 W/m-K OR BETTER
3. LOCAL FLATNESS ZONE 0.077MM (0.003") CENTERED ON HEAT SINK BASE
4. REMOVE ALL BURRS, SHARP EDGES, GREASES, AND/OR SOLVENTS AFTER MACHINING AND FIN ASSEMBLY
5. INTEL MUST APPROVE ALL CHANGES
NOTES:
1) UNITS ARE IN MM [IN]
2) REFERENCE THERMAL SOLUTION SHALL BE CENTERED ABOUT PACKAGE CENTER
3) MOUNTING HOLE PLATING PRESENT ON PRIMARY AND SECONDARY SIDES
## Heatsink Suppliers

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<td>00Z94630201</td>
<td>Chaun-Choung Technology Corp (CCI)</td>
<td>Contact: Monica Chih, <a href="mailto:monica_chih@ccic.com.tw">monica_chih@ccic.com.tw</a>, 886-2-29952666 ext.1131</td>
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**Note:**
1. Supplier listing is provided by Intel as a convenience to its customers. Intel does not make any representations or warranties whatsoever regarding the quality, reliability, functionality, or compatibility of these devices.
2. All “Part Numbers” listed are in prototype phase and have not been verified to meet performance targets or quality and reliability requirements and are subject to change.
3. Supplier information provided in the table was deemed accurate when this document was released.
4. Customers planning on using the Intel reference design should contact the suppliers for the latest information on their product(s).
5. Customers must evaluate performance against their own product requirements.