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## Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Description</th>
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<tr>
<td>November 2016</td>
<td>002</td>
<td>Memory specification updated. Power Delivery chapter added.</td>
</tr>
<tr>
<td>December 2015</td>
<td>001</td>
<td>Initial release.</td>
</tr>
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1.0 Introduction

1.1 Overview

This design guide provides motherboard implementation recommendations for the Intel® Quark™ Microcontroller D2000 platform, based on the Intel® Quark™ Microcontroller D2000 processor. This document includes design guidelines for Intel® Quark™ Microcontroller D2000 platforms and the hardware integration aspects that must be considered when designing a platform.

This design guide has been developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues. Design recommendations are based on Intel's simulations and lab experience and are strongly recommended, if not necessary, to meet the timing and signal quality specifications. Design recommendations are based on the reference platforms designed by Intel. They should be used as an example but may not be applicable to particular designs.

*Note:* The guidelines recommended in this document are based on experience, simulation, and preliminary validation work done at Intel while developing the Intel® Quark™ Microcontroller D2000 processor-based platform. This work is ongoing, and these recommendations are subject to change.

*Caution:* If the guidelines listed in this document are not followed, it is very important that designers perform thorough signal integrity and timing simulations. Even when following these guidelines, Intel recommends the critical signals to be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

Metric units are used in some sections in addition to the standard use of U.S. customary system of units (USCS). If there is a discrepancy between the metric and USCS units, assume the USCS unit is most accurate. The conversion factor used is 1 inch (1000 mils) = 25.4 mm.

1.2 Audience and Purpose

The Intel® Quark™ Microcontroller D2000 is a highly integrated, ultra-low-power part designed to enable innovative wearable solutions with long battery life for fitness/health/wellness monitors, smart watches, and so on.

This document is intended to aid platform hardware designers in system implementation and reference design reuse by:

- Documenting the hardware implementation of a specific form factor wearable based on the Intel® Quark™ Microcontroller D2000 platform
• Providing details such as block diagrams, which illustrate connectivity, system level considerations, options, and design guidelines
• Describing the theory of operation or principles considered in deriving a design guideline

1.3 Terminology

Table 1. Terminology

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>Analog-to-Digital Converter</td>
</tr>
<tr>
<td>CRB</td>
<td>Customer Reference Board</td>
</tr>
<tr>
<td>GPIO</td>
<td>General Purpose Input/Output</td>
</tr>
<tr>
<td>I²C</td>
<td>Inter-Integrated Circuit</td>
</tr>
<tr>
<td>I2S</td>
<td>Inter-IC Sound</td>
</tr>
<tr>
<td>JTAG</td>
<td>Joint Test Action Group</td>
</tr>
<tr>
<td>OSC</td>
<td>Oscillator</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>RTC</td>
<td>Real-Time Clock</td>
</tr>
<tr>
<td>SIO</td>
<td>Serial I/O</td>
</tr>
<tr>
<td>SoC</td>
<td>System on Chip</td>
</tr>
<tr>
<td>SPI</td>
<td>Serial Peripheral Interface</td>
</tr>
<tr>
<td>UART</td>
<td>Universal Asynchronous Receiver Transmitter</td>
</tr>
<tr>
<td>XTAL</td>
<td>Crystal</td>
</tr>
</tbody>
</table>

1.4 Reference Documents

Table 2. Reference Documents

<table>
<thead>
<tr>
<th>Document</th>
<th>Document No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® Quark™ Microcontroller D2000 Datasheet</td>
<td>333577</td>
</tr>
</tbody>
</table>
2.0 System Assumptions

2.1 General Assumptions

This section covers general Intel® Quark™ Microcontroller D2000 and Intel® Quark™ Microcontroller D2000 Customer Reference Board (CRB) system topology and interface connectivity assumptions. The Intel® Quark™ Microcontroller D2000 CRB is used as a baseline reference example for guidelines.

Figure 1. Block Diagram
Figure 2. PCB Floor Plan
2.1.1 PCB Technology and Stackup

The system uses the PCB technology of a standard interconnect, Type 3, 4-layer board, no blind or buried vias. It is important to note that variations in the stackup of a motherboard, such as changes in the dielectric height, trace widths, and spacing, can impact the impedance, loss, and jitter characteristics of all the interfaces. Such changes may be intentional, or may be the result of variations in the manufacturing process. In either case, they must be properly considered when designing interconnects. This design guide applies the CRB PCB stackup and trace width/spacing that is shown in Figure 4.

*Note:* All the routing guidelines in this document are simulated based on the CRB stackup.

2.1.2 PCB Technology Considerations

The typical values, including the design and material tolerances, are centered on a nominal single line impedance specification of $50\Omega \pm 15\%$ for microstrip. Many interfaces specify a different nominal single-ended impedance. For more details on the
nominal trace width to meet those impedance targets, refer to the individual interface section.

The following general stackup recommendations should be followed:

- Microstrip layers are assumed to be built from 1/2oz. foil, plated up nominally another 1 oz.; however, the trace thickness range defined allows for significant process variance around this nominal.
- Based on the Intel® Quark™ Microcontroller D2000 layout layers, 3/4 dual stripline is assumed to be built from 1 oz. copper.
- All high-speed signals should reference solid planes over the length of their routing and should not cross plane splits. Ground referencing is preferred.
- Reference plane stitching vias must be used in conjunction with high-speed signal layer transitions that include a reference plane change. Refer to each signal group section for more specification.
- The parameter values for internal and external traces are the final thickness and width after the motherboard materials are laminated, conductors plated, and etched. Intel uses these exact values to generate the associated electrical models for simulation.

**Figure 4. Single-Ended Microstrip Diagram**
**System Assumptions**

Figure 5. Differential Microstrip Diagram

![Microstrip Diagram](image)

Table 3. Stackup Details

<table>
<thead>
<tr>
<th>Layer</th>
<th>Cu Weight</th>
<th>Proposed Thickness (mils)</th>
<th>Structure</th>
<th>Ref</th>
<th>Single End</th>
<th>Differential</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>50 Ohm ± 10%</td>
<td>90 Ohm ± 10%</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Target LW</td>
<td>Finished LW</td>
</tr>
<tr>
<td>Soldermask</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LW</td>
<td>LW/SP</td>
</tr>
<tr>
<td>L1</td>
<td>Top</td>
<td>Hoz+Plating</td>
<td>1.80</td>
<td>L2</td>
<td>3.94</td>
<td>4.2/8</td>
</tr>
<tr>
<td></td>
<td>Prepreg</td>
<td></td>
<td>2.70</td>
<td>1080</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L2</td>
<td>GND</td>
<td>1oz</td>
<td>1.20</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Core</td>
<td></td>
<td>50</td>
<td>50mil core</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L3</td>
<td>GND</td>
<td>1oz</td>
<td>1.20</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Prepreg</td>
<td></td>
<td>2.70</td>
<td>1080</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L4</td>
<td>Bottom</td>
<td>Hoz+Plating</td>
<td>1.80</td>
<td>L3</td>
<td>3.94</td>
<td>4.2/8</td>
</tr>
<tr>
<td></td>
<td>Soldermask</td>
<td></td>
<td>0.50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Finished Thickness (mils)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>62.40</td>
<td></td>
</tr>
</tbody>
</table>
2.2 Backward and Forward Coupling Coefficient Calculation

Some designs require a stackup build that is outside of the ranges provided. In this case, compare the routing electrical characteristics versus the Intel recommendation. Comparing the single-ended and differential impedances is important. However, crosstalk level, which is governed by trace spacing, is not implied by the impedance target. Calculating and comparing the backward coupling coefficient is recommended to choose proper trace spacing in cases where the selected stackup varies from the Intel recommendation. The coupling coefficient represents the source voltage percentage that is coupled to victim lines. As shown in Figure 6, \( K_b \) is defined as the backward coupling coefficient. For backward (near-end) crosstalk, inductive and capacitive coupling are of the same polarity and the noise magnitude is not a function of trace length. The backward coupling coefficient (\( K_b \)) values can be used to determine trace spacing. For forward (far-end) crosstalk, \( K_f \) inductive and capacitive coupling are of opposite polarity, and the crosstalk magnitude (\( V_{fe} \)) is proportional to both trace length and edge rate. \( K_f \) is typically a very small value in most practical designs. Therefore, Intel has not included the \( K_f \) values in the design guide. However, if the value is desired, the equation for calculating \( K_f \) is provided in Figure 7.

Figure 6. Backward Coupling Coefficient

\[
K_b = \frac{1}{4} \left( \frac{C_y}{\sqrt{C_a C_y}} + \frac{L_y}{\sqrt{L_a L_y}} \right), \\
V_{NE} = K_b \cdot V_0
\]

Figure 7. Forward Coupling Coefficient

\[
K_f = \frac{1}{2} \left( \frac{C_y}{\sqrt{C_a C_y}} - \frac{L_y}{\sqrt{L_a L_y}} \right) (L_a C_a L_b C_y)^{1/4}, \\
V_{FE} = K_f \cdot \text{Length} + \frac{dV}{dt}
\]
Breakout topologies are mainly decided by package ballout patterns and pitches. Similar geometries will be used for various stackups. Refer to the interface sections for the breakout maximum length allowed and signals not listed in Table 3.

2.3 Feature Set

A wearable can contain any feature set and capabilities supported on Intel® Quark™ Microcontroller D2000. The following is an example feature set of a typical wearable and used in the Intel® Quark™ Microcontroller D2000 form factor. Refer to the SoC Datasheet for the latest features supported on the platform.

Intel® Quark™ Microcontroller D2000 features:

- Intel® Quark™ Microcontroller D2000 SoC 32 MHz
- 32 KB flash memory (internal)
- 8 KB OTP flash (internal)
- 4 KB Data flash (internal)
- 8 KB SRAM (internal)
- 1x I²C (Master/Slave)
- 1x SPI master supports up to 4 devices
- 1x SPI slave
- 2x UART, supports 9-bit addressing mode
- 19 ADC/Comparator inputs
• 2x PWM signals
• 25 GPIOs
• Real-time clock
• Watchdog timer

Intel® Quark™ Microcontroller D2000 main expansion options:
• “Arduino Uno” compatible SIL sockets (3.3V I/O only)

Intel® Quark™ Microcontroller D2000 on-board components:
• Accelerometer/Magnetometer sensor
• UART/JTAG to USB convert for USB debug port

Other Intel® Quark™ Microcontroller D2000 connectors:
• 1x USB 2.0 Device Port – micro Type B
• On-board coin cell battery holder
• 5V input screw terminal/header (external power or Li-ion)
• EEMBC power input header

Power sources for this platform:
• External 5V DC input
• Li-ion battery (external)
• USB power (5V) via debug port
• Coin cell battery (on-board)
2.4 CRB Pin Mapping

Figure 10 shows the CRB interfaces and mapping.

Figure 10. CRB Pin Mapping Diagram
3.0 **Subsystem Details**

This chapter provides design guidelines for the SoC associated interfaces. All of the routing guidelines (W/S, isolation, length requirement) are based on CRB 4-layer PCB technology. If a different PCB stackup is implemented, the electrical guidelines (impedance, $K_b$, Insertion Loss) provided in this document must be followed to ensure that the layout can meet simulation recommendations.

3.1 **Design Recommendations**

The Intel® Quark™ Microcontroller D2000 SoC is an ultra-low-power Intel® architecture SoC that integrates an Intel® Quark™ Microcontroller D2000 processor core, memory subsystem with on-die volatile and non-volatile storage and I/O interfaces into a single system-on-chip solution.

This section presents design recommendations for the subsystems that make up the Intel® Quark™ Microcontroller D2000 platform. The sections include overview information, component selection studies, suggested routing guidelines, and additional filter and signal information for the Intel® Quark™ Microcontroller D2000 platform.

The design recommendations are developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues.

*Note:* These design recommendations should be carefully followed and any deviations should be verified through simulations. The component selection recommendations describe the components that are being considered for the Intel® Quark™ Microcontroller D2000. If and when updated boards become available, this will be noted in these sections.

The following subsystems are covered in this section:

- On-die SRAM
- Display interface
  - SPI
- Storage
  - SPI
- $I^2C$
- SPI
- Integrated Sensor
- UART
- GPIO
3.2 General Design Guideline Assumptions

The following assumptions pertain to all the subsystems discussed in this chapter.

- Package length compensation is needed. The length values are tested and measured as package-pin-to-package-pin.
- The breakout and breakin minimum spacing ratio is 1:1 for all interfaces.
- The trace width/intra-spacing for differential pairs and trace width for single-ended signals depend on the impedance.
- For analog signals, it is important to keep the analog ground return path clean of digital noise to maintain a high signal-to-noise ratio.
- For technical specifications (such as speeds, supported resolutions, and data rates), refer to the Intel® Quark™ Microcontroller D2000 Datasheet.

**Note:**
1. Follow the general guidelines in this section, if a specific interface design guide is not available.
2. All the routing guidelines in this document are simulated based on the CRB stackup.

### Table 4. Good Layout Practices

<table>
<thead>
<tr>
<th>Stitching Vias</th>
</tr>
</thead>
<tbody>
<tr>
<td>Provide stitching vias for layer transitions</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Break-In/Break-Out Regions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. If desired trace width cannot be maintained in the break regions, maintain a minimum trace width of 3.5 mil.</td>
</tr>
<tr>
<td>2. If desired trace spacing cannot be maintained in the break regions, maximize the trace spacing.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Over and Around the Voids</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Avoid routing over the voids and reference plane splits. Consult the SIE if split crossing cannot be avoided</td>
</tr>
<tr>
<td>2. When going around the voids, maintain a minimum spacing of 1xh between signal trace and void. Desirable spacing is 3xh where &quot;h&quot; is the distance to the nearest reference plane.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Lateral Distance to Reference Plane Edge</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Keep a signal trace 4xh away from the edge of the reference plane.</td>
</tr>
</tbody>
</table>
4.0 I²C Interface

I²C is a two-wire serial bus for inter-IC communication. One wire is for data, the other for clock. There is one I²C controller. The controller owns its own two-wire bus.

4.1 I²C Interface Signals

Signals for the I²C interface are illustrated in the table 6 below.

I²C features:
- One I²C interface
- Support for both master and slave operation
- Operational speeds:
  - Standard mode (0 to 100Kbps)
  - Fast mode (≤ 400Kbps)
  - Fast mode plus (≤ 1Mbps)
- 7-bit or 10-bit addressing
- Support for clock stretching by slave devices
- Multi-master arbitration
- Spike suppression
Hardware Handshake Interface to support DMA capability
- Interrupt Control
- FIFO support with 16B deep RX and TX FIFOs

4.2 Interface Routing Guidelines

I²C clock and data signals require pull-up resistors. The pull-up size is dependent on the bus capacitive load (this includes all device leakage currents).

![Figure 12. I²C Point-to-Point Topology](image)

The following table shows detailed routing requirements for the I²C bus.

### Table 5. I²C Point-to-Point Platform Routing Guidelines

<table>
<thead>
<tr>
<th>Leveraged from Intel® Quark™ SoC</th>
<th>I²C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmission Line Segment</td>
<td></td>
</tr>
<tr>
<td>I²C (SDA, SCL)</td>
<td>BRK OUT</td>
</tr>
<tr>
<td>Routing Layer (Microstrip/Stripline)</td>
<td>MS/SL</td>
</tr>
<tr>
<td>Characteristic Impedance</td>
<td>50Ω + 10% (MS)</td>
</tr>
<tr>
<td>Trace Width (w)</td>
<td>Meet impedance</td>
</tr>
<tr>
<td>Trace Spacing (S): Between SPI signals</td>
<td>5 mil minimum</td>
</tr>
<tr>
<td>Trace Spacing (S2): Between SPI signals and other signals</td>
<td>5 mil minimum</td>
</tr>
<tr>
<td>Trace Length</td>
<td>0.5&quot; max</td>
</tr>
<tr>
<td>Pull-up Resistor Rpu</td>
<td>See below</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Length matching between Data and Clk is 540 mils
2. Load = routing length capacitance + MCP = device pin capacitance
3. MCP + device pin capacitance = 10 µF
4. Cap per inch of board (pF) = 3 pF/inch (for the current stackup)
5. If the nominal trace width is not possible in the breakout area, use 4 mils as minimum trace width. Choose a stackup so that 50 Ohms will be minimum 4 mils.

4.2.1 **General Design Considerations**

The maximum bus capacitive load for each I²C bus is 400 pF. The pull-up resistor cannot be made so large that the bus time constant (Resistance X Capacitance) does not meet the I²C rise and fall time specification.
5.0 Pulse Width Modulation (PWM)

The Pulse Width Modulation (PWM) block allows individual control of the frequency and duty cycle of two output signals. The PWM block also supports use as a Timer block for the purposes of generating periodic interrupts. A possible usage model includes connecting PWM to drive a haptic driver. The two PWM pins are also multiplexed and can be used as a GPIO. Two 32-bit timers running at system clock can be configured to generate two PWM outputs.

**Figure 13. PWM**

The following is a list of PWM features:

- Two counters capable of operating in PWM Mode or Timer Mode
- **PWM Mode**
  - Configurable high and low times for each PWM Output
    - Minimum high and low time of 2 32MHz clock periods (8MHz)
    - Maximum high and low time of $2^{32}$ 32MHz clock periods (< 1Hz)
  - High and low time granularity of a single 32MHz clock period
  - Interrupt generation always on both the rising and falling edges of the PWM Output
  - Interrupt control per PWM Output:
    - Interrupt generation only on both edges of the PWM Output
    - Interrupt mask capability
- **Timer Mode**
  - 32-bit timer operating at 32MHz
  - Timer periods from 1 32MHz clock period (31.25ns) to $2^{32}$-1
5.1 PWM Signaling

The Timer and PWM block supports the generation of PWM Output signals with configurable low and high times, which allows both the duty cycle and frequency to be set.

Example PWM Output signals are shown in the following figures.

**Figure 14. Duty Cycle of 20%**

![Figure 14. Duty Cycle of 20%](image1)

**Figure 15. Duty Cycle of 50%**

![Figure 15. Duty Cycle of 50%](image2)

**Figure 16. Duty Cycle of 80%**

![Figure 16. Duty Cycle of 80%](image3)

5.2 Functional Operation

Each counter is identical, has an associated PWM Output, and can be individually configured with the following options:

- Enable
- PWM Mode or Timer Mode
- PWM Duty Cycle and Frequency
- Timer Timeout Period
- Interrupt Masking

In PWM Mode, the high and low times can be configured as follows. This assumes a nominal system clock frequency of 32MHz. The values, in nanoseconds, will differ if the system clock frequency is changed.
Table 6. PWM Timing

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value (System Clock Cycles)</th>
<th>Value (Time)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low Time Granularity</td>
<td>1</td>
<td>31.25 ns</td>
</tr>
<tr>
<td>Low Time Range</td>
<td>2 to 4294967296 (2^32)</td>
<td>62.5 ns to 134.22 s</td>
</tr>
<tr>
<td>High Time Granularity</td>
<td>1</td>
<td>31.25 ns</td>
</tr>
<tr>
<td>High Time Range</td>
<td>2 to 4294967296 (2^32)</td>
<td>62.5 ns to 134.22 s</td>
</tr>
</tbody>
</table>

PWM Mode supports the following maskable interrupt source:

- Both edges of the PWM Output signal

In Timer Mode, the timeout period can be configured as follows. This assumes a nominal system clock frequency of 32MHz. The values, in nanoseconds, will differ if the system clock frequency is changed.

Table 7. Timer Period

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value (System Clock Cycles)</th>
<th>Value (Time)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timeout Period Granularity</td>
<td>1</td>
<td>31.25 ns</td>
</tr>
<tr>
<td>Timeout Period Range</td>
<td>0 to 4294967295 (2^32 - 1)</td>
<td>0 to 134.22 s</td>
</tr>
</tbody>
</table>

Timer Mode supports the following maskable interrupt source:

- Timer expiry

Interrupts are cleared by reading the Timer N End of Interrupt register.

§
UART is one of the hardware blocks in the Serial I/O (SIO).

Main features:
- Two 16550 compliant UART interfaces
- Support for baud rates from 300 to 2M with less than 2% frequency error
- Support for hardware and software flow control
- FIFO mode support (16B TX and RX FIFOs)
- Support for HW DMA with configurable FIFO thresholds
- Support for 9-bit operation mode
- Support for RS485 and RS232
- Support for DTR/DCD/DSR/RI Modem Control Pins through GPIO pins controlled by software
6.1 Signal Descriptions

Table 8. UART Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction/Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>UART_x_TXD</td>
<td>Logic output</td>
<td>UART A single-ended Transmit data (RS232 or RS485). In RS485 mode, the differential driver is outside the SoC.</td>
</tr>
<tr>
<td>UART_x_RXD</td>
<td>Logic input</td>
<td>UART A single-ended Receive data (RS232 or RS485). In RS485 mode, the differential receiver is outside the SoC.</td>
</tr>
<tr>
<td>UART_x_RTS</td>
<td>Logic output</td>
<td>UART A Request to send (RS232)</td>
</tr>
<tr>
<td>UART_x_CTS</td>
<td>Logic input</td>
<td>UART A Clear to send (RS232)</td>
</tr>
<tr>
<td>UART_x_DE</td>
<td>Logic output</td>
<td>UART A Driver Enable (RS485 mode). Used to control the differential driver of RS485 in the platform/board. Polarity is configurable. This is multiplexed onto the UART_A_RTS pin depending on RS485 or RS232 mode of operation.</td>
</tr>
<tr>
<td>UART_x_RE</td>
<td>Logic output</td>
<td>UART B Receiver Enable (RS485 mode). Used to control the differential receiver of RS485 in the platform/board. Polarity is configurable. This is multiplexed onto the UART_B_CTS pin depending on RS485 or RS232 mode of operation.</td>
</tr>
</tbody>
</table>

Figure 18. UART 2-Via Point-to-Point Topology
### Table 9. UART Point-to-Point Topology Platform Routing Guidelines

<table>
<thead>
<tr>
<th>TXD, RXD, RTS, CTS</th>
<th>UART</th>
</tr>
</thead>
<tbody>
<tr>
<td>BRK OUT</td>
<td>Main</td>
</tr>
<tr>
<td>Transmission Line</td>
<td>L1</td>
</tr>
<tr>
<td>Segment</td>
<td></td>
</tr>
<tr>
<td>Stackup Layer</td>
<td>MS/SL</td>
</tr>
<tr>
<td>(Microstrip/</td>
<td></td>
</tr>
<tr>
<td>Stripline/Dual</td>
<td></td>
</tr>
<tr>
<td>Stripline)</td>
<td></td>
</tr>
<tr>
<td>Characteristic</td>
<td>50Ω SE10%</td>
</tr>
<tr>
<td>Impedance</td>
<td></td>
</tr>
<tr>
<td>Trace Width (w)</td>
<td>Meet</td>
</tr>
<tr>
<td></td>
<td>impedance</td>
</tr>
<tr>
<td>Min Trace Spacing</td>
<td>5 mil</td>
</tr>
<tr>
<td>(S1): Between</td>
<td></td>
</tr>
<tr>
<td>UART signals</td>
<td></td>
</tr>
<tr>
<td>Min Trace Spacing</td>
<td>5 mil</td>
</tr>
<tr>
<td>(S2): Between</td>
<td></td>
</tr>
<tr>
<td>UART signals and</td>
<td></td>
</tr>
<tr>
<td>other signals</td>
<td></td>
</tr>
<tr>
<td>Trace Segment</td>
<td>0.5” max</td>
</tr>
<tr>
<td>Length</td>
<td></td>
</tr>
</tbody>
</table>

### Table 10. UART Point-to-Point Topology Platform Routing Guidelines

<table>
<thead>
<tr>
<th>Total Trace length and Length Matching Rules (brd+pkg)</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total trace length</td>
<td></td>
<td>1-5”</td>
</tr>
<tr>
<td>No length matching required</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number of vias allowed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Via stub length</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Plane</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Continuous Ground Reference</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- If nominal trace width is not possible in breakout area, use 4 mil as min trace width. Choose a stack up so 50ohms will be min 4mils

Routing can also be extended to 10-12" in which case a series Rs of 22 Ω close to the driver will be necessary to avoid ring back TX - SOC driver, RX - UART driver Max speed = 2MBaud.

### 6.2 Features

Both UART instances are configured identically. The following is a list of the UART controller features:

- Operation compliant with the 16550 Standard
  - Start bit
  - 5 to 9 bits of data
  - Optional Parity bit (Odd or Even)
  - 1, 1.5 or 2 Stop bits
• Baud rate configurability between 300 baud and 2M baud
  – Maximum baud rate is limited by system clock frequency divided by 16.
  – Supported baud rates: 300, 1200, 2400, 4800, 9600, 14400, 19200, 38400, 57600, 76800, 115200; multiples of 38.4 Kbps and multiples of 115.2 Kbps up to 2M baud
• Auto Flow Control mode as specified in the 16750 Standard
• Hardware Flow Control
• Software Flow Control (when Hardware Flow Control is disabled)
• Hardware Handshake Interface to support DMA capability
• Interrupt Control
• FIFO support with 16B TX and RX FIFOs
• Support of RS485
  – Differential driver/receiver is external to the SoC.
  – Driver enable (DE) and Receiver enable (RE) outputs are driven from the SoC to control the differential driver/receiver.
• Fractional clock divider that ensures less than 2% frequency error for most supported baud rates.
  – Fraction resolution is 4 bits.
  – Exception: 2.07% error for 1.391 Mbaud, 2.12% for 1.882 Mbaud and 2Mbaud, 2.53% error for 1.684 Mbaud.
• 9-bit data transfer mode to support a multi-drop system where one master is connected to multiple slaves in a system.
7.0 SPI

The Serial I/O implements one SPI controller that supports master mode and slave mode. Refer to the Datasheet for additional SPI compatibility requirements and features. Support for SPI Flash devices is a key platform requirement and needed for all SoC designs.

Figure 19. SPIO

Features include:

- One SPI master interface with support for SPI clock frequencies up to 16 MHz
- One SPI slave interface with support for SPI clock frequencies up to 3.2 MHz
- Support for 4-bit up to 32-bit frame size
- Up to 4 Slave Select pins per master interface
- FIFO mode support (16B TX and RX FIFOs)
- Support for HW DMA with configurable FIFO thresholds
7.1 Features

The following is a list of the SPI master features:

- One SPI master interface
- Control of up to 4 Slave Selects
- Frame formats:
  - Motorola® SPI
  - Texas Instruments® SSP
  - National Semiconductor Microwire®
- Transfer modes:
  - Transmit & Receive
SPI

- Transmit Only
- Receive Only
- EEPROM Read

- Serial clock frequencies up to 16 MHz
- 4-bit to 32-bit frame size
- Configurable Clock Polarity and Clock Phase
- Hardware Handshake Interface to support DMA capability
- Interrupt Control
- FIFO mode support with 16B deep TX and RX FIFOs

The following is a list of the SPI slave features:

- One SPI slave interface
- Frame formats:
  - Motorola* SPI
  - Texas Instruments* SSP
  - National Semiconductor Microwire*
- Transfer modes:
  - Transmit & Receive
  - Transmit Only
  - Receive Only
  - EEPROM Read
- Serial clock frequencies up to 3.2 MHz
- 4-bit to 32-bit frame size
- Configurable Clock Polarity and Clock Phase
- Hardware Handshake Interface to support DMA capability
- Interrupt Control
- FIFO mode support with 16B deep TX and RX FIFOs

§
The SoC clocking is controlled by the Clock Control Unit (CCU). There are two primary clocks: a System clock, and an RTC clock. The CCU uses the primary clocks to generate secondary clocks to sub modules in the SoC. The secondary clocks are gated and scales versions of the primary clocks.

The SoC contains a Real-Time Clock (RTC) with 32 bytes of battery-backed SRAM. The SoC uses the RTC to keep track of time. The RTC operates from 1 Hz to 32.768 kHz. The RTC supports alarm functionality that allows scheduling an Interrupt/Wake Event for a future time. The RTC operates in all SoC power states. The RTC is powered from the same battery supply as the rest of the SoC and does not have its own dedicated supply.
Table 12. RTC Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction/Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSC32_IN</td>
<td>I Analog</td>
<td>Crystal Input: This signal is connected to the 32.768 kHz Crystal.</td>
</tr>
<tr>
<td>OSC32_OUT</td>
<td>O Analog</td>
<td>Crystal Output: This signal is connected to the 32.768 kHz Crystal.</td>
</tr>
</tbody>
</table>

8.1 Features

The following is a list of the RTC features:

- Programmable 32-bit binary counter
- Counter increments on successive edges of a Counter Clock from 1 Hz to 32.768 kHz (derived from the 32.768 kHz Crystal Oscillator clock)
- Comparator for Interrupt/Wake Event generation based on the programmed Match Value
- Support for Interrupt/Wake Event generation when only the Counter Clock is running (Fabric Clock is off)
General Purpose I/O (GPIO)

9.0 General Purpose I/O (GPIO)

The SoC contains GPIO pins and the interfaces can be active at different times. To provide maximum flexibility at the lowest cost point, some GPIO pins are shared/muxed among various interfaces. BIOS is responsible for enabling proper configuration. The SoC contains a single instance of the GPIO controller.

Figure 23. GPIO

The GPIO controller provides a total of 26 independently configurable GPIOs.

- All GPIOs are interrupt capable supporting level sensitive and edge triggered modes.
- All GPIOs support Debounce logic for interrupt sources.
- All 26 GPIOs are Always-on interrupt and wake capable.

9.1 Signal Descriptions

All GPIO pins are described in the SoC Datasheet.
Figure 24. GPIO Pin Routing Topology

Table 13. GPIO Pin Routing Guidelines

<table>
<thead>
<tr>
<th>GPIO (MV to GPIO Header/Device)</th>
<th>BRK OUT</th>
<th>Main</th>
<th>BRK IN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmission Line Segment</td>
<td>L1</td>
<td>L2</td>
<td>L3</td>
</tr>
<tr>
<td>Routing Layer</td>
<td>MS/SL</td>
<td>MS/SL</td>
<td>MS/SL</td>
</tr>
<tr>
<td>(Microstrip/Stripline)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Characteristic Impedance</td>
<td>50Ω + 10% (MS)</td>
<td>50Ω + 10% (MS)</td>
<td>50Ω + 10% (MS)</td>
</tr>
<tr>
<td></td>
<td>50Ω + 10% (SL)</td>
<td>50Ω + 10% (SL)</td>
<td>50Ω + 10% (SL)</td>
</tr>
<tr>
<td>Trace Width (w)</td>
<td>Meet impedance</td>
<td>Meet impedance</td>
<td>Meet impedance</td>
</tr>
<tr>
<td>Trace Spacing (S): Between SPI signals</td>
<td>5 mil minimum</td>
<td>2*w</td>
<td>5 mil minimum</td>
</tr>
<tr>
<td>Trace Spacing (S2): Between SPI signals and other signals</td>
<td>5 mil minimum</td>
<td>3*w</td>
<td>5 mil minimum</td>
</tr>
<tr>
<td>Trace Length</td>
<td>0.5” max</td>
<td>9” max</td>
<td>0.5” max</td>
</tr>
<tr>
<td>Trace Total Length</td>
<td>Total trace length = 10” max</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE:
1. Rs = 22 or 33Ω ideally closer to driver.
2. The modelled GPIO device is 30pF. GPIOs can drive higher loads at reduced lengths.
3. Maximum speed = 8 MHz.

9.2 Features

The following is a list of the GPIO controller features:

- 26 independently configurable GPIOs
- Separate data register bit and data direction control bit for each GPIO
- Metastability registers for GPIO read data
- Interrupt mode supported for all GPIOs, configurable as follows:
  - Active High Level
  - Active Low Level
  - Rising Edge
  - Falling Edge
  - Both Edge
- Debounce logic for interrupt sources
This section provides JTAG information.

**Figure 25. JTAG Connectivity**

**Table 14. Generic Routing Requirements**
11.0  Analog-to-Digital Converter (ADC)

The SoC implements a Successive-Approximation (SAR) Analog-to-Digital Converter (ADC), which can take 19 single-ended analog inputs for conversion. The ADC is characterized to operate over the AVDD (1.8 to 3.6V) analog input range.

Analog signal traces in the SoC should be shielded completely to minimize noise coupling and crosstalk between analog signals.

Figure 26. Analog Shielding Requirements

Example: Analog signal traces A, B and C are shielded “agnd” net with metal layers/traces adjacent, above and below the signals. An “agnd” trace should be added on top of signal C if there will be another signal route over it.

11.1  Features

The following is a list of the ADC features:

- 19:1 multiplexed single-ended analog input channels, 6 high-speed inputs and 13 low-speed inputs.
- Selectable resolution among 12-, 10-, 8-, and 6-bit (12-bit at 2.28 MSps and 6-bit at 4 MSps).
  - Maximum achievable sampling rate = (adc clock frequency) / (selres + 2).
- ADC parameters:
  - Differential Non-Linearity (DNL) = +/- 1.0 LSB
  - Integral Non-Linearity (INL) = +/- 2.0 LSB
  - SINAD = 68 dBFS
  - Offset Error = +/- 2 LSB (calibration enabled), +/- 64 LSB (calibration disabled)
- Latencies:
  - Power-up time of <= 10 us
  - 1 conversion cycle = (resolution bits + 2) cycles
- Full-scale input range is 0 to AVDD.
  - ADC Reference Voltage (Vrefp) of ADC HIP is connected to AVDD.

- Current consumption:
  - ~18 uA at 10 kSPS
  - ~240 uA at 1 MSPS
  - ~1.1 mA at 5 MSPS
  - ~15 uA standby
  - ~2 uA powerdown
12.0 Power Delivery

This chapter provides the recommendations on how to deliver the power into the Intel® Quark™ Microcontroller D2000 SoC to assure the system stability and to avoid unexpected behavior of the system, during power ON sequence especially.

12.1 DVDD Linear Regulator

Providing a load to the DVDD linear regulator at the start of power cycle using active pull-down circuit it is a very important step which must not be overlooked.

12.1.1 Operation of an Active Pull – Down Circuit

PVDD power rail charges PCB bulk capacitance via on-board VR U5. When PVDD ramps up/down due to power rail being applied/disconnected, U1 turns on and presents R1 load across DVDD which discharges PCB bulk capacitance. When PVDD reaches steady state U1 disconnects and removes R1 load across DVDD. PVDD voltage range is from 2.0V to 3.6V.

12.1.2 Implementation of an Active Pull – Down Circuit

Figure 27 illustrates a recommended implementation of an Active Pull – Down Circuit. The table provides a bill of materials used and recommended.

Figure 27. Active Pull – Down circuit implementation
Table 15. Active Pull – Down circuit BOM

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Element</th>
<th>Parameters</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2</td>
<td>MLCC</td>
<td>10uf X7R 0603 6.3Vdc</td>
<td>Farnell 1828828 or 2210949</td>
</tr>
<tr>
<td>D2</td>
<td>Schottky Diode</td>
<td>BAT48</td>
<td>Farnell 9801472</td>
</tr>
<tr>
<td>R1</td>
<td>Thick Film resistor</td>
<td>316.1% 0603</td>
<td>Any</td>
</tr>
<tr>
<td>R2</td>
<td>Thick Film resistor</td>
<td>31K6 1% 0603</td>
<td>Any</td>
</tr>
<tr>
<td>U1</td>
<td>P-MOSFET</td>
<td>Vishay SI1013R-T1</td>
<td>Farnell 2335267</td>
</tr>
</tbody>
</table>

**Note:** Not adhering to the recommendations described in this chapter may lead to a faulty power ON sequence, especially during hard reset. If a faulty power sequence occurs, the device may enter a high current state and become unresponsive. This high current state can lead to device heating.