



**Intel® Pentium® 4 Processor in
478-pin Package and Intel®
845/845E/845G/845GL/845GV/
845GE/845PE Chipset**

Platform Design Guide Addendum

**For Support with Intel® Celeron® D
Processor in 478-pin Package**

August 2004

Revision 1.1



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Revision History

Revision Number	Description	Revision Date
1.1	Added 845 and 845E support.	August 2004
1.0	Public Release	July 2004



1 Introduction

This document describes the required changes to platforms utilizing the Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process to support a migration to the Intel® Celeron® D processor in the 478-pin package. The information in this document should be used in conjunction with specifications presented in the latest version of the *Intel® Celeron® D Processors 335, 330, 325, and 320 Datasheet* and *Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process and Intel® Pentium® 4 Processor Extreme Edition Supporting Hyper-Threading Technology Datasheet*.

This design guide addendum is provided as a supplement to the platform design guidelines from documents listed in Section 1.2. This document highlights changes to the platform design guidelines for the purpose of adding support for the Intel Celeron D Processor in the 478-pin package. All other design implementation details from the platform design guidelines are applicable for the Intel Celeron D processor in the 478-pin package support, given the limitations described in Section 2.

1.1 State of the Data

This document contains compatibility requirements between the Intel Celeron D processor in the 478-pin package and the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process with the 845 family of chipset based platforms.

The board-level electrical design changes (system bus routing recommendations, new signal definition, system bus termination recommendations, etc.) are the most up to date design details for the Intel Celeron D processor in the 478-pin package. This includes the pinout changes and their implementation for a “compatible platform” (see Section 1.3 for definition).

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document:

Table 1. References

Document	Document Number
<i>Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845G / 845GL / 845GV Chipset Platform Design Guide</i>	http://developer.intel.com/design/chipsets/designex/298654.htm
<i>Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845GE / 845PE Chipset Platform Design Guide</i>	http://www.intel.com/design/chipsets/designex/251925.htm
<i>Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845 Chipset Platform for SDR Design Guide</i>	http://www.intel.com/design/chipsets/designex/298354.htm
<i>Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 845 Chipset Platform for DDR Platform Design Guide</i>	http://www.intel.com/design/chipsets/designex/298605.htm
<i>Intel® Pentium® 4 Processor in the 478-Pin Package and Intel® 845E Chipset Platform for DDR Design Guide</i>	http://www.intel.com/design/chipsets/designex/298652.htm
<i>Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines</i>	http://www.intel.com/design/Pentium4/guides/252161.htm
<i>Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process and Intel® Pentium® 4 Processor Extreme Edition Supporting Hyper-Threading Technology Datasheet</i>	http://www.intel.com/design/Pentium4/datashts/298643.htm
<i>Voltage Regulator-Down (VRD) 10.0 Power Delivery Design Guide</i>	http://developer.intel.com/design/Pentium4/guides/252885.htm
<i>Intel® Pentium® 4 Processor VR-Down Design Guidelines</i>	http://developer.intel.com/design/Pentium4/guides/249891.htm
<i>Intel® Architecture Software Developer's Manual</i>	
Volume 1: Basic Architecture	http://www.intel.com/design/Pentium4/manuals/253665.htm
Volume 2A: Instruction Set Reference A - M	http://developer.intel.com/design/pentium4/manuals/253666.htm
Volume 2B: Instruction Set Reference N - Z	http://developer.intel.com/design/pentium4/manuals/253667.htm
Volume 3: System Programming Guide	http://developer.intel.com/design/pentium4/manuals/253668.htm
<i>ITP700 Debug Port Design Guide</i>	http://developer.intel.com/design/Xeon/guides/249679.htm
<i>Intel® Celeron® D Processors 335, 330, 325, and 320 Datasheet</i>	http://www.intel.com/design/celeron/datashts/302353.htm
<i>Intel® Celeron® D Processor for Embedded Applications Thermal Design Guide</i>	http://www.intel.com/design/intarch/designgd/302647.htm
<i>Intel® 845G/845GL/845GV Chipset Datasheet: Intel® 82845G/82845GL/82845GV Graphics and Memory Controller Hub (GMCH)</i>	http://developer.intel.com/design/chipsets/datashts/290746.htm?iid=ipp_845gvchpst+info_ds&
<i>Intel® 845GE/845PE Chipset Datasheet: Intel® 82845GE Graphics and Memory Controller Hub (GMCH) / Intel® 82845PE Memory Controller Hub (MCH)</i>	http://developer.intel.com/design/chipsets/datashts/251924.htm?iid=ipp_845gechpst+info_ds&



1.3 Definitions

- **Intel® Celeron® D Processor in the 478-pin Package** - The Intel Celeron D Processor in the 478-pin package is an Intel 32-bit microprocessor intended for desktop platforms. It is based on a new 90 nm process and will include core frequency improvements, microarchitectural improvements and additional instructions. The Intel Celeron D processor in the 478-pin package uses the 478-pin socket.
- **Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process** - The Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process is the second-generation processor based on Intel NetBurst® microarchitecture. It is based on the 0.13 micron processor and has 512-Kbytes of L2 cache.
- **Compatible Platform** - For the purpose of this document, a compatible platform is an 845/845E/845G/855GL/845GV/845GE/845PE chipset-based design, originally built to support the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process processor, and has been modified to add support for the Intel Celeron D processor in the 478-pin package. The compatible platform should implement the design guidelines listed in this document including VRD 9.0 or VRD10.0 design requirements, changes in processor circuits, system bus pin changes to support both the Intel Celeron D Processor in the 478-pin package and the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.

2 Compatibility Overview

Implementing the changes outlined in this document will assist in making an Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process-based system design compatible with the Intel Celeron D processor in the 478-pin package. Compatibility will ultimately be limited by factors such as the ability of the system to supply the required current for this future generation processor, maintaining the processor power supply within the voltage tolerances specified for the Intel Celeron D processor, and adequate system cooling capability. This design guideline is used as a supplement to the standard platform design guidelines and is used only when designing in support for the Intel Celeron D processor in the 478-pin package. These standard platform design guidelines include the *Intel® Pentium® 4 Processor in 478-pin package and Intel® 845G/845GL/845GV Chipset Platform Design Guide*; the *Intel® Pentium® 4 Processor in 478-pin package and Intel® 845GE/845PE Chipset Platform Design Guide*; the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 845 Chipset Platform for SDR Platform Design Guide*; the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 845 Chipset Platform for DDR Platform Design Guide*; and the *Intel® Pentium® 4 Processor in the 478-Pin Package and Intel® 845E Chipset Platform for DDR Design Guide*.

2.1 Power Delivery

Power delivery for the Intel Celeron D processor in the 478-pin package: VRD 9.0 is required and VRD 10.0 is compatible.

2.2 System Bus Design

Supporting the Intel Celeron D processor in the 478-pin package will require some 478-pin socket signal definition changes as well. The changes will not interfere with the proper operation of the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process. Refer to Section 6.1 for details on the pinout changes.

Bus lengths and routing strategies for the 533 MHz system bus remain unchanged from the recommendations provided in the platform design guidelines.

2.3 Thermal and Mechanical Design

The same mechanical retention solution employed for an Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process will be appropriate for use with the Intel Celeron D processor in the 478-pin package at frequencies intended for the compatible design. Heatsinks designed to support the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process FMB2 requirements will support the Intel Celeron D processor in the 478-pin package requirements. Refer to [Section 7.0](#) for details on thermal and mechanical design changes.



2.4 BIOS Support

BIOS-level changes are required to support the Intel Celeron D processor in the 478-pin package. Please contact your Intel representative to get the latest microcode update.

3 Power Delivery Changes

The compatible platform should meet the FMB2 requirements of the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and the Intel Celeron D processor in the 478-pin package requirements. To support this feature the compatible platform should meet the requirements of the Voltage Regulator-Down (VRD) 9.0 or 10.0 Design Guidelines. Designs will continue to utilize the power delivery guidelines outlined in the platform design guidelines listed in Section 1.2, along with the additional requirements recommended in this section. This includes layout and decoupling recommendations found in these platform design guidelines. Refer to Section 8.1 for further considerations.

See Section 4.2 for additional voltage regulator requirements.

Table 2. Intel® Celeron® D Processor in the 478-Pin Package FMB Guideline

	Intel® Pentium® 4 Processor with 512 KB L2 cache on 0.13 Micron Process FMB2	Intel® Celeron® D Processor in the 478-Pin Package
IccMax	70 A	73 A
VRD (Loadline)	9.0	9.0 or 10.0
VR_TDC	N/A	62A
Power (TDP)	82 W	73 W
Max T _C	70 °C	67 °C
Ta	42 C	42 C

3.1 Decoupling Requirements

Table 3. Decoupling Requirements Table for the Intel® Celeron® D Processor³

Capacitance	ESR (each)	ESL (each)	Ripple Current Rating (each)
10 aluminum polymer, 560 µF	9.28 mΩ, max	6.4 nH, max	4.080 A, Note 1
3 AL Electrolytic, 3300 µF	12 mΩ	5 nH	Note 1
24 0805 package 10 µF			Note 1, 2
14 1206 package, 10 µF	3.5 mΩ, typ	1.15 nH, typ	Note 1, 2

NOTES:

1. The ESR, ESL and ripple current values in this table are based on the values used in power delivery simulation by Intel, and are not vendor specifications.
2. If only 1206s are used, 38 are required.
3. Supports both Intel Pentium 4 processor on 0.13 micron process and Intel Celeron D processor.

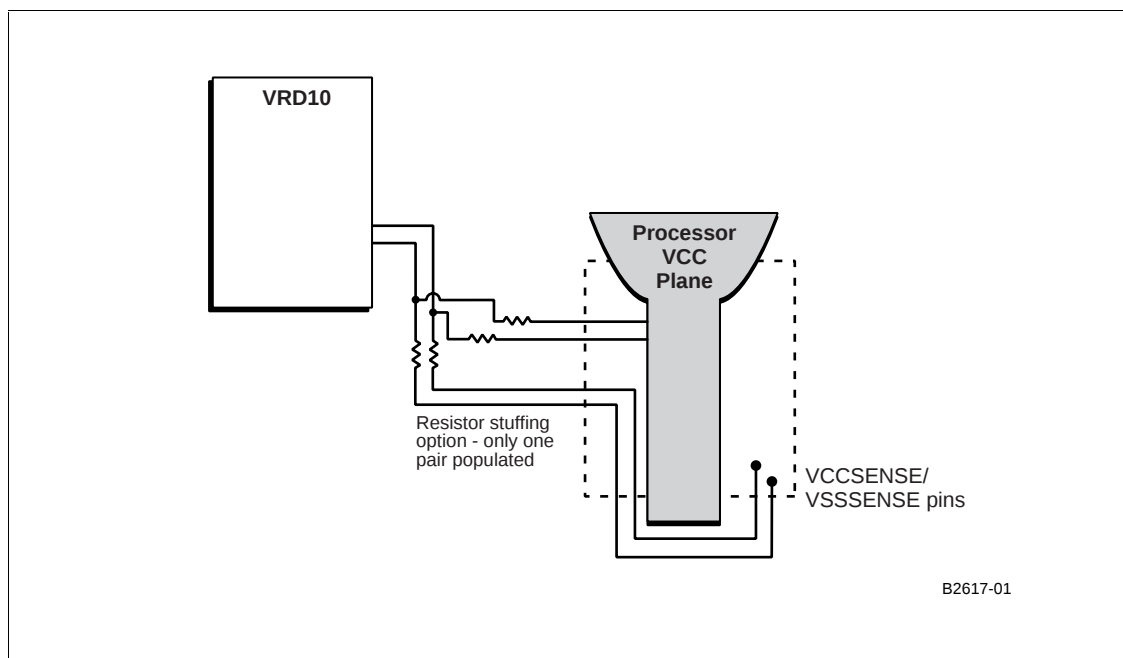
4 Processor Circuits

This section outlines all system bus pinout changes that are required for platforms to support the Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process as well as the Intel® Celeron® D processor.

4.1 Socket Sense

The compatible platform should have additional routing from the VRD 10.0 to the processor and resistor stuffing options should be used to select socket sense option.

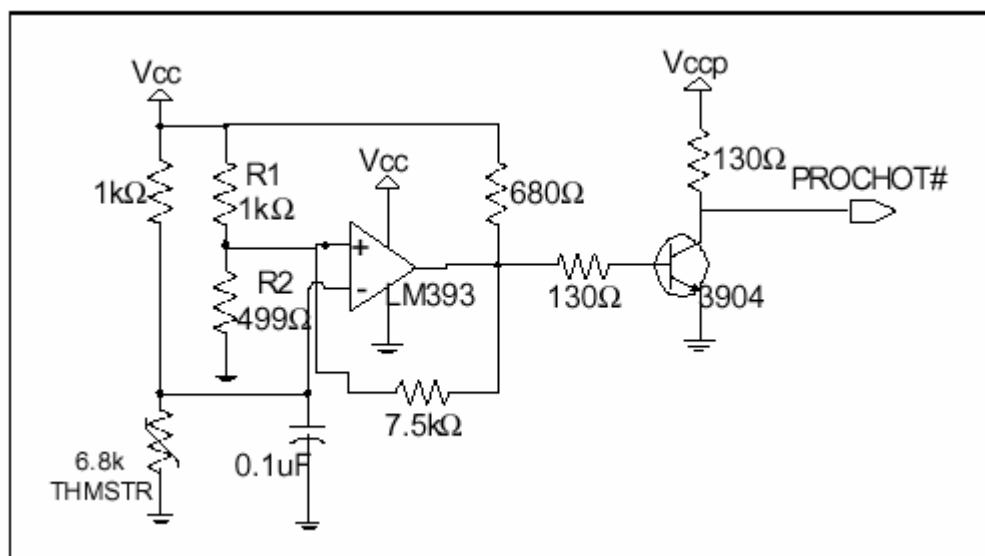
Figure 1. Socket Sense Circuit



4.2 Bidirectional PROCHOT#

Intel recommends that the compatible system boards be designed to support the Intel Celeron D processor in the 478-pin package. These guidelines include an ICC_MAX and a VR_TDC (VR Thermal Design Current). The processor voltage regulator (VR) solution should be designed to support ICC_MAX electrically for brief time periods. The voltage regulator solution should also be designed to support a minimum of VR_TDC indefinitely within the envelope of system operating conditions. The VR_TDC limits of the system board are typically governed by the system board thermal limits. Intel recommends that system boards designed to the above guidelines implement a VR thermal monitor circuit.

Figure 2. Bi-Directional PROCHOT# Circuit



For this circuit implementation, the thermistor (THMSTR) should be placed in the hottest area of the VR. As the thermistor heats up, its resistance goes down. This creates an error voltage based on the resistance of the thermistor and the voltage reference provided by R1 and R2. The values of R1 and R2 should be adjusted to calibrate the circuit for a specific system board design so that it asserts PROCHOT# when the VR reaches its thermal limit. The values of R1 and R2 in Figure 2 are included as an example. The value of R2 is adjusted to calibrate the circuit so that PROCHOT# is asserted when the VR reaches its thermal limit in the system that it is intended to operate in. An adequate VR cooling solution should be implemented such that VR_TDC current levels can be maintained indefinitely.

4.3 Dual Loadline Implementation (VRD 10.0 Only)

The Intel® Celeron® D Processor in the 478-pin package and the Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process have different loadline requirements. Therefore, the VRD 10.0 controller must switch feedback networks depending on which processor is installed. The BOOTSELECT signal is used by the VRD to detect whether an Intel Celeron D processor in the 478-pin package or Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process is inserted into the processor socket and switches the feedback network. Figure 3 shows a diagram of the switching network, while Figure 4 shows an example of the switching circuit.

4.4 SYS_RESET# Timing Circuitry

If restarting the system after a shutdown caused by a catastrophic thermal event (THERMTRIP# event) and in order to protect the Intel Celeron D processor in the 478-pin package during the reset state, there are two reset timing requirements that have to be met: CPUPWRGD active to CPURST inactive, and VCC_CPU active to CPUPWRGD assertion.

The front-panel reset switch (FP_RST #) is connected to SYS_RESET# to reset the whole system. The reset timing may violate the system stability conditions. To prevent this condition, the following two schematics are recommended to generate a 20 ms $\pm$ 20% pulse reset signal. Compatible platforms should implement either of the two timing circuits shown in Figure 5 or Figure 6.

Figure 5. Reset Timing Circuit - 1

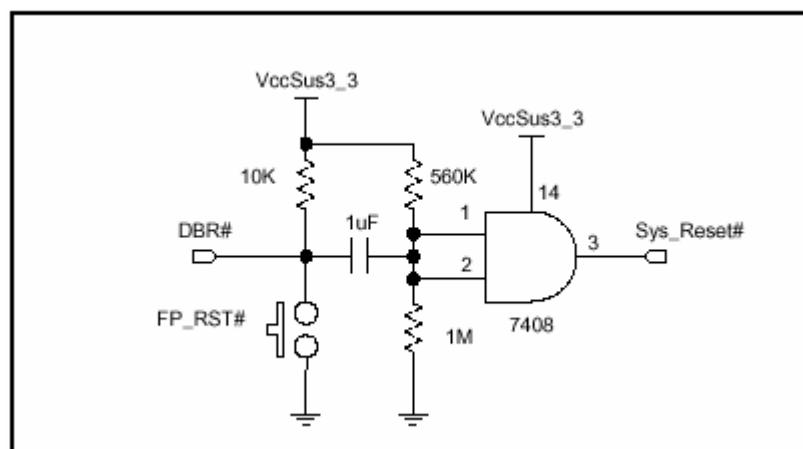
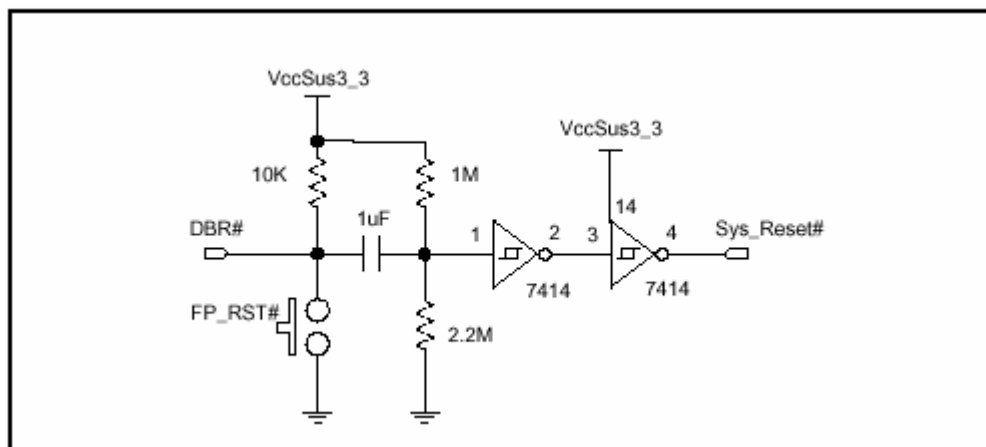


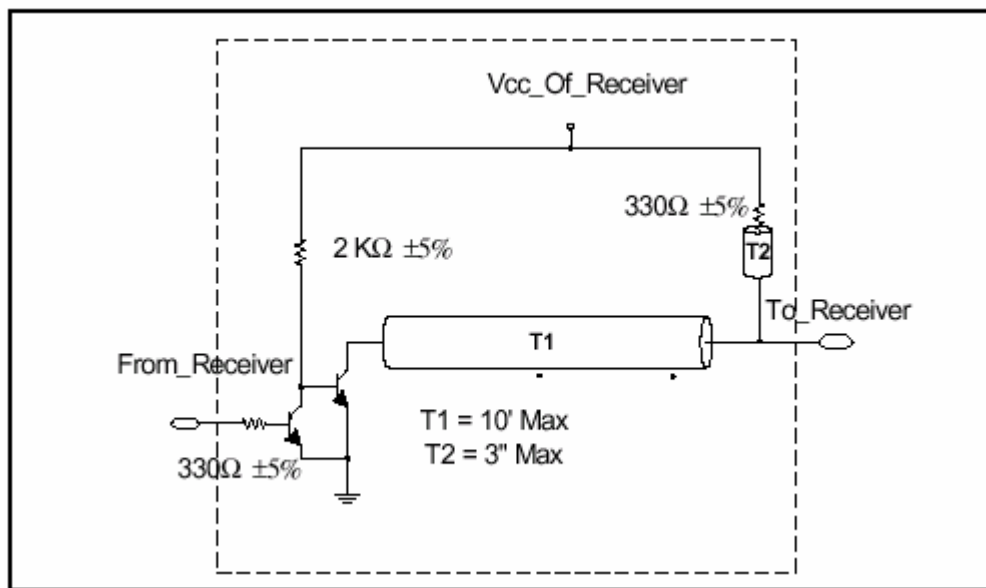
Figure 6. Reset Timing Circuit - 2



4.5 INIT# Signal Topology

The recommended logic circuit for level shifting the INIT# signal has changed. The lower processor VID has led to changes in the circuit and input resistor values.

Figure 7. Voltage Translation of INIT#



5 ***BIOS Support***

5.1 **Microcode Updates**

The Intel Celeron D processor in the 478-pin package will use variable size microcode updates (as large as 16K bytes in size) that compliant with the new INT 15h Variable Size Microcode Update Specification. For the latest Microcode Update, please contact your local Intel Representative.

5.2 **Processor Identification**

The Intel Celeron D processor in the 478-pin package will not support the Brand ID feature of the CPUID instruction as a method of processor identification. The BIOS should use the Brand String feature of the CPUID instruction as the preferred processor identification mechanism.

6 System Bus Design Changes

6.1 Pinout Changes

There are several new signal assignments - some of which are required for platforms supporting the Intel® Celeron® D processor in the 478-pin package - from the pinout defined for the current Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process. The platform must be designed with the 478-pin socket in order to mechanically support the Intel Celeron D processor on 90 nm process and in the 478-pin package.

Table 4. 478-Pin Socket Pin-Map Changes

Pin	Old Name ¹	New Name ²	Signal Group ²
AD3	RESERVED	VID5	Output
AF3	RESERVED	VCCVIDLB	Power/Other
AD2	RESERVED	VIDPWRGD	Power/Other
AE26	Vss	OPTIMIZED/COMPAT#	Input
AD1	Vss	BOOTSELECT	Input

NOTES:

1. Definition associated with the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.
2. Definition associated with the Intel Celeron D processor in the 478-pin package. These new pin definitions do not interfere with the proper operation of the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.

6.1.1 Pinout Definitions and Implementation Details

This section provides specific changes to the processor pinout to migrate a design from supporting only the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process to one supporting the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and the Intel Celeron D processor in the 478-pin package. Only pinout changes marked as “Required Platform Changes” must be implemented by the platform and impact the connectivity of the 478-pin socket pinout.

6.1.1.1 VID5

The compatible platforms should connect the VID5 pin to the VRD 10.0. A pull-up resistor of 1 K Ω to a 3.3 V or less supply is required.

For the VRD 9.0 platform, leave VID5 as NC.

6.1.1.2 VCCVID and VCCVIDLB (Required Platform Change)

For platforms that were designed to only support Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process, the VCCVID output is tied to a 1.2-V linear regulator on the

platform. This regulator provides the power to the processor logic responsible for driving the VID[5:0] and the BSEL[1:0] outputs. The compatible platform must connect the VCCVID pin to the VCCVIDLB pin to 1.2 V. A 5-mil trace is acceptable to connect these pins. The current specification for the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process VCCVID supply is 30 mA. To support the Intel Celeron D processor in the 478-pin package, a linear regulator that can supply at least 150 mA should be used.

Note: To support VRD 9.0 or VRD 10.0, the VCCVID and VCCVIDLB pins must be tied together, and 1.2 V must be supplied to the VCCVID (AF4) and VCCVIDLB (AF3) pin.

6.1.1.3 VIDPWRGD

To support VRD 10.0, VIDPWRGD should be pulled up to 1.2V VCCVID through a 680 Ω resistor. The VIDPWRGD pin does not have an on-die pull-up resistor and should follow the timing and voltage requirements below:

Table 5. VIDPWRGD Specifications

VIDPWRGD	Minimum	Maximum
Input Low Voltage (V_{IL})	–	0.3 V
Input High Voltage (V_{IH})	0.9 V	–
Falling Edge Voltage (V_T)	–	0.95 V
Rise Time -	–	150 ns

Note: To support VRD 9.0, VIDPWRGD pin (AD2) needs to get a power good signal from the VCCVID regulator.

6.1.1.4 OPTIMIZED/COMPAT# Pin

For VRD 10.0 and 9.0, the OPTIMIZED/COMPAT# input informs the processor about the type of platform where the processor is installed. This signal must be connected to Vss to signify that the platform offers compatibility with the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process. This signal must use a 60 Ω pull-down resistor to connect to Vss.

6.1.1.5 BOOTSELECT

To support VRD 10.0, refer to Section 4.3.

To support VRD 9.0, the BOOTSELECT must be NC. The Intel Celeron D processor will not boot if it sees GND on the BOOTSELECT pin (AD1). Leaving BOOTSELECT NC will support both the Celeron D processor and the Intel Pentium 4 processor with 512K cache on 0.13 micron process.

CAUTION: The design guidelines for BOOTSELECT with respect to this application note are only for the Intel Celeron D Processor in the 478-pin package. If the Intel Pentium 4 processor on 90 nm process is plugged in, serious damage or malfunction could result in the board.

7 Thermal - Mechanical Changes

The Intel Celeron D processor in the 478-pin package is mechanically identical to the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process package except for a slight difference in total package height, defined as the distance from the bottom of the substrate to the top of the integrated heat spreader (IHS). The table below compares the two processor package heights. Currently, the package height change has been determined to have no impact on the existing Intel reference thermal and mechanical solution. Customers planning on reusing their Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process thermal and mechanical solutions for the Intel Celeron D processor in the 478-pin package should consider the package height change and ensure that their designs have adequate performance over the package height range.

The dimensions for the bottom-side component keep-out zones have been slightly changed for the Intel Celeron D processor in the 478-pin package. The zone dimension for the Intel Celeron D processor in the 478-pin package is 1.5 mm [0.059 in], while the dimension for the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process is 1.25 mm [0.049 in]. Any components mounted on the motherboard in the socket center opening must not intrude into this keep-out zone underneath the processor package.

Refer to the *Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process Thermal Design Guidelines* or *Intel® Celeron® D Processor for Embedded Applications Thermal Design Guidelines* for more details, depending on your application. Document locations are listed in Section 1.2

Table 6. Intel® Celeron® D Processor in the 478-Pin Package Height Comparison

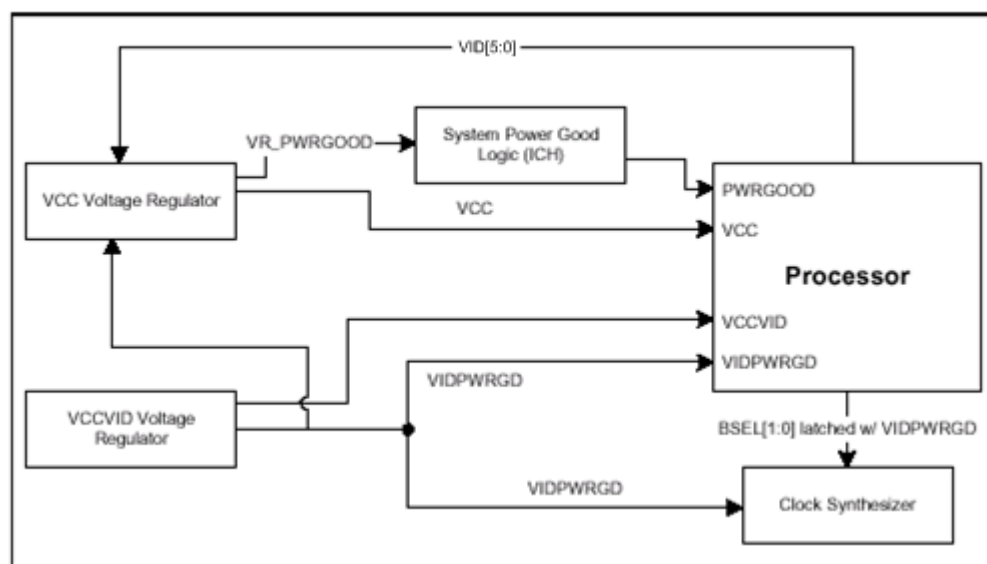
	Intel® Celeron® D Processor on 90 nm Process and the Intel® Celeron® D Processor in the 478-Pin Package	Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process
Minimum Package Height	3.308 mm [0.130 in]	3.246 mm [0.128 in]
Maximum Package Height	3.848 mm [0.151 in]	3.670 mm [0.144 in]

8 Other Platform Considerations

8.1 Power Sequencing

To support the Intel Celeron D processor in the 478-pin package, there are additional power sequencing requirements. This is mainly due to the addition of a VIDPWRGD input to the Intel Celeron D processor in the 478-pin package. This input is designed to indicate when the VCCVID voltage is stable and the processor is able to drive the VID[5:0] outputs. A block diagram of an example implementation is shown in Figure 8.

Figure 8. Voltage Sequence Block Diagram



8.2 System Bus Signal Levels

The estimated value for the VID code of the Intel Celeron D processor in the 478-pin package is 1.25 V to 1.40 V. The current VID value for VCC of the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process is 1.475 to 1.550 V. The specific values will be determined as the processors are fully characterized. Refer to *Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process* and *Intel® Pentium® 4 Processor Extreme Edition Supporting Hyper-Threading Technology Datasheet* and *Intel® Celeron® D Processors 335, 330, 325, and 320 Datasheet*, depending on your application. Document locations are listed in Section 1.2.

Table 7 outlines AGTL+ signal level definition differences between the Intel Celeron D processor on 90 nm process and in the 478-pin package and the Intel Pentium 4 processor with 512-KB L2



cache on 0.13 micron process. I/O buffer models are available for the Intel Celeron D processor on 90 nm process and in the 478-pin package; simulation should be performed for the system bus interface to ensure that these levels are met. Other bus electrical characteristics are expected to be compatible with the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process specifications.

Because the system bus is terminated to the processor's power supply, all chipset devices and other logic tied to the system bus must be capable of operating within the voltage ranges associated with the Intel Celeron D processor in the 478-pin package and Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process. Refer to Table 7 for estimated voltage ranges of these processors.

Table 7. System Bus Voltage Estimates

Processor	VID	VCC Max	VCC Min	GTLREF Max	GTLREF Min	Notes
Intel® Celeron® D Processor in the 478-pin Package	1.25 to 1.4	Note 2	Note 2	$2/3 * V_{CC} + 2\%$	$2/3 * V_{CC} - 2\%$	1
Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 Micron Process	1.475 to 1.550	Note 2	Note 2	$2/3 * V_{CC} + 2\%$	$2/3 * V_{CC} - 2\%$	1

NOTES:

1. These values are for reference only. The processor datasheet contains the actual specifications for the processor.
2. VCC minimum and maximum specifications are processor core frequency specific. VCC maximum is dependent on ICC for a given frequency. VCC minimum is rated at any ICC value for a given frequency.

Any platform logic that connects to system bus signals must be compatible with the lower voltages of the Intel Celeron D processor in the 478-pin package and must tolerate the lower reference point if the logic connects to AGTL+ system bus signals.

8.3 Voltage Tolerance for Special Signals

There are two groups of Intel Celeron D processor in the 478-pin package signals that will have a higher voltage tolerance to ease compatibility with components enabled for the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process. The VID[5:0] and BSEL[1:0] outputs are designed to tolerate a pull-up voltage of up to 3.3 V. This allows the Intel Celeron D processor in the 478-pin package to be used with existing clock synthesizers and voltage regulators that pull these signals up to a 3.3 V power supply.

8.4 Designing to Support Debug Tools

Intel strongly recommends that platforms be designed to support run time control tools, such as the Intel in-target probe (ITP) and logic analyzer interfaces. These tools can greatly reduce the time required to troubleshoot platform, BIOS, and application issues.

8.4.1 Run Time Control Tools

Existing run time control tools, like the ITP, are able to support the Intel Celeron D processor in the 478-pin package with only a software update.

8.4.2 Logic Analyzer Interface (LAI)

Initial debug of a compatible platform utilizing the Intel Celeron D processor is supported by current LAIs for the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.

8.4.3 Intel® Celeron® D Processor in the 478-Pin Package Checklist

Table 8. Compatible System Checklist

Name	Intel® Celeron® D Processor in the 478-Pin Package	Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process
VRD 10 or 9	X (VRD 10 or 9)	X (VRD 10 or 9)
Decoupling Requirements	X (see Table 3)	
Dual loadline Implementation	VRD 9 not required VRD 10 recommended	
Pinout changes	X	
Mechanical Changes	X	
Microcode update	X	