Intel® Atom™ Processor
N450, D410 and D510 for
Embedded Applications

Thermal Design Guide

February 2010

Revision 1.0
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This document contains information on products in the design phase of development.

Hyper-Threading Technology requires a computer system with a processor supporting HT Technology and an HT Technology enabled chipset, BIOS and operating system. Performance will vary depending on the specific hardware and software you use. For more information including details on which processors support HT Technology, see http://www.intel.com/info/hyperthreading.

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§
Introduction

1 Introduction

This document describes the thermal characteristics of the Intel® Atom™ Processor N450, D410 and D510 and provides guidelines for meeting the thermal requirements imposed on a single-processor system.

The goals of this document are to:

- Identify the thermal and mechanical specification for the device
- Describe a reference thermal solution that meets the specifications

A properly designed thermal solution adequately cools the device die temperature at or below the thermal specification. This is accomplished by providing a suitable local ambient temperature, ensuring adequate local airflow, and minimizing the die to local ambient thermal resistance. Operation outside the functional limits can degrade system performance and may cause permanent changes in the operating characteristics of the component.

This document describes thermal and mechanical design guidelines for the Intel® Atom™ processors in the micro Flip Chip Ball Grid Array (micro-FCBGA) package. For thermal design information on other Intel® components, refer to the respective component datasheets.

1.1 Reference Documents

<table>
<thead>
<tr>
<th>Document</th>
<th>Document No./Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® Atom™ Processor D400 and D500, Thermal Mechanical Specifications and Design Guideline</td>
<td>See Note 1</td>
</tr>
<tr>
<td>Intel® Atom™ Processor (Pineview) Thermal Model User’s Guide</td>
<td>See Note 1</td>
</tr>
<tr>
<td>Intel® Atom™ Processor N450 and Intel® Atom Processor D410</td>
<td>See Note 1</td>
</tr>
<tr>
<td>Desktop SKUs: Intel® Atom™ Processor D400 and D500 Datasheet Volume 1 and 2</td>
<td>See Note 1</td>
</tr>
<tr>
<td>Mobile SKUs: Intel® Atom™ Processor N400 Datasheet Volume 1 and 2</td>
<td>See Note 1</td>
</tr>
</tbody>
</table>

Note:

1. For the latest revision and order number of this document, contact your Intel field sales representative.
## 1.2 Terminology

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>°C</td>
<td>Degrees Celsius</td>
</tr>
<tr>
<td>EDS</td>
<td>External Design Specification</td>
</tr>
<tr>
<td>FCBGA</td>
<td>Flip Chip Ball Grid Array</td>
</tr>
<tr>
<td>in.</td>
<td>Inches</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>$T_{J\text{-MAX}}$</td>
<td>The maximum junction temperature of the processor, as specified in the processor datasheet (°C)</td>
</tr>
<tr>
<td>$T_{J\text{-MIN}}$</td>
<td>The minimum junction temperature of the processor, as specified in the processor datasheet (°C)</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Junction Temperature of Processor</td>
</tr>
<tr>
<td>$T_{LA}$</td>
<td>Local ambient temperature (°C). This is the temperature measured inside the chassis, approximately 1&quot; upstream from a component heatsink.</td>
</tr>
<tr>
<td>$T_S$</td>
<td>Heatsink Temperature measured at geometric center of heatsink base.</td>
</tr>
<tr>
<td>TIM</td>
<td>Thermal Interface Material – the thermally conductive compound between the heatsink and processor. This material fills air gaps and voids, and enhances spreading of the heat from the processor to the heatsink.</td>
</tr>
<tr>
<td>TDP</td>
<td>Thermal Design Power</td>
</tr>
<tr>
<td>W</td>
<td>Watt</td>
</tr>
<tr>
<td>$\Psi_{JS}$</td>
<td>Junction-to-sink thermal characterization parameter. Defined as $(T_J - T_S) / \text{TDP}$</td>
</tr>
<tr>
<td>$\Psi_{SA}$</td>
<td>Sink-to-ambient thermal characterization parameter. Defined as $(T_S - T_{LA}) / \text{TDP}$</td>
</tr>
<tr>
<td>$\Psi_{JA}$</td>
<td>Junction-to-ambient thermal characterization parameter. Defined as $(T_{J\text{-MAX}} - T_{LA}) / \text{TDP}$</td>
</tr>
</tbody>
</table>
2 Package Information

The Intel® Atom Processor N450, D410 and D450 all utilize a 22 x 22 mm, 559 ball micro-FCBGA package as shown in Figure 1 and Figure 2. Note that there are capacitors near the die. Although the die-side capacitors are slightly shorter than the silicon die, be careful to avoid contacting the capacitors with electrically conductive materials or a heatsink base. Consider using an insulating material between the capacitors and heatsink to prevent capacitor shorting.

The data provided in this section is for reference purposes only. Refer to the device’s most recent datasheet for up-to-date information. In the event of conflict, the device’s datasheet supersedes data shown in these figures.
Figure 1. Intel® Atom™ Processor D510 micro-FCBGA Package
Figure 2. Intel® Atom™ Processor N450 and D410 micro-FCBGA Package
2.1 Thermal Design Power

Thermal Design Power (TDP) specifications for the Intel® Atom processors N450, D410 and D510 are listed in Table 1. TDP is the recommended design point for the thermal solution’s power dissipation and is based on running worst-case, real-world applications and benchmarks at maximum component temperature. The thermal solution must ensure that the processor junction temperature limit is never exceeded under TDP conditions.

Table 1. Thermal Specification

<table>
<thead>
<tr>
<th>CPU SKU</th>
<th># of Cores</th>
<th>Frequency (GHz)</th>
<th>TDP (W)</th>
<th>TJ-MAX (°C)</th>
<th>TJ-MIN (°C)</th>
<th>Die Size (cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® Atom™ Processor N450</td>
<td>1</td>
<td>1.66</td>
<td>5.5</td>
<td>100</td>
<td>0</td>
<td>0.659</td>
</tr>
<tr>
<td>Intel® Atom™ Processor D410</td>
<td>1</td>
<td>1.66</td>
<td>10</td>
<td>100</td>
<td>0</td>
<td>0.659</td>
</tr>
<tr>
<td>Intel® Atom™ Processor D510</td>
<td>2</td>
<td>1.66</td>
<td>13</td>
<td>100</td>
<td>0</td>
<td>0.866</td>
</tr>
</tbody>
</table>

2.2 Package Mechanical Requirements

The processor package has mechanical load limits, maximum static and dynamic load limits, which should not be exceeded during their respective stress conditions. These include heat-sink installation, removal, mechanical stress testing, and standard shipping conditions.

- When a compressive static load is necessary to ensure thermal performance of the thermal interface material between the heat-sink base and the processor die, it should not exceed the corresponding specification.
- When a compressive static load is necessary to ensure mechanical performance, it should remain in the minimum/maximum range specified.
- No portion of the substrate should be used as a mechanical reference or load-bearing surface for the thermal or mechanical solution.

Table 2. Processor Loading Specification

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Compressive Load</td>
<td>24N [5.4 lbf]</td>
<td>67N [15 lbf]</td>
<td>1, 2, 3</td>
</tr>
</tbody>
</table>

NOTES:
1. These specifications apply to uniform compressive loading in a direction normal to the processor die.
2. This is the minimum and maximum static force that can be applied by the heat-sink and retention solution to maintain the heat-sink and processor interface.
3. These specifications are based on limited testing for design characterization. Loading limits are for the package only.
4. Processor loading specifications are for dual and single core.
3.1 Processor Power Dissipation

An increase in processor operating frequency not only increases system performance, but also increases the processor power dissipation. The relationship between frequency and power is generalized in the following equation:

\[ P = CV^2F \]

(where \( P \) = power, \( C \) = capacitance, \( V \) = voltage, \( F \) = frequency)

From this equation, it is evident that power increases linearly with frequency and with the square of voltage. In the absence of power saving technologies, ever increasing frequencies will result in processors with power dissipations in the hundreds of watts. Fortunately, there are numerous ways to reduce the power consumption of a processor, and Intel is aggressively pursuing low power design techniques. For example, decreasing the operating voltage, reducing unnecessary transistor activity, and using more power efficient circuits can significantly reduce processor power consumption.

An on-die thermal management feature called Thermal Monitor is available on the processor. It provides a thermal management approach to support the continued increases in processor frequency and performance. By using a highly accurate on-die temperature sensing circuit and a fast acting Thermal Control Circuit (TCC), the processor can rapidly initiate thermal management control. The Thermal Monitor can reduce cooling solution cost, by allowing thermal designs to target TDP.

3.2 Thermal Monitor Implementation

The Thermal Monitor helps control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel® Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active. With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable. An under designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss and may affect the long-term reliability of the processor.

In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously. The Intel® Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks when the processor silicon reaches its maximum operating temperature. The Intel® Thermal Monitor uses two modes to activate the TCC: automatic mode and on-demand mode. If both modes are activated, automatic
mode takes precedence. There is only one automatic mode called Intel® Thermal Monitor 1 (TM1). This mode is selected by writing values to the MSRs of the processor. After automatic mode is enabled, the TCC will be activated only when the internal die temperature reaches the maximum allowed value for operation. The Intel® Thermal Monitor automatic mode must be enabled through BIOS for the processor to be operating within specifications. Intel recommends TM1 be enabled on Intel® Atom™ processors. When TM1 is enabled and a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, the automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active.

The Intel® Thermal Monitor automatic mode must be enabled through the BIOS for the processor to be operating within specifications. Intel recommends TM1 be enabled on the processors. TM1 feature can be referred to as Adaptive Thermal Monitoring features.

The TCC may also be activated via on-demand mode. If bit 4 of the ACPI Intel® Thermal Monitor control register is written to a 1, the TCC will be activated immediately independent of the processor temperature. When using the on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Intel Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in on-demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-demand mode may be used at the same time automatic mode is enabled, however, if the system tries to enable the TCC via on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode will take precedence. An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor also includes one ACPI register, one performance counter register, three MSR, and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel Thermal Monitor feature. The Intel Thermal Monitor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#. PROCHOT# will not be asserted when the processor is in the Stop Grant power states; hence, the thermal diode reading must be used as a safeguard to maintain the processor junction temperature within maximum specification. If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters one of the above power states with PROCHOT# already asserted, PROCHOT# will remain asserted until the processor exits the Stop Grant power state and the processor junction temperature drops below the thermal trip point. If Intel Thermal Monitor automatic mode is disabled, the processor will be operating out of specification.

Regardless of mode, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon reaches a temperature of approximately 125°C. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is
independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in the Intel® Atom Processor D510 External Design Specification.

The Thermal Monitor consists of the following components:

- A highly accurate on-die temperature sensing circuit
- A bi-directional signal (PROCHOT#) that indicates if the processor has exceeded its maximum temperature or can be asserted externally to activate the Thermal Control Circuit (TCC)
- A Thermal Control Circuit that will attempt to reduce processor temperature by rapidly reducing power consumption when the on-die temperature sensor indicates that it has exceeded the maximum operating point.
- Registers to determine the processor thermal status.

3.2.1 Thermal Monitor 2

*Note:* Intel® Atom Processor D410 and D510 support TM1
Intel® Atom Processor N450 supports TM1 and TM2

The processor supports an enhanced Thermal Control Circuit. In conjunction with the existing Thermal Monitor logic, this capability is known as Thermal Monitor 2. This enhanced TCC provides an efficient means of reducing the power consumption within the processor and limiting the processor temperature.

When Thermal Monitor 2 is enabled, and a high temperature situation is detected, the enhanced TCC will be activated. The enhanced TCC causes the processor to adjust its operating frequency (by dropping the bus-to-core multiplier to its minimum available value) and input voltage identification (VID) value. This combination of reduced frequency and VID results in a reduction in processor power consumption.

A processor enabled for Thermal Monitor 2 includes two operating points, each consisting of a specific operating frequency and voltage. The first operating point represents the normal operating condition for the processor.

The second operating point consists of both a lower operating frequency and voltage. When the TCC is activated, the processor automatically transitions to the new frequency. This transition occurs very rapidly (to the order of 5 microseconds). During the frequency transition, the processor is unable to service any bus requests, all bus traffic is blocked. Edge-triggered interrupts will be latched and kept pending until the processor resumes operation at the new frequency.

Once the new operating frequency is engaged, the processor will transition to the new core operating voltage by issuing a new VID code to the voltage regulator. The voltage regulator must support VID transitions to support Thermal Monitor 2. During the voltage change, it will be necessary to transition through multiple VID codes to reach the target operating voltage. Each step will be one VID table entry (i.e., 12.5 mV steps). The processor continues to execute instructions during the voltage transition. Operation at the lower voltage reduces the power consumption of the processor, providing a temperature reduction.

Once the processor has sufficiently cooled, and a minimum activation time has expired, the operating frequency and voltage transition back to the normal system.
operating point. Transition of the VID code will occur first, in order to ensure proper operation once the processor reaches its normal operating frequency. Refer to Figure 3 for an illustration of this ordering.

**Figure 3. Thermal Monitor 2 Frequency and Voltage Ordering**

![Diagram showing Thermal Monitor 2 Frequency and Voltage Ordering]

<table>
<thead>
<tr>
<th>VID</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>VID_{TM2}</td>
<td>T_{TM2}</td>
</tr>
</tbody>
</table>

3.3 **PROCHOT # Signal**

The primary function of the PROCHOT# signal is to provide an external indication that the processor has exceeded its maximum operating temperature. While PROCHOT# is asserted, the TCC will be active. Assertion of the PROCHOT# signal is independent of any register settings within the processor. It is asserted any time the processor die temperature reaches the trip point.

PROCHOT# can be configured via the BIOS as an output or bi-directional signal. As an output, PROCHOT# will go active when the processor temperature of either core exceeds its maximum operating temperature. This indicates the TCC has been activated. As an input, assertion of PROCHOT# will activate the TCC for both cores. The TCC will remain active until the system de-asserts PROCHOT#.

As an output, the temperature at which the PROCHOT# signal becomes active is individually calibrated during manufacturing. The power dissipation of each processor affects the set point temperature and once configured in the manufacturing process, the temperature at which the PROCHOT# signal is asserted is not re-configurable.

One possible application is the thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low)
which activates the TCC, the VR can cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR, and rely on bi-directional PROCHOT# signal only as a backup in case of system cooling failure.

**Note:** A thermal solution designed to meet the thermal specifications should rarely experience activation of the TCC as indicated by the PROCHOT# signal going active.

### 3.4 Thermal Control Circuit

The Thermal Control Circuit portion of the Thermal Monitor must be enabled for the processor to operate within specifications. The Thermal Monitor’s TCC, when active, will attempt to lower the processor temperature by reducing the processor power consumption. In the original implementation of thermal monitor this is done by changing the duty cycle of the internal processor clocks, resulting in a lower effective frequency. When active, the TCC turns the processor clocks off and then back on with a predetermined duty cycle. The duty cycle is processor specific, and is fixed for a particular processor. The maximum time period the clocks are disabled is ~3 μs. This time period is frequency dependent and higher frequency processors will disable the internal clocks for a shorter time period. Figure 4 illustrates the relationship between the internal processor clocks and PROCHOT#.

Performance counter registers, status bits in model specific registers (MSRs), and the PROCHOT# output pin are available to monitor the Thermal Monitor behavior.

**Figure 4. Concept of Clocks under Thermal Monitor Control**

![Concept of Clocks under Thermal Monitor Control](image)
3.5 Operation and Configuration

To maintain compatibility with previous generations of processors, which have no integrated thermal logic, the Thermal Control Circuit portion of Thermal Monitor is disabled by default. During the boot process, the BIOS must enable the Thermal Control Circuit. Thermal Monitor must be enabled to ensure proper processor operation.

The Thermal Control Circuit feature can be configured and monitored in a number of ways. OEMs are required to enable the Thermal Control Circuit while using various registers and outputs to monitor the processor thermal status. The Thermal Control Circuit is enabled by the BIOS setting a bit in an MSR (model specific register). Enabling the Thermal Control Circuit allows the processor to attempt to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines. When the Thermal Control Circuit has been enabled, processor power consumption will be reduced after the thermal sensor detects a high temperature (i.e., PROCHOT# assertion). The Thermal Control Circuit and PROCHOT# transitions to inactive once the temperature has been reduced below the thermal trip point, although a small time-based hysteresis has been included to prevent multiple PROCHOT# transitions around the trip point. External hardware can monitor PROCHOT# and generate an interrupt whenever there is a transition from active-to-inactive or inactive-to-active. PROCHOT# can also be configured to generate an internal interrupt which would initiate an OEM supplied interrupt service routine.

Regardless of the configuration selected, PROCHOT# will always indicate the thermal status of the processor.

The power reduction mechanism of the thermal monitor can also be activated manually using an “on-demand” mode. Refer to Section 3.6 for details on this feature.

3.6 On-Demand Mode

For testing purposes, the Thermal Control Circuit may also be activated by setting bits in the ACPI MSRs. The MSRs may be set based on a particular system event (e.g., an interrupt generated after a system event), or may be set at any time through the operating system or custom driver control thus forcing the thermal control circuit on. This is referred to as “on-demand” mode. Activating the thermal control circuit may be useful for thermal solution investigations or for performance implication studies. When using the MSRs to activate the on-demand clock modulation feature, the duty cycle is configurable in steps of 12.5%, from 12.5% to 87.5%.

For any duty cycle, the maximum time period the clocks are disabled is ~3 μs. This time period is frequency dependent, and decreases as frequency increases. To achieve different duty cycles, the length of time that the clocks are disabled remains constant, and the time period that the clocks are enabled is adjusted to achieve the desired ratio. For example, if the clock disable period is 3 μs, and a duty cycle of ¼ (25%) is selected, the clock on time would be reduced to approximately 1 μs [on time (1 μs) ÷ total cycle time (3 + 1) μs = ¼ duty cycle]. Similarly, for a duty cycle of 7/8 (87.5%), the clock on time would be extended to 21 μs [21 ÷ (21 + 3) = 7/8 duty cycle].

In a high temperature situation, if the thermal control circuit and ACPI MSRs (automatic and on-demand modes) are used simultaneously, the fixed duty cycle determined by automatic mode would take precedence.
3.7 System Consideration

Intel requires the Thermal Monitor and Thermal Control Circuit to be enabled for all processors. The thermal control circuit is intended to protect against short term thermal excursions that exceed the capability of a well designed processor thermal solution. Thermal Monitor should not be relied upon to compensate for a thermal solution that does not meet the thermal profile up to the thermal design power (TDP).

Each application program has its own unique power profile, although the profile has some variability due to loop decisions, I/O activity and interrupts. In general, compute intensive applications with a high cache hit rate dissipate more processor power than applications that are I/O intensive or have low cache hit rates.

The processor TDP is based on measurements of processor power consumption while running various high power applications. This data is used to determine those applications that are interesting from a power perspective. These applications are then evaluated in a controlled thermal environment to determine their sensitivity to activation of the thermal control circuit. This data is used to derive the TDP targets published in the processor datasheet.

A system designed to meet the thermal specification of $T_{\text{JUNCTION-MAX}}$ values published in the processor datasheet greatly reduces the probability of real applications causing the thermal control circuit to activate under normal operating conditions. Systems that do not meet these specifications could be subject to more frequent activation of the thermal control circuit depending upon ambient air temperature and application power profile. Moreover, if a system is significantly under designed, there is a risk that the Thermal Monitor feature will not be capable of maintaining a safe operating temperature and the processor could shutdown and signal THERMTRIP#.

3.8 Operating System and Application Software

The Thermal Monitor feature and its thermal control circuit work seamlessly with ACPI compliant operating systems. The Thermal Monitor feature is transparent to the application software since the processor bus snooping, ACPI timer, and interrupts is active at all times.

3.9 THERMTRIP# Signal

In the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon temperature reaches its operating limit. At this point the system bus signal THERMTRIP# becomes active and power must be removed from the processor. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. Refer to the processor datasheet for more information about THERMTRIP#.

The temperature at which the THERMTRIP# signal becomes active is individually calibrated during manufacturing. The temperature at which THERMTRIP# becomes active is roughly parallel to the thermal profile and greater than the PROCHOT# activation temperature. Once configured, the temperature at which the THERMTRIP# signal is asserted is neither re-configurable nor accessible to the system.
3.10 Cooling System Failure Warning

It may be useful to use the PROCHOT# signal as an indication of cooling system failure. Messages could be sent to the system administrator to warn of the cooling failure, while the thermal control circuit would allow the system to continue functioning or allow a normal system shutdown. If no thermal management action is taken, the silicon temperature may exceed the operating limits, causing THERMTRIP# to activate and shut down the processor. Regardless of the system design requirements or thermal solution ability, the Thermal Monitor feature must be enabled to ensure proper processor operation.

3.11 Digital Thermal Sensor

The Intel® Atom Processors N450, D410 and D510 introduce the Digital Thermal Sensor (DTS) as the on-die sensor to use for processor temperature monitoring. The Processor will have both the DTS and thermal diode enabled. The DTS monitors the same sensor that activates the TCC (see Section 3.4). The readings from the DTS are relative to the activation of the TCC. The DTS value where TCC activation occurs is 0 (zero).

The Intel® Atom™ processors’ DTS can only be accessed via an MSR. The value read via the MSR is an unsigned number of degrees C away from TCC. Multiple digital thermal sensors can be implemented within the package without adding a pair of signal pins per sensor as required with the thermal diode. The digital thermal sensor is easier to place in thermally sensitive locations of the processor than the thermal diode. This is achieved due to a smaller footprint and decreased sensitivity to noise. Since the DTS is factory set on a per-part basis there is no need for the health monitor components to be updated at each processor family.

3.12 Thermal Diode

The processor incorporates an on-die PNP transistor whose base emitter junction is used as a thermal “diode”, with its collector shorted to ground. The thermal diode can be read by an off-die analog/digital converter (a thermal sensor) located on the motherboard or a stand-alone measurement kit. The thermal diode may be used to monitor the die temperature of the processor for thermal management or instrumentation purposes but is not a reliable indication that the maximum operating temperature of the processor has been reached. When using the thermal diode, a temperature offset value must be read from a processor MSR and applied. The reading of the external thermal sensor (on the motherboard) connected to the processor thermal diode signals will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the external thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die, and time based variations in the die temperature measurement.

Time based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the TJ temperature can change. Offset between the thermal diode based temperature reading and the Intel Thermal Monitor reading may be characterized using the Intel Thermal Monitor’s Automatic mode activation of the thermal control circuit. This temperature offset must be taken
into account when using the processor thermal diode to implement power management events.

This offset is different than the diode $T_{offset}$ value programmed into the Intel® Atom™ processor Model Specific Register (MSR). Table 3 and Table 4 provide the diode interface and specifications. The transistor model parameters shown in Table 4 provide more accurate temperature measurements when the diode ideality factor is closer to the maximum or minimum limits. Contact your external sensor supplier for their recommendation. The thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Table 3. Thermal Diode Interface

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Pin/Ball Number</th>
<th>Signal Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>THERMDA_1</td>
<td>D30</td>
<td>Thermal diode anode</td>
</tr>
<tr>
<td>THERMDA_2</td>
<td>C30</td>
<td>Thermal diode anode (on D510 only)</td>
</tr>
<tr>
<td>THERMDC_1</td>
<td>E30</td>
<td>Thermal diode cathode</td>
</tr>
<tr>
<td>THERMDC_2</td>
<td>D31</td>
<td>Thermal diode anode (on D510 only)</td>
</tr>
</tbody>
</table>

Table 4. Thermal Diode Parameters using Transistor Model

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>IFW</td>
<td>Forward Bias Current</td>
<td>5</td>
<td>200</td>
<td>μA</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>IE</td>
<td>Emitter Current</td>
<td>5</td>
<td>200</td>
<td>μA</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>nQ</td>
<td>Transistor Ideality</td>
<td>0.997</td>
<td>1.001</td>
<td>1.015</td>
<td>2,3,4</td>
<td></td>
</tr>
<tr>
<td>Beta</td>
<td></td>
<td>0.25</td>
<td>0.65</td>
<td></td>
<td>2,3</td>
<td></td>
</tr>
<tr>
<td>RT</td>
<td>Series Resistance</td>
<td>2.79</td>
<td>4.52</td>
<td>6.24</td>
<td>Ω</td>
<td>2,5</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized across a temperature range of 50–100°C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, $n_Q$, represents the deviation from ideal transistor model behavior as exemplified by the equation for the collector current:
   \[ IC = IS * (e^{qVBE/n_QkT} - 1) \]
   where $IS$ = saturation current, $q$ = electronic charge, $VBE$ = voltage across the transistor base emitter junction (same nodes as $VD$), $k$ = Boltzmann Constant, and $T$ = absolute temperature (Kelvin).
5. The series resistance, $RT$, provided in the Diode Model Table (Table 4) can be used for more accurate readings as needed.

When calculating a temperature based on the thermal diode measurements, a number of parameters must be either measured or assumed. Most devices measure the diode ideality and assume a series resistance and ideality trim value, although are capable of also measuring the series resistance. Calculating the temperature is then accomplished using the equations listed under Table 4. In most sensing devices, an expected value for the diode ideality is designed into the temperature calculation equation. If the designer of the temperature sensing device assumes a perfect diode, the ideality value (also called $n_{trim}$) will be 1.000. Given that most diodes are not perfect, the designers usually select an $n_{trim}$ value that more closely matches the behavior of the diodes in the processor. If the processor diode ideality deviates from
that of the \( n_{\text{trim}} \), each calculated temperature will be offset by a fixed amount. This temperature offset can be calculated with the equation:

\[
T_{\text{error(nf)}} = T_{\text{measured}} \times (1 - \frac{n_{\text{actual}}}{n_{\text{trim}}})
\]

where \( T_{\text{error(nf)}} \) is the offset in degrees C, \( T_{\text{measured}} \) is in Kelvin, \( n_{\text{actual}} \) is the measured ideality of the diode, and \( n_{\text{trim}} \) is the diode ideality assumed by the temperature sensing device.
4 Thermal Solution Requirement

4.1 Characterizing the Thermal Solution Requirement

The idea of a "thermal characterization parameter", $\Psi$ (Greek letter Psi), is a convenient way to characterize the performance needed for the thermal solution and to compare thermal solutions in identical situations (i.e., heating source, local ambient conditions, etc). A thermal characterization parameter is calculated using total package power, whereas actual thermal resistance, $\Theta$ (theta), is calculated using actual power dissipated between two points. Measuring actual power dissipated into a heatsink is difficult, since some of the power is dissipated via heat transfer into the package, board and surrounding air.

The junction-to-local ambient thermal characterization parameter ($\Psi_{JA}$) is used as a measure of the thermal performance of the overall thermal solution. It is defined by the following equation, and measured in units of °C/W:

\[
\Psi_{JA} = \frac{T_{J-MAX} - T_{LA}}{TDP}
\]

Where:

$\Psi_{JA}$ = Junction-to-local ambient thermal characterization parameter (°C/W)

$T_{J-MAX}$ = Maximum allowed device temperature (°C)

$T_{LA}$ = Local ambient temperature near the device (°C)

TDP=Thermal Design Power (W), assumes all power dissipates through the top surface of the device.

The junction-to-local ambient thermal characterization parameter, $\Psi_{JA}$, comprises $\Psi_{JS}$, which includes the thermal interface material thermal characterization parameter, and $\Psi_{SA}$, the sink-to-local ambient thermal characterization parameter.
Equation 4-2. Junction- to- Local Ambient Thermal Charaterization Parameter

\[ \Psi_{JA} = \Psi_{JS} + \Psi_{SA} \]

Where:

- \( \Psi_{JS} \) = Thermal characterization parameter of the package and TIM (°C/W)
- \( \Psi_{SA} \) = Thermal characterization parameter from heatsink-to-local ambient (°C/W)
- \( \Psi_{JS} \) is strongly dependent on the thermal conductivity and thickness of TIM between heatsink and die.
- \( \Psi_{SA} \) is a measure of the thermal characterization parameter from the geometric center of the heatsink base to the local ambient air. \( \Psi_{SA} \) depends on the heatsink material, thermal conductivity, and geometry. It is also depends strongly on the air velocity through the fins of the heatsink. As the ambient temperature increases, the required \( \Psi_{SA} \) decreases, hence the heatsink dimension increases or the airflow needs to be increased so that the thermal solution target performance can be met. Figure 5 illustrates the combination of the different thermal characterization parameters.

Figure 5. Processor Thermal Characterization Parameter Relationships
4.2 Example: Calculating the Required Thermal Performance

The process to determine the required thermal performance needed to cool the device includes:

- Define a target component temperature $T_{J,M} -$ Max and corresponding TDP
- Define a target local ambient temperature $T_{LA}$
- Use Equation 4-1. and Equation 4-2 to determine the required thermal performance needed to cool the device

The following example illustrates how to determine the appropriate performance targets:

Assume:

- $T_{DP} = 15.0$W and $T_{J,MAX} = 100^\circ C$ (Available from processor datasheet)
- Local processor ambient temperature, $T_{LA}=35^\circ C$

Then the following could be calculated using Equation 4-1 for the given processor frequency:

$$\Psi_{JA} = \frac{T_{J,M} - T_{LA}}{TDP} = \frac{100 - 35}{13} = 5^\circ C/W$$

To determine the required heatsink performance, a heatsink solution provider would need to determine $\Psi_{JS}$ performance for the selected TIM and mechanical load configuration. If the heatsink solution were designed to work with TIM material performing at $\Psi_{JS} \leq 0.55^\circ C/W$ solving from Equation 4-2, the performance of the heatsink required is:

$$\Psi_{SA} = \Psi_{JA} - \Psi_{JS} = 5.0 - (0.55) = 4.45^\circ C/W$$

If the local processor ambient temperature is increased to 40°C, the same calculation can be carried out to determine the new thermal solution performance requirement.

$$\Psi_{JA} = \frac{T_{J,M} - T_{LA}}{TDP} = \frac{100 - 40}{13} = 4.6^\circ C/W$$

It is evident from the above calculations that an increase in the local ambient temperature has a significant effect on the junction-to-ambient thermal resistance requirement. This effect can increase cost, heatsink size, heatsink weight, or a higher system airflow rate.

Table 5 summarizes the thermal budget required to adequately cool the processor. Since the data is based on air data at sea level, a correction factor would be required to estimate the thermal performance at other altitudes.
<table>
<thead>
<tr>
<th>SKU, TDP</th>
<th>$\Psi_{JA}$ (°C/W) at $T_{LA} = 35^\circ C^{1,2}$</th>
<th>$\Psi_{JA}$ (°C/W) at $T_{LA} = 55^\circ C^{1,2}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® Atom™ processor N450, 5.5 W</td>
<td>11.81</td>
<td>8.18</td>
</tr>
<tr>
<td>Intel® Atom™ processor D410, 10W</td>
<td>6.50</td>
<td>4.50</td>
</tr>
<tr>
<td>Intel® Atom™ processor D510, 13W</td>
<td>5.00</td>
<td>3.46</td>
</tr>
</tbody>
</table>

1. $T_{LA}$ is defined as the local (internal) ambient temperature measured approximately 1” upstream from the device.
2. $\Psi_{JA}$ is determined by $(T_{J-MAX} - T_{LA})/TDP$, so this value will change if any parameter changes.
5 Reference Thermal Solution

5.1 Thermal Solution Design Considerations

The thermal solution in a fanless system can be placed into two general categories: stand-alone natural convection heatsink and conduction cooling system. A stand-alone natural convection heatsink is similar to a typical, extruded heatsink. The heatsink contacts only the component that it is cooling. This thermal solution is placed inside the chassis and relies on natural air movement created by a temperature difference instead of forced convection from an airflow source to remove the heat.

A conduction cooled system is one in which the heat dissipating component(s) are attached to the chassis and rely on a majority of the heat being conducted into the chassis. This type of solution relies on natural convection to remove heat from the chassis. In this case, the heat dissipating components are usually directly attached to the chassis or utilize a heatpipe to transfer the heat to the chassis.

The next section explains the major factors that influence a fanless thermal solution design.

5.2 Thermal Solution Design Factors

1. **Thermal design power (TDP) and ambient temperature**: The TDP for a component is probably the biggest factor in determining whether a component can be cooled in a fanless system. In most cases, a target power for fanless cooling is less than 10 W, but this depends on the target ambient temperature. Intel® Atom™ processors N450, D410 and D510 are good candidates for fanless cooling even though the power is slightly above 10 W.

2. **The area of the surface on which the heat transfer takes place**: Without enhancements, this is the surface of the processor (bare die). One method to improve thermal performance is to attach a heatsink to the bare die. A heatsink can increase the effective heat transfer surface area by conducting heat from the die and into the surrounding air through fins attached to the heatsink base.

3. **The conduction path from the heat source to the heatsink fins**: Providing a direct conduction path from the heat source to the heatsink fins and selecting materials with higher thermal conductivity typically improves heatsink performance. The length, thickness, and conductivity of the conduction path from the heat source to the fins directly impact the thermal performance of the heatsink. In particular, the quality of the contact between the die surface and the heatsink base has a greater impact on the overall thermal solution performance as processor cooling requirements become stricter.

4. **Thermal Interface Material (TIM)**: TIM fills the gap between die and the bottom surface of the heatsink, improving the overall performance of the stackup (TIM-heatsink). With an extremely poor heatsink interface flatness or roughness, the TIM may not adequately fill the gap. The TIM thermal
performance depends on its thermal conductivity and the pressure applied to it.

5. **Heat Distribution**: In the case of conduction cooled system thermal solutions, it is important to optimize the heat distribution from heat source(s). This can be achieved by using multiple heatpipes to transport the heat to a larger area of the system chassis.

6. **Fin thickness and fin pitch**: In a natural convection solution, the air flow is induced by the phenomenon of hot air moving to the opposite of gravitational direction. Therefore, the fin to fin spacing and the thickness of the fins play a critical role in improving the air flow and reducing thermal resistance. Thermal solution designers need to optimize these parameters to obtain the best performance while designing for manufacturability.

7. **Location of venting in the chassis**: The vents in the chassis allow for heat to escape and for external air that is at a lower temperature to enter the chassis. Critical components with the highest amount of power generation (usually the processor) need to be placed close to the chassis vents. This placement facilitates the movement of air caused by thermodynamic effects.

8. **Heat trapped inside fully enclosed system**: For fanless systems that are fully enclosed, not all heat sources have direct heat conduction to the heatsink(s) or chassis. Therefore, the heat generated could eventually lead to internal heat accumulation until system failure results due to raising the internal local ambient temperature (TLA). System thermal solution designers must take into account this potential impact to temperature inside the chassis.

9. **Maximum allowable chassis temperature**: The external chassis temperature should be considered in applications where a fanless system will have potential users come in contact with the chassis. Due to the amount of heat transfer to the outer chassis there is potential for the surface to burn a user who comes in contact with the device. System designers need to monitor the surface temperature of the chassis to ensure that end users will not be harmed and the chassis temperature meets applicable standards.

To analyze all these design factors it is recommended that designers utilize third-party CFD thermal analysis software such as Flotherm* and Icepak*. Intel has package models for the Intel® Atom™ processors N450, D510 and D510 product line available for these software packages. Contact your Intel Field representative for more information.

### 5.3 Natural Convection Heatsink

**Experimental Test Setup**

Intel has developed reference thermal solutions that are suitable for the Intel® Atom™ processor in natural convection environments. These heatsinks were tested in a test chamber as shown in Figure 6. These tests were performed on the component level to characterize the performance of the heatsink. System designers will have to use this performance data apply it to their system design, which is best achieved through CFD computer simulations.
The heatsinks were tested using a processor Thermal Test Vehicle (TTV). A TTV is a device that thermally and physically represents the processor package. However, instead of being a functional processor, it has a heat resistor and temperature sensors within the die. A TTV is used to characterize a thermal solution because the amount of power dissipated can be accurately controlled and the temperature can be monitored. When testing on a real system, it is difficult to measure the power dissipated by the processor into the heatsink. By using a TTV a thermal engineer can have confidence in the heatsink thermal performance.

The TTV is placed in the natural convection test chamber and Figure 6 shows the dimensions of the test chamber. The test chamber is open at the bottom and top to allow air to enter and exit the chamber. The top part of the chamber has a top plate and vents to allow air to escape, but also prevents outside factors from influencing the test data (such as air conditioning). This test setup is used to determine key thermal solution parameters $\Psi_{JS}$ and $\Psi_{SA}$.

Figure 6. Isometric View of Natural Convection Test Chamber

Two different heatsink designs for the Intel® Atom™ processor were tested. One has a footprint of 64 x 64 mm and the other 40 x 40 mm. PCM45F was used as thermal interface material between the die and the heatsink.

Table 6 and Table 7 summarize thermal characterization performance for the Intel® Atom™ Processor reference heatsinks in the natural convection environment. Based on lab testing the TIM $\Psi_{JS}$ obtained is 0.25 °C-cm²/W. This value could increase over
time due to degradation of the material. It is recommended that system designers work with their TIM suppliers to obtain TIM thermal performance.

**Table 6. Experimental Thermal Solution Performance for 64 x 64mm Heatsink (Intel part # E85767-001)**

<table>
<thead>
<tr>
<th>SKU, TDP</th>
<th>$\Psi_{SA}$ (°C/W)</th>
<th>$\Psi_{JA}$ (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® Atom™ processor N450, 5.5 W</td>
<td>2.36</td>
<td>3.17</td>
</tr>
<tr>
<td>Intel® Atom™ processor D410, 10W</td>
<td>2.36</td>
<td>3.17</td>
</tr>
<tr>
<td>Intel® Atom™ processor D510, 13W</td>
<td>2.36</td>
<td>3.09</td>
</tr>
</tbody>
</table>

The above results are based on lab testing.

**5.4 Mechanical Design**

Heatsinks are attached to the board using 2 pushpins. Figure 7 illustrates an example of the thermal solution assembly.

**Figure 7. Mini-ITX Natural Convection Reference Heatsink Assembly (Natural Convection) Intel part # E85767-001**
### Table 7. Experimental Thermal Solution Performance for 40 x 40 mm Heatsink (Intel part# E85766-001)

<table>
<thead>
<tr>
<th>SKU, TDP</th>
<th>$\Psi_{SA}$ (ºC/W)</th>
<th>$\Psi_{JA}$ (ºC/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® Atom™ processor N450, 5.5 W</td>
<td>5.22</td>
<td>6.77</td>
</tr>
<tr>
<td>Intel® Atom™ processor D410, 10W</td>
<td>5.22</td>
<td>6.77</td>
</tr>
<tr>
<td>Intel® Atom™ processor D510, 13W</td>
<td>5.22</td>
<td>6.50</td>
</tr>
</tbody>
</table>

Based on the above thermal performance of the heatsink, the design engineer can determine if the heatsinks will meet their specific thermal design requirements. Refer to Figure 17 for Intel part # E85766-001.

### 5.5 Fanless System Design Examples

This section details case studies for fanless system design for the Intel® Atom™ processor D510 in a ventilated system environment. A system designer wishing to develop a stand-alone natural convection thermal solution would apply the same design principles. It is very important to note that there is not a one size fits all fanless thermal solution. Fanless designs are custom designs and each application needs to be modeled and tested.

#### 5.5.1 System Level Simulations for Print Imaging

Cooling feasibility analysis was performed for a print imaging chassis (X,Y=181mm, Z=61mm) both in vertical and horizontal orientation for an ambient temperature of 55ºC and for a TIM thermal impedance of $R = 0.40$ ºC-cm²/W. The following figures show the board component layout and resulting airflow movement created through natural convection. It is important for system designers to analyze the movement of heat within the system. The location and size of the chassis vents will affect the movement of airflow and the ability to create a system level thermal design will help to meet component temperature requirements.
5.5.1.1 Vertical Orientation

**Figure 8. Model setup**

- Vent (50% FAR)
- ICH8M (2.4W)
- Intel® Atom ™Processor D510 (13W)
- PCB (6W)
- So DIMM (2W)
- Harddrive (2W)
- Vent (50% FAR)

**Figure 9. Isometric view of model setup**

- Vent (FAR 50%)
- ICH8M
- SODIMMS
- Harddrive
- Vent (FAR 50%)

- 6 USB
- Video/LAN
- VGA/Parallel
- PS2
The airflow plot in Figure 10 shows an increase in airflow velocity when compared to the chassis in a horizontal configuration (Figure 12). This is based on the fact that the vents and heatsink fins are in the same direction as gravity and it is much easier for the airflow to enter and exit the chassis. A vertical configuration will almost always perform better than a horizontal configuration.

Based on thermal simulation and analysis, this system thermal solution can achieve a junction-to-ambient (ΨJA) thermal resistance of 3.13° C/W in the vertical configuration and 3.43° C/W in the horizontal configuration for the Intel® Atom™ processor D510 (13W) Processor. The system integrator must test and validate the entire thermal solution to ensure that it meets thermal specifications and requirements.

CFD thermal simulation software allows a design engineer to try different component placements, orientations, and geometries so the end product will have optimized performance and meet all component specifications. This software also allows a
designer to potentially identify opportunities to reduce cost in the case of a solution that has a lot of thermal margin. Intel® Atom™ processors N450, D410 and D510 are ideally suited for fanless applications. With diligent analysis and using the recommendations in this document, a system designer can develop a fanless system.

5.5.1.2 Horizontal Orientation

Figure 11. Isometric view of horizontal orientation
5.5.2 System Level Simulations for Industrial PC

The following is an example of an Industrial PC system which has no vents that allow external ambient air to enter the chassis. This is an example of a chassis conduction cooled system. Heat from the components is dissipated into the chassis and then the heat dissipation from the chassis takes place via natural convection and radiation to the surrounding ambient air. A system designer who wishes to develop a stand-alone natural convection thermal solution would apply the same design principles.
First level TIM material is used as surface contact between the Intel® Atom™ processor DS10 and the copper heat spreader, and in order to improve the thermal resistance a second level interface is used as the gap pad between the copper heat spreader and Al pedestal touching the chassis wall. ICH8M is very low power part and hence only Al pedestal is used to transfer heat to the chassis.
Figure 15. Isometric view of Industrial PC simulation

Figure 16. Natural Convection Airflow plot for Vertical Chassis Configuration
Based on thermal simulation and analysis, this system thermal solution can achieve a junction to ambient (\(\Psi_{ja}\)) thermal resistance of 2.98 °C/ W for Intel® Atom™ processor D510 and 13.5 °C/ W for ICH8M in a fully closed vertical configuration with external ambient temperature of 55 °C hence, with current configuration Intel® Atom™ processor D510 had a margin of 6.25 °C and ICH8M had a margin of 16 °C. The system integrator must test and validate the entire thermal solution to ensure that it meets thermal specifications and requirements. CFD thermal simulation allows a designer to try different component placements, orientation, and geometries so the end product will have optimized performance and meet all the component specifications. The software also allows the designer to potentially identify opportunities to reduce cost in the case of a solution that has a lot of thermal margin.

Intel® Atom™ processor N450, D410 and D510 are ideally suited for fanless applications. With diligent analysis and using the recommendations in this document, a system designer can develop a fanless system according to their requirements.

5.6 Reference Heatsink for Forced Convection

Intel has developed reference heatsinks designed to meet the cooling needs for Intel® Atom™ processor N450, D410 and D510 in an embedded form factor application. The system designer must ensure that suitable airflow is provided when using the forced convection reference heatsinks. A third party active heatsink (fan included) is available. Appendix A, "Thermal Solution Component Suppliers" contains vendor information for each component. Heatsinks are attached to the board using two pushpins. Figure 17 illustrates an example of the thermal solution assembly. Detailed mechanical drawings of the heatsinks are provided in Appendix B, "Mechanical Drawings".

The performance curves for each reference heatsink are based on using EOLine TIM (PCM45F) Performance. A system designer may choose to use a different TIM as long as the thermal performance requirements and the component temperature specifications are satisfied. Based on the boundary conditions, the heatsink will meet the thermal performance needed to cool Intel® Atom™ processor N450, D410 and D510 with an ambient temperature of 55 °C. See Figure 18 for performance curve for various airflows. However, it is up to the system designer to validate the entire thermal solution (heatsink, attach method, TIM) in its final intended system. The data shown in Figure 18 is based on experimental test data.
**Figure 17.** Mini-ITX Forced Convection Reference Thermal Solution Assembly

**Figure 18.** Mini-ITX Forced Convection Reference Heatsink Thermal Performance versus Airflow Rate
5.7 Active Heatsink

Figure 19. Mini-ITX Active Heatsink

Table 8. Experimental Thermal Solution Performance for Active Heatsink (Intel part# E59451-001)

<table>
<thead>
<tr>
<th>SKU, TDP</th>
<th>$\Psi_{SA}$ (°C/W)</th>
<th>$\Psi_{JA}$ (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® Atom™ processor N450, 5.5 W</td>
<td>1.56</td>
<td>2.13</td>
</tr>
<tr>
<td>Intel® Atom™ processor D410, 10W</td>
<td>1.56</td>
<td>2.13</td>
</tr>
<tr>
<td>Intel® Atom™ processor D510, 13W</td>
<td>1.56</td>
<td>2.08</td>
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</tbody>
</table>

Above results are based on limited lab testing.

5.8 Keep Out Zone Requirements

The PCB keep-out zones for this heatsink assembly are shown in Appendix B, “Mechanical Drawings”.
6 Thermal Metrology

This section discusses guidelines for testing thermal solutions, including measuring processor temperatures.

6.1 Digital Thermal Sensor measurement (Tjunction-Max Methodology)

For the system integrator or designer, to validate their thermal solution design on Intel® Atom™ processor D510, it is suggested to monitor the processor's junction temperature (Tjunction). To ensure functionality and reliability, the thermal solution should be able to maintain Tjunction in the processor to be at or below the maximum temperature listed in Table 5.

It is with reasonable accuracy and aligned with the Intel Thermal Monitor function to use DTS as an indicator of Tjunction temperature and validate thermal design via DTS value. For the definition of DTS value, please refer to Section 3.11. To provide a more convenient way for system designer to monitor DTS value, Intel will support system designer with a software tool to read out the DTS value in real time when conducting thermal tests, please contact your Intel representatives for more detail and getting this tool. Even without Intel's SW tool, system designer can always access DTS value via MSR. Please check RS – Intel® Atom™ Processor N450, D410 and D510 (Formerly Pineview) BIOS Writer's Guide (BWG) Volume 1 and 2 for more details.

6.2 Local Ambient Temperature Measurement Guidelines

The local ambient temperature Ta is the temperature of the ambient air surrounding the processor. For a passive heat-sink, Ta is defined as the heat-sink approach air temperature; for an actively cooled heat-sink, it is the temperature of inlet air to the active cooling fan.

It is worthwhile to determine the local ambient temperature in the chassis around the processor to understand the effect it may have on the die temperature.

Ta is best measured by averaging temperature measurements at multiple locations in the heat-sink inlet airflow. This method helps reduce error and eliminate minor spatial variations in temperature. The following guidelines are meant to enable accurate determination of the localized air temperature around the processor during system thermal testing.

For active heat-sinks, it is important to avoid taking measurement in the dead flow zone that usually develops above the fan hub and hub spokes. Measurements should be taken at four different locations uniformly placed at the center of the annulus formed by the fan hub and the fan housing to evaluate the uniformity of the air temperature at the fan inlet. The thermocouples should be placed approximately 3 mm to 8 mm [0.1 to 0.3 in] above the fan hub vertically and halfway between the fan
hub and the fan housing horizontally as shown in Figure 20 (avoiding the hub spokes). Using an open bench to characterize an active heat-sink can be useful, and usually ensures more uniform temperatures at the fan inlet. However, additional tests that include a solid barrier above the test motherboard surface can help evaluate the potential impact of the chassis. This barrier is typically clear Plexiglas*, extending at least 100 mm [4 in] in all directions beyond the edge of the thermal solution. Typical distance from the motherboard to the barrier is 81 mm [3.2 in]. For even more realistic airflow, the motherboard should be populated with significant elements like memory cards, graphic card, and chipset heat-sink. If a barrier is used, the thermocouple can be taped directly to the barrier with a clear tape at the horizontal location as previously described, half way between the fan hub and the fan housing. If a variable speed fan is used, it may be useful to add a thermocouple taped to the barrier above the location of the temperature sensor used by the fan to check its speed setting against air temperature. When measuring $T_A$ in a chassis with a live motherboard, add-in cards, and other system components, it is likely that the $T_A$ measurements will reveal a highly non-uniform temperature distribution across the inlet fan section.

For **passive heat-sinks**, thermocouples should be placed approximately 13 mm to 25 mm [0.5 to 1.0 in] away from processor and heat-sink as shown in Figure 21. The thermocouples should be placed approximately 51 mm [2.0 in] above the baseboard. This placement guideline is meant to minimize the effect of localized hot spots from baseboard components.

**Note:** Testing an active heat-sink with a variable speed fan can be done in a thermal chamber to capture the worst-case thermal environment scenarios. Otherwise, when doing a bench top test at room temperature, the fan regulation prevents the heatsink from operating at its maximum capability. To characterize the heat-sink capability in the worst-case environment in these conditions, it is then necessary to disable the fan regulation and power the fan directly, based on guidance from the fan supplier.
Figure 20. Locations for measuring $T_{LA}$ with Active heatsink

Figure 21. Locations for Measuring $T_{LA}$, Passive Heatsink
It is recommended that full and routine calibration of temperature measurement equipment be performed before attempting to perform temperature measurement. Intel recommends checking the meter probe set against known standards. This should be done at 0°C (using ice bath or other stable temperature source) and at an elevated temperature, around 80°C (using an appropriate temperature source). Wire gauge and length also should be considered as some less expensive measurement systems are heavily impacted by impedance. There are numerous resources available throughout the industry to assist with implementation of proper controls for thermal measurements.
# Appendix A: Thermal Solution component supplier

## Table 9: Suppliers

<table>
<thead>
<tr>
<th>Part</th>
<th>Intel Part number</th>
<th>Supplier/ Part number</th>
<th>Contact Information</th>
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</thead>
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<tr>
<td>Forced Convection Heatsink</td>
<td>E85766-001</td>
<td>CHC-00005-01-GP</td>
<td><a href="mailto:yuchin_lai@cooler.master.com">yuchin_lai@cooler.master.com</a></td>
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<td></td>
<td></td>
</tr>
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<td>Natural Convection Heatsink</td>
<td>E85767-001</td>
<td>CHC-00006-01-GP</td>
<td><a href="mailto:yuchin_lai@cooler.master.com">yuchin_lai@cooler.master.com</a></td>
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<tr>
<td>Active Heatsink</td>
<td>E59451-001</td>
<td>ECB-00697-01-GP</td>
<td><a href="mailto:yuchin_lai@cooler.master.com">yuchin_lai@cooler.master.com</a></td>
</tr>
</tbody>
</table>
Appendix B: Mechanical Drawings

This appendix contains following Mechanical Drawings
B 1: Mini–ITX Forced Convection Heatsink Assembly (40 x 40 mm)
B 2: Mini–ITX Forced Convection Heatsink Drawing
B 3: PCB Keep-Out Zone for Forced Convection Heatsink
B 4: Mini-ITX Natural Convection Heatsink Assembly (64 x 64 mm)
B 5: Mini–ITX Natural Convection Heatsink Drawing
B 6: PCB Keep-Out Zone for Natural Convection Heatsink
B.1: Mini –ITX Forced Convection Heatsink Assembly (40 x 40 mm)
B.3: PCB Keep-Out Zone for Forced Convection Heatsink
Appendix B: Mechanical Drawings

B.4: Mini-ITX Natural Convection Heatsink Assembly (64 x 64 mm)
B.5: Mini-ITX Natural Convection Heatsink drawing
Appendix B: Mechanical Drawings

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Thermal Design Guide

B.6: PCB Keep-Out Zone for Natural Convection Heatsink

- Generic Board Outline
- Heatsink Area 2
- Component Height Below Heatsink
- Package Location: No Component Placement Allowed
- 2 x Ø 3±0.1 drill through

Notes:
Dimensions in Millimeters

- No Motherboard Component Placement Allowed
- Heatsink Area Max 3mm Component Height
- Heatsink Pushpin Location

Department
- 2200 Mission College Blvd.
P.O. Box 58119
Santa Clara CA 95052-5819

Size
- B

Case Code
- X

Drawing Number
- M0474-0A

Natural Convection Heatsink 002

Rev
- SHEET 3 OF 3

Scale 1:1
- DO NOT SCALE DRAWING

Intel