Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub (PCH)

Thermal Mechanical Specifications and Design Guidelines (TMSDG)

June 2013
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<table>
<thead>
<tr>
<th>Revision Number</th>
<th>Description</th>
<th>Revision Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>001</td>
<td>Initial release</td>
<td>June 2013</td>
</tr>
</tbody>
</table>

§
1 Introduction

The goals of this document are to:

- Outline the thermal and mechanical operating limits and specifications for the Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub (PCH) for use in single processor systems for the Desktop and Server/Workstation.
- Describe reference thermal solutions that meet the specifications of the Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub (PCH).

The Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub (PCH) components supported in this document are:

- Intel® Q87 Express Chipset
- Intel® Q85 Express Chipset
- Intel® B85 Express Chipset
- Intel® Z87 Express Chipset
- Intel® H87 Express Chipset
- Intel® C222 Chipset
- Intel® C224 Chipset
- Intel® C226 Chipset

Note: Unless otherwise specified, the term “Platform Controller Hub” or “PCH” will be used to refer to any version of the chipset for the Desktop or Server/Workstation. Only where required will a specific product code be used.

Properly designed thermal solutions provide adequate cooling to maintain the Platform Controller Hub case (or junction) temperatures at or below thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the case to local-ambient thermal resistance. By maintaining the PCH case (or junction) temperature at or below the specified limits, a system designer can ensure the proper functionality, performance, and reliability of the PCH. Operation outside the functional limits can cause data corruption or permanent damage to the component.

The simplest and most cost-effective method to improve the inherent system cooling characteristics is through careful chassis design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heatsink can be varied to balance size and space constraints with acoustic noise.
1.1 Related Documents

The reader of this specification should also be familiar with material and concepts presented in the following documents.

Table 1-1. Related Documents

<table>
<thead>
<tr>
<th>Title</th>
<th>Document Number / Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub (PCH) Datasheet</td>
<td>328904</td>
</tr>
<tr>
<td>Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub (PCH) Specification Update</td>
<td>328905</td>
</tr>
<tr>
<td>Various system thermal design suggestions</td>
<td><a href="http://www.formfactors.org">http://www.formfactors.org</a></td>
</tr>
</tbody>
</table>

1.2 Terminology

Table 1-2. Terminology

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BLT</td>
<td>Bond Line Thickness. Final settled thickness of the thermal interface material after installation of the heatsink.</td>
</tr>
<tr>
<td>CTE</td>
<td>Coefficient of Thermal Expansion. The relative rate a material expands during a thermal event.</td>
</tr>
<tr>
<td>FC-BGA</td>
<td>Flip Chip Ball Grid Array. A package type defined by a plastic substrate where a die is mounted using an underfill C4 (Controlled Collapse Chip Connection) attach style. The primary electrical interface is an array of solder balls attached to the substrate opposite the die. Note that the device arrives at the customer with solder balls attached.</td>
</tr>
<tr>
<td>MD</td>
<td>Metal Defined pad is one where a pad is individually etched into the PCB with a minimum width trace exiting it</td>
</tr>
<tr>
<td>PCH</td>
<td>Platform Controller Hub. The PCH is connected to the processor using the Direct Media Interface (DMI) and the Intel® Flexible Display Interface (Intel® FDI)</td>
</tr>
<tr>
<td>SMD</td>
<td>The Solder Mask Defined pad is typically a pad in a flood plane where the solder mask opening defines the pad size for soldering to the component.</td>
</tr>
<tr>
<td>TDP</td>
<td>Thermal design power. Thermal solutions should be designed to dissipate this power level. TDP is not the peak power that the PCH can dissipate.</td>
</tr>
<tr>
<td>TIM</td>
<td>Thermal Interface Material. A conductive material used between the component and heatsink to improve thermal conduction.</td>
</tr>
<tr>
<td>TMTV</td>
<td>Thermal Mechanical Test Vehicle. A mechanically equivalent package that contains a resistive heater in the die to evaluate thermal solutions. The package has daisy chain connections for use in evaluation of solder joint reliability.</td>
</tr>
</tbody>
</table>

§ §
2 Packaging Mechanical Specifications

2.1 PCH Package for Single Processor Desktop or Server / Workstation

The Platform Controller Hub uses a 22mm x 23mm square flip chip ball grid array (FC-BGA) package (see Figure 2-1 through Figure 2-3). The complete package drawing can be found in Appendix B.

**Figure 2-1. Package Dimensions (Top View)**

*Notes:*
1. All dimensions in mm
2. Drawing not to scale
Figure 2-2. Package Dimensions (Side View)

Figure 2-3. Package (Land Side View)

Note: All dimensions in mm
2.2 Solder Balls

A total of 708 solder balls corresponding to the lands are on the bottom of the PCH package for surface mounting with the motherboard. The package solder ball has the following characteristics:

- Lead-free SAC (SnAgCu) 405 solder alloy with a silver (Ag) content between 3% and 4% and a melting temperature of approximately 217 °C. The alloy is compatible with immersion silver (ImAg) and Organic Solderability Protectant (OSP) motherboard surface finishes and a SAC alloy solder paste.
- Solder ball diameter 16 mil [0.4138 mm], before attaching to the package.

2.3 Package Mechanical Requirements

The package has a bare die that is capable of sustaining a maximum static normal load of 15 lbf (67N). These mechanical load limits must not be exceeded during heatsink installation, mechanical stress testing, standard shipping conditions, and/or any other use condition.

Note: The heatsink attach solutions must not induce continuous stress to the package with the exception of a uniform load to maintain the heatsink-to-package thermal interface.

Note: These specifications apply to uniform compressive loading in a direction perpendicular to the die top surface.

Note: These specifications are based on limited testing for design characterization. Loading limits are for the package only.
3 Thermal Specifications

To ensure proper operation and reliability of the PCH, the case (or junction) temperature must be at or below the maximum value specified in Table 3-1. System and/or component level thermal solutions are required to maintain these temperature specifications. Chapter 5 provides the thermal metrology guidelines for case (or junction) temperature measurements.

3.1 Thermal Design Power (TDP)

Real applications are unlikely to cause the PCH component to consume maximum power dissipation for sustained time periods. Therefore, to arrive at a more realistic power level for thermal design purposes, Intel characterizes power consumption to reach a Thermal Design Power (TDP). TDP is the target power level to which the thermal solutions should be designed. TDP is not the maximum power that the PCH can dissipate (see Table 3-1).

TDP condition is a set of applications when run simultaneously, would stress all its features and dissipate power equivalent to TDP in the worst leakage scenario (see Table 3-2). The configuration of PCH TDP is in Table 3-3.

3.2 Thermal Specifications

The data in Table 3-1 is based on pre-silicon estimates for the PCH. The TDP, Idle, and S3 values are based on system configuration. Intel recommends designing the PCH thermal solution to the TDP for maximum flexibility and reuse. The PCH package has poor heat transfer capability into the board and minimal thermal capability without thermal solutions. Intel requires that system designers plan for an attached heatsink when using the PCH. The reference thermal solution is described in Chapter 6.

Table 3-1. PCH Thermal Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCASE-MAX</td>
<td>104 °C</td>
<td></td>
</tr>
<tr>
<td>TCASE-MIN</td>
<td>0 °C</td>
<td></td>
</tr>
<tr>
<td>Tj,max</td>
<td>108 °C</td>
<td></td>
</tr>
<tr>
<td>TDP</td>
<td>4.1 W</td>
<td>The value is based on system configuration and applications running simultaneously, see Table and Table 3-4. The value measurement is based on a core voltage of 1.05 V and Tj of Tj,max.</td>
</tr>
<tr>
<td>Idle</td>
<td>0.700 W</td>
<td>The value is based on system configuration, see Table 3-4. The value measurement is based on a core voltage of 1.05 V and Tj of 50 °C.</td>
</tr>
<tr>
<td>S3</td>
<td>0.091 W</td>
<td></td>
</tr>
</tbody>
</table>
### Table 3-2. PCH Thermal Design Power (TDP) Workload Running Simultaneously

<table>
<thead>
<tr>
<th>TDP Workload Description (Applications running concurrently)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1080P HD video callover PCIE</td>
</tr>
<tr>
<td>Read from USB2 Port 3, write to SATA Port 2/3</td>
</tr>
<tr>
<td>Read from SATA Port 4/5, write to USB2 Port 10</td>
</tr>
<tr>
<td>Read from SATA Port 4/5, write to USB2 Port 11</td>
</tr>
<tr>
<td>Read from SATA Port 4/5, write to USB2 Port 12</td>
</tr>
<tr>
<td>Read from SATA Port 4/5, write to USB3 Port 2</td>
</tr>
<tr>
<td>Read from USB3 Port 2, write to SATA Port 2/3</td>
</tr>
<tr>
<td>HDMI video input from TV</td>
</tr>
<tr>
<td>Local network file transfer</td>
</tr>
</tbody>
</table>

### Table 3-3. PCH Thermal Design Power (TDP) Configuration

<table>
<thead>
<tr>
<th>PCH Interfaces</th>
<th>Peripherals and Plug-ins</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDI Port 1</td>
<td>VGA External Flat Panel, 1920x1080 60 Hz</td>
</tr>
<tr>
<td>USB3 Port 0</td>
<td>USB3 SSD</td>
</tr>
<tr>
<td>USB3 Port 1</td>
<td>Flash thumb drive</td>
</tr>
<tr>
<td>USB2 Port 0</td>
<td>Keyboard</td>
</tr>
<tr>
<td>USB2 Port 1</td>
<td>Mouse</td>
</tr>
<tr>
<td>USB2 Port 2</td>
<td>Digital Camera</td>
</tr>
<tr>
<td>USB2 Port 3</td>
<td>Webcam</td>
</tr>
<tr>
<td>USB2 Port 4</td>
<td>Media card reader</td>
</tr>
<tr>
<td>USB2 Port 5</td>
<td>No connection</td>
</tr>
<tr>
<td>USB2 Port 6</td>
<td>Game controller</td>
</tr>
<tr>
<td>USB2 Port 7</td>
<td>No connection</td>
</tr>
<tr>
<td>USB2 Port 8</td>
<td>Flash thumb drive</td>
</tr>
<tr>
<td>USB2 Port 9</td>
<td>Flash thumb drive</td>
</tr>
<tr>
<td>USB2 Port 10</td>
<td>USB external hard disk</td>
</tr>
<tr>
<td>USB2 Port 11</td>
<td>MP3 player</td>
</tr>
<tr>
<td>USB2 Port 12</td>
<td>Flash thumbdrive</td>
</tr>
<tr>
<td>USB2 Port 13</td>
<td>No connection</td>
</tr>
<tr>
<td>SATA Port 0</td>
<td>SATA Gen1 Optical disk drive</td>
</tr>
<tr>
<td>SATA Port 1</td>
<td>Raid 0 Hard drive array (SATA Gen3)</td>
</tr>
<tr>
<td>SATA Port 2</td>
<td>Raid 0 Hard drive array (SATA Gen3)</td>
</tr>
<tr>
<td>SATA Port 3</td>
<td>Raid 0 Hard drive array (SATA Gen3)</td>
</tr>
<tr>
<td>SATA Port 4</td>
<td>Raid 0 Hard drive array (SATA Gen3)</td>
</tr>
<tr>
<td>SATA Port 5</td>
<td>SATA Gen1 Optical disk drive</td>
</tr>
<tr>
<td>PCIEx1 Port 3</td>
<td>WLAN card</td>
</tr>
<tr>
<td>PCIEx1 Port 4</td>
<td>Dual HDTV tuner</td>
</tr>
<tr>
<td>PCIEx1 Port 5</td>
<td>Intel GbE PHY</td>
</tr>
<tr>
<td>Intel® High Definition Audio (Intel® HD Audio)</td>
<td>Enabled (microphone and headphone active)</td>
</tr>
</tbody>
</table>
Thermal Specifications

Table 3-4. PCH Idle Power Configuration

<table>
<thead>
<tr>
<th>PCH Interfaces</th>
<th>Link Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® High Definition Audio (Intel® HD Audio)</td>
<td>Idle</td>
</tr>
<tr>
<td>USB2.0 Port0</td>
<td>Keyboard</td>
</tr>
<tr>
<td>USB2.0 Port1</td>
<td>Mouse</td>
</tr>
<tr>
<td>SATA Port 0</td>
<td>Intel S20 Series 240GB SSD (Gen 3, OS boot)</td>
</tr>
<tr>
<td>SATA Port 1</td>
<td>BD-RW ODD</td>
</tr>
</tbody>
</table>

3.3 Storage Specifications

Table 3-5 includes a list of the specifications for device storage in terms of maximum and minimum temperatures and relative humidity. These conditions should not be exceeded in storage or transportation.

Table 3-5. Storage Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Max</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{ABSOLUTE}$ STORAGE</td>
<td>The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to for any length of time.</td>
<td>-25 °C</td>
<td>125 °C</td>
<td>1, 2, 3</td>
</tr>
<tr>
<td>$T_{SUSTAINED}$ STORAGE</td>
<td>The ambient storage temperature limit (in shipping media) for a sustained period of time.</td>
<td>-5 °C</td>
<td>40 °C</td>
<td>4, 5</td>
</tr>
<tr>
<td>$R_{H SUSTAINED}$ STORAGE</td>
<td>The maximum device storage relative humidity for a sustained period of time.</td>
<td>60% @ 24 °C</td>
<td></td>
<td>5, 6</td>
</tr>
<tr>
<td>$TIME_{SUSTAINED}$ STORAGE</td>
<td>A prolonged or extended period of time; typically associated with customer shelf life.</td>
<td>0 Months</td>
<td>6 Months</td>
<td>6</td>
</tr>
</tbody>
</table>

Note:
1. Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals.
2. Specified temperatures are based on data collected. Exceptions for surface mount reflow are specified in by applicable JEDEC standard. Non-adherence may affect component reliability.
3. $T_{ABSOLUTE}$ storage applies to the unassembled component only and does not apply to the shipping media, moisture barrier bags or desiccant.
4. Intel branded board products are certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40 °C to 70 °C and Humidity: 50% to 90%, non-condensing with a maximum wet bulb of 28 °C). Post board attach storage temperature limits are not specified for non-Intel branded boards.
5. The JEDEC, J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
6. Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by $T_{SUSTAINED}$ and customer shelf life in applicable Intel box and bags.

§§
Intel provides thermal simulation models of the PCH and associated user guides to aid system designers in simulating, analyzing, and optimizing their thermal solutions in an integrated, system-level environment. The models are for use with the commercially available Computational Fluid Dynamics (CFD)-based thermal analysis tool FLOHERM* (version 9.2 or higher) by Flomerics, Inc.* and Icepak* by Fluent*. Contact your Intel field sales representative to order the thermal models and user guides.
5 Thermal Metrology

The system designer must make temperature measurements to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques to measure the PCH case and junction temperatures. The flowchart in Figure 5-1 offers useful guidelines for thermal performance and evaluation.

**Figure 5-1. Thermal Solution Decision Flow Chart**

![Flowchart showing thermal solution decision process]

5.1 $T_{\text{case}}$ Temperature Measurements

To ensure functionality and reliability, the $T_{\text{case}}$ of the PCH must be maintained between the maximum/minimum operating range of the temperature specification as noted in Table 3-1. The surface temperature at the geometric center of the die corresponds to $T_{\text{case}}$. Measuring $T_{\text{case}}$ requires special care to ensure an accurate temperature measurement.

Temperature differences between the surface and the surrounding local ambient air can introduce errors in the measurements. The measurement errors could be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, and/or contact between the thermocouple cement and the heatsink base (if a heatsink is used). For maximum measurement accuracy, only the following thermocouple attach approach is recommended.

5.1.1 Heatsink Thermocouple Attach Methodology

1. Mill a 3.3 mm (0.13 in.) diameter and 1.5 mm (0.06 in.) deep hole centered on the bottom of the heatsink base.
2. Mill a 1.3 mm (0.05 in.) wide and 0.5 mm (0.02 in.) deep slot from the centered hole to one edge of the heatsink. The slot should be parallel to the heatsink fins (see Figure 5-3).
3. Attach thermal interface material (TIM) to the bottom of the heatsink base.
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heatsink base.
5. Attach a 36 gauge or smaller calibrated K-type thermocouple bead to the center of the top surface of the die using a high thermal conductivity cement. During this step, ensure no contact is present between the thermocouple cement and the heatsink base because any contact will affect the thermocouple reading. It is critical that the thermocouple bead makes contact with the die (see Figure 5-3).

6. Attach heatsink assembly to the package and route thermocouple wires out through the milled slot.

Figure 5-2. Heatsink Modifications

![Heatsink Modifications](image)

**Note:** Not to Scale

Figure 5-3. Top View of Package

![Top View of Package](image)

5.2 Ambient Temperature and Airflow Measurement

Figure 5-4 describes the recommended location for air temperature measurements measured relative to the component. For a more accurate measurement of the average approach air temperature, Intel recommends averaging temperatures recorded from two thermocouples spaced about 25 mm (1.0 in) apart. Locations for both a single thermocouple and a pair of thermocouples are presented.

Airflow velocity should be measured using industry standard air velocity sensors. Typical airflow sensor technology may include hot wire anemometers.
Figure 5-4 provides guidance for airflow velocity measurement locations. These locations are for a typical JEDEC test setup and may not be compatible with all chassis layouts due to the proximity of the, PCI* and PCI Express* add-in cards to the component. The user may have to adjust the locations for a specific chassis. Be aware that sensors may need to be aligned perpendicular to the airflow velocity vector or an inaccurate measurement may result. Measurements should be taken with the chassis fully sealed in its operational configuration to achieve a representative airflow profile within the chassis.

Figure 5-4. Airflow and Temperature Measurement Locations
5.3 Thermal Mechanical Test Vehicle (TMTV)

A Thermal Mechanical Test Vehicle (TMTV) is available for early thermal testing. The TMTV contains a heater die and can be powered up to a desired power level to simulate the heating of a PCH package. The TMTV needs to be surface mounted to a custom board designed to provide connectivity to the die heater. Although the TMTV is designed to closely match the PCH package, it is recommended that final validation be performed with actual production silicon.
6 Advanced Technology eXtended (ATX) Reference Thermal Solution

Note: The reference thermal mechanical solution information shown in this document represents the current state of the design. The data is subject to modification and represents design targets, not commitments by Intel.

The design strategy for the PCH thermal solution is to reuse the z-clip heatsink designed from Intel® 5 Series Chipset and used on subsequent PCH designs through the Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub (PCH).

This section describes the overall requirements for the EmbeddedATX (EmbATX) heatsink reference thermal solution including critical-to-function dimensions, operating environment, and validation criteria. Other chipset components may or may not need attached thermal solutions depending on your specific system local-ambient operating conditions.

6.1 Reference Solution

The reference solution is an extruded aluminum heatsink with pre-applied phase change thermal interface material (TIM). The TIM is a Chomerics* T710. The reference solution is provided as an assembly with the clip, TIM and extrusion. See Appendix B for the complete set of mechanical drawings including the motherboard keep out zone.

The reference design z-clip centers the load on the die and by design will keep the heatsink flush and parallel with the top surface of the die. The TIM size in the reference design is larger than the die area. The resistivity of the TIM is $5 \times 10^{16}$ Ohm-cm. Any TIM material that comes in contact with die side capacitors (DSC) will not cause a short.

During the heatsink assembly process, the heatsink may come in contact with DSC. The maximum spring force allowed for the reference design z-clip has not been shown to cause damage to DSC during assembly.

However, the TDP for the Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub (PCH) is lower than previous generations, so there exists opportunities for cost-optimized heatsink design. The motherboard keep-out zone maximum height is now 1.0 mm, as shown in Figure B-2. A reference solution that fits only to the shadow of the PCH package (22x23 mm) would not require a motherboard keep-out zone, outside of the mounting hardware. There is also opportunity for a heatsink-less design, but the required airflow boundary condition may exceed what currently exists in EmbATX-based systems (specifically μSFF and AIO systems).
Figure 6-1. Velocity Boundary Condition Assessment

Figure 6-2. Reference Thermal Solution
6.2 Environmental Reliability Requirements

The reference solution heatsink will be evaluated to the reliability requirements in Table 6-1. The mechanical loading of the component may vary depending on the heatsink, and attach method used. The customer should define a validation test suite based on the anticipated use conditions and resulting reliability requirements. Thermal cycling, bake and humidity tests were performed on original design and are not being repeated. The designer should select appropriate thermal/humidity tests for the expected use conditions.

Table 6-1. Reference Thermal Solution Environmental Reliability Requirements

<table>
<thead>
<tr>
<th>Test</th>
<th>Requirement</th>
<th>Pass / Fail Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mechanical Shock</td>
<td>3 drops for + and - directions in each of 3 perpendicular axes (that is, total 18 drops). Profile: 50 G trapezoidal waveform, 170 inches/sec. minimum velocity change. Setup: Mount sample board on test fixture</td>
<td>Visual/Electrical Check</td>
</tr>
<tr>
<td>Random Vibration</td>
<td>Duration: 10 min/axis, 3 axes Frequency Range: 5 Hz to 500 Hz Power Spectral Density (PSD) Profile: 3.13 g RMS</td>
<td>Visual/Electrical Check</td>
</tr>
</tbody>
</table>
Thermal Solution Component Vendors

Note: These vendors and devices are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change without notice.

Table A-1. Reference Heatsink Enabled Components

<table>
<thead>
<tr>
<th>Item</th>
<th>Intel PN</th>
<th>AVC</th>
<th>CCI</th>
<th>Foxconn</th>
<th>Wieson</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heatsink Assembly</td>
<td>C46655-001</td>
<td>S702C00001</td>
<td>00C855802B</td>
<td>22802-009</td>
<td></td>
</tr>
<tr>
<td>Anchor</td>
<td>A13494-008</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table A-2. Supplier Contact Information

<table>
<thead>
<tr>
<th>Supplier</th>
<th>Contact</th>
<th>Phone</th>
<th>Email</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVC* (Asia Vital Corporation)</td>
<td>Kai Chang</td>
<td>+86 755 3366 8888 x63588</td>
<td><a href="mailto:kai.chang@avc.com.tw">kai.chang@avc.com.tw</a></td>
</tr>
<tr>
<td>CCI* (Chaun Choung Technology)</td>
<td>Monica Chih</td>
<td>+886-2-2995-2666</td>
<td><a href="mailto:monica.chih@ccic.com.tw">monica.chih@ccic.com.tw</a></td>
</tr>
<tr>
<td>Foxconn*</td>
<td>Jack Chen</td>
<td>(408) 919-6121</td>
<td><a href="mailto:jack.chen@foxconn.com">jack.chen@foxconn.com</a></td>
</tr>
<tr>
<td></td>
<td>Wanchi Chen</td>
<td>(408) 919-6135</td>
<td><a href="mailto:wanchi.chen@foxconn.com">wanchi.chen@foxconn.com</a></td>
</tr>
<tr>
<td>Wieson*</td>
<td>Chary Lee</td>
<td>+886-2-2647-1896 ext. 6684</td>
<td><a href="mailto:chary@wieson.com">chary@wieson.com</a></td>
</tr>
<tr>
<td></td>
<td>Henry Liu</td>
<td>+886-2-2647-1896 ext.6330</td>
<td><a href="mailto:henry@wieson.com">henry@wieson.com</a></td>
</tr>
</tbody>
</table>
The mechanical drawings included in this appendix:

Figure B-1, “Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub (PCH) Package Drawing” on page 28.

Figure B-2, “Motherboard Keep-Out for ATX Reference Heatsink” on page 29.

Figure B-3, “ATX Reference Heatsink Assembly” on page 30.

Figure B-4, “ATX Reference Heatsink Extrusion” on page 31.

Figure B-5, “ATX Reference Heatsink Clip” on page 32.
Figure B-1. Intel® 8 Series / C220 Series Chipset Family Platform Controller Hub (PCH) Package Drawing
**Figure B-2.** Motherboard Keep-Out for ATX Reference Heatsink
Figure B-3. ATX Reference Heatsink Assembly
Figure B-4. ATX Reference Heatsink Extrusion
Figure B-5. ATX Reference Heatsink Clip