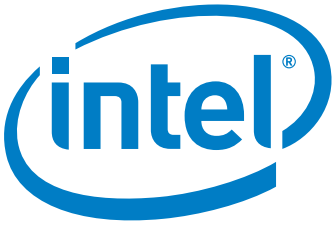


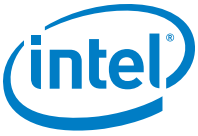
Intel® Xeon Phi™ Processor x200 Product Family Datasheet, Volume One: Electrical

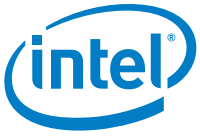
Volume 1 of 2

Rev. 002

January 2017

Order No.: 334710-002





Contents

Figures

Tables

Revision History

Document Number	Revision Number	Description	Revision Date
334710	001	Initial release	August 2016
334710	002	• Updated Table 3-12 to match the current Customer Reference Board (CRB). • Updated Table 4-4 with the latest Vtyp changes, and changed to relative operational voltage limits on two rails.	January 2017

1.0 Overview

1.1 Introduction

The datasheet is a two-volume set that provides electrical and register specification details for the second generation Intel® Xeon Phi™ processor family.

- *Intel® Xeon Phi™ Processor x200 Product Family Datasheet, Volume One: Electrical* provides DC electrical specifications, signal integrity, differential signaling specifications, land and signal definitions, and a limited overview of processor interfaces.
- *Intel® Xeon Phi™ Processor x200 Product Family Datasheet, Volume Two: Registers* provides Configuration Space Registers (CSRs) information.

Thermal and mechanical specifications are no longer maintained in this document and are now archived exclusively in the *Intel® Xeon Phi™ Processor x200 Product Family Thermal/Mechanical Specification and Design Guide (TMSDG)*.

The target audience for this document is primarily system architects and engineers who are planning to develop the Intel® Xeon Phi™ Processor x200 Product Family based High Performance Computers (HPCs). Additionally, this document may be used by system test engineers, board designers, and BIOS developers.

The structure and scope of the processor datasheet volumes are provided in Table 1-1.

Throughout this document, unless specified otherwise, the term "processor" represents any member of the Intel® Xeon Phi™ Processor x200 Product Family; where distinction is necessary, the term "processor with fabric" will represent the Intel® Xeon Phi™ processor with integrated Intel® Omni-Path Fabric (Intel® OP Fabric).

The Intel® Xeon Phi™ Processor x200 Product Family is the next generation of 64-bit, multi-core enterprise processor built on 14-nanometer process technology. The processor is designed for a two-chip platform comprised of a processor and the Intel® C610 Series Chipset Platform Controller Hub (PCH). The Intel® Xeon Phi™ Processor x200 Product Family is designed for HPC applications.

This processor features up to 36 lanes of PCI Express* 3.0 links capable of 8.0 GT/s, and four lanes of DMI2 with a peak transfer rate of 5.0 GT/s. Two integrated memory controllers accessing up to six DDR4 channels.

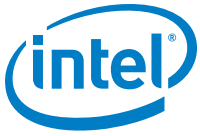


Table 1-1. Processor Datasheet Volume Structure

Datasheet Volume Topics
Volume One: Electrical Specifications
Overview
Signal Descriptions
Power Supply Specifications
Signal Specifications
Volume Two: Register Information
Configuration Process and Registers
Processor Integrated I/O (IIO) Configuration Registers
Processor Uncore Configuration Registers

1.2 Related Documents

Refer to the documents in Table 1-2 for additional information.

Table 1-2. Public Specifications

Document	Document Number/Location
Advanced Configuration and Power Interface Specification 3.0	http://www.acpi.info/
PCI Local Bus Specification 3.0	http://www.pcisig.com/specifications/
PCI Express® Base Specification - Revision 3.0 *PCI Express® Base Specification - Revision 2.1 and 1.1*	
System Management Bus (SMBus) Specification, Version 2.0	http://smbus.org/
DDR4 SDRAM Specification JESD79-4A *DDR4 SDRAM Register Specifications* *DDR4 RDIMM Design Specification and Raw Card Annexes* *DDR4 LRDIMM Design Specification and Raw Card Annexes*	http://www.jedec.org/
Intel® 64 and IA-32 Architectures Software Developer's Manuals • Volume 1: Basic Architecture • Volume 2A: Instruction Set Reference, A-M • Volume 2B: Instruction Set Reference, N-Z • Volume 3A: System Programming Guide • Volume 3B: System Programming Guide *Intel® 64 and IA-32 Architectures Optimization Reference Manual*	http://www.intel.com/products/processor/manuals/index.htm
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	http://download.intel.com/technology/computing/vptech/Intel(r)_VT_for_Direct_IO.pdf

1.3 Terminology

Table 1-3 provides a list of common terms used in this document, along with a brief description.

Table 1-3. Descriptions of Terms (Sheet 1 of 2)

Term	Description
BMC	Baseboard Management Controller
Cbo	Is a term used for the functional unit (also called the CHA) inside the die that serves as the internal cache agent logic connecting to the mesh and controlling memory and caching communication, including ordering read/write requests to coherent memory.
CHA	Cbo and home agent, see Cbo description.
DDR4	Fourth generation Double Data Rate SDRAM memory technology
DMA	Direct Memory Access
DMI2	Direct Media Interface Gen 2
DRAM	Dynamic Random Access Memory
DTS	Digital Thermal Sensor
ECC	Error Correction Code
EDC	Embedded DRAM controller integrated in the processor die which controls accesses to MCDRAM memory
Functional Operation	Refers to the normal operating conditions in which all processor specifications, including DC, AC, system bus, signal quality, mechanical, and thermal, are satisfied.
IIO	The Integrated I/O Controller. An I/O controller is integrated in the processor die.
IMC	The Integrated Memory Controller. A DDR4 memory controller that is integrated in the processor die.
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture.
Intel® ME	Intel® Management Engine (Intel® ME), integrated into the PCH
Intel® Turbo Boost Technology	Intel® Turbo Boost Technology is a way to automatically run the processor core faster than the marked frequency if the part is operating under power, temperature, and current specification limits of the Thermal Design Power (TDP). This results in increased performance of both single- and multi-threaded applications.
Intel® Virtualization Technology (Intel® VT)	Processor virtualization, which when used in conjunction with virtual machine monitor software enables multiple, robust independent software environments inside a single platform.
Intel® VT-d	Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d). Intel VT-d is a hardware assist for enabling I/O device virtualization. It is under system software (Virtual Machine Manager or OS) control. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.
Jitter	Any timing variation of a transition edge or edges from the defined Unit Interval (UI)
LLC	Last Level Cache refers to the last level of CPU-side cache. MCDRAM can serve as a memory-side direct-mapped cache when the processor is configured in a cache or hybrid memory hierarchy.
LRDIMM	Load Reduced Dual In-line Memory Module
MCDRAM	Multi-Channel DRAM is a stacked die technology used for on-package memory.
Mesh	An bus interconnect integrated on the processor die that connects the tiles to memory and I/O.
MLC	Mid-Level Cache is the 1 MB L2 cache associated with each tile.

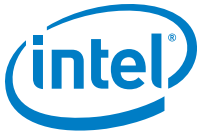


Table 1-3. Descriptions of Terms (Sheet 2 of 2)

Term	Description
NCTF	Noncritical to Function processor package lands: NCTF locations are typically redundant ground or noncritical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.
PCH	Platform Controller Hub. The next generation chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security and storage features.
PCI Express*	PCI Express* Generation 3.0/2.0/1.0
PCI Express* 3.0	The third generation PCI Express* specification that operates 60% faster than PCI Express* 2.0 (8 Gb/s vs. 5 Gb/s); however, PCI Express* 3.0 is completely backward compatible with PCI Express* 2.0 and 1.0.
pcode	Microcode that is run on the dedicated micro-controller within the PCU.
PCU	Power Control Unit
PECI	Platform Environment Control Interface
Rank	A unit of DRAM corresponding to four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DDR4 DIMM.
RDIMM	Registered Dual In-line Memory Module
SCI	System Control Interrupt. Used in ACPI protocol.
SDRAM	Synchronous DRAM
SKU	A processor Stock Keeping Unit (SKU) to be installed in either server or workstation platforms. For the Intel® Xeon Phi™ Processor x200 Product Family, different SKUs will be distinguished by different marketing names and offer, e.g., different numbers of cores, clock frequencies, etc.
SMBus	System Management Bus. A two-wire interface through which simple system and power management related devices can communicate with the rest of the system. It is based on the principals of the operation of the I^2C* two-wire serial bus from NXP Semiconductors*.
SSE	Intel® Streaming SIMD Extensions (Intel® SSE)
Storage conditions	A nonoperational state. The processor may be loose or installed in a platform or tray. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased, or receive any clocks. Upon exposure to “free air” (unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with Moisture Sensitivity Labeling (MSL) as indicated on the packaging material.
TAC	Thermal Averaging Constant
TDP	Thermal Design Power
Tile	A processing block consisting of vector processing units (VPUs), Intel® Atom™ based cores, and an L2 cache.
TSOD	Thermal Sensor on DIMM
UI	Unit Interval: Signaling convention that is binary and unidirectional. In this binary signaling, one bit is sent for every edge of the forwarded clock, whether it be a rising edge or a falling edge. If a number of edges are collected at instances t_1, t_2, t_n,…., t_k, then the UI at instance "n" is defined as: $UI_n = t_n - t_{n-1}$.
V_{CC}	Processor core power supply
VPU	Vector Processing Unit, a computational engine inside the tile
VR	Voltage Regulator
V_{SS}	Processor ground
xN, where N = 1, 4, 8, etc	Refers to a link or port with “N” physical lanes, where N = 1, 4, 8, 16, etc.

1.4 Processor Feature Overview

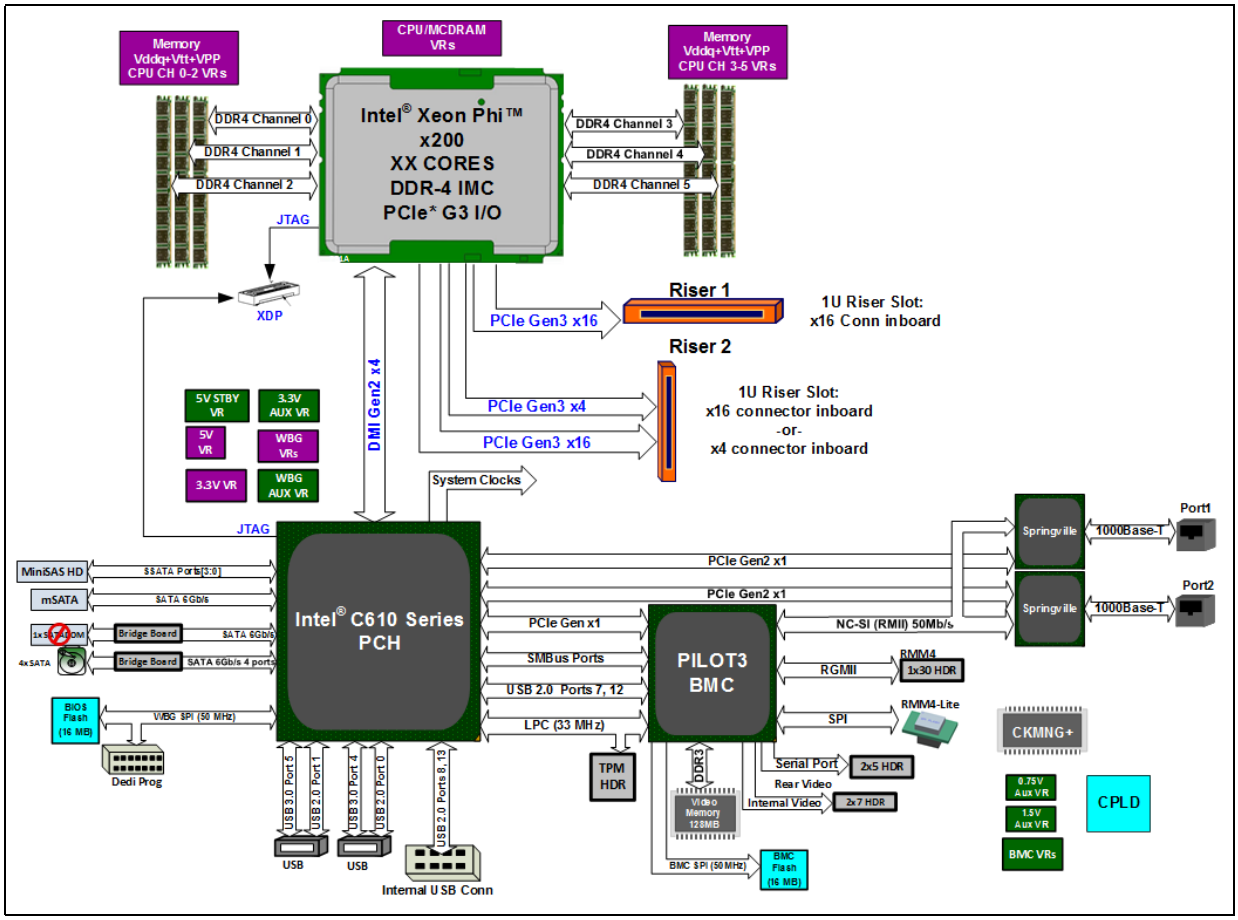
This section provides a limited overview of the processor features.

1.4.1 Tile and Core Feature Overview

- Up to 36 tiles with a mesh interconnect
- Each tile contains two Intel® Atom™ cores and four Vector Processing Units (VPUs); up to 72 physical cores are enabled in total
- Each core supports four threads (Intel® Hyper-Threading Technology), up to 288 threads per node
- 32-KB instruction and 32-KB data first-level cache (L1) for each core
- 1 MB shared instruction/data mid-level (L2) cache for each tile

A rudimentary block diagram of the Intel® Xeon Phi™ Processor x200 Product Family platform is illustrated in Figure 1-1 with a processor interconnected to a Platform Controller Hub (PCH).

Figure 1-1. Intel® Xeon Phi™ Processor x200 Product Family Platform



1.5 Interface Feature Overview

This section provides a limited overview of the processor interfaces.

1.5.1 System Memory

Eight MCDRAM on-package memory modules with 16 GB capacity total.

Six DDR4 channels, each channel limited to one DIMM per channel (max. DIMM capacity is 64 GB), 384 GB capacity total.

- Voltages: 1.2V standard I/O and 2.5V charge pump
- Bus Width: 64-bit wide data plus 8-bits of ECC support for each channel
- Speed: Data transfer rates of 1867, 2133 and 2400 MT/s
- Device Density and I/O Width: 4 and 8 Gb, x4 and x8, DRAM devices
- DIMM Types: Registered DIMMs (RDIMMs) and load reduced DIMMs (LRDIMMs)
- Ranks: Up to four physical ranks supported per memory channel, and up to eight logical ranks (3DS devices) supported per channel
- Memory thermal monitoring support for DIMM temperature via two memory signals, DDR{012/345}_MEMHOT_N

1.5.2 PCI Express*

- Up to 36 lanes of PCI Express
- Compliant to the PCI Express Base Specification, Revision 3.0 (PCIe* 3.0)
- Reduced link width negotiation supported:
  - x16 port (port 2 and 3) may negotiate down to x8, x4, x2, or x1
  - x4 port (port 1) may negotiate down to x2, or x1
  - Lane reversal and polarity inversion are supported

1.5.3 Direct Media Interface Gen 2 (DMI2)

- Primary processor interface to the Platform Controller Hub (PCH)
- Link width is exclusively x4
- Operation at PCI Express 1.0 or 2.0 speeds

1.5.4 Platform Environment Control Interface (PECI)

PECI is a single-wire multi-drop interface providing a communication channel between a PECI client (the processor) and a PECI master (the PCH or the BMC). The PECI interface is based on revision 3.0 of the specification.

- Supports operation at up to 2 Mbps data transfers.

1.6 Socket and Package Summary

Mechanical details of the socket and package are provided in the *Intel® Xeon Phi™ Processor x200 Product Family Thermal/Specification and Design Guide (TMSDG)*. The processor is a multi-chip package consisting of the processor silicon die and 8 MCDRAM chips, all housed in an FC-LGA package that interfaces with the motherboard via an LGA3647-1 socket.

1.7 Statement of Volatility (SOV)

The processor does not retain any end-user data when powered down and/or the processor is physically removed from the socket.

1.8 State of Data

The data contained within this document is final. It is the most accurate information available by the publication date of this document. Electrical DC specifications are based on estimated I/O buffer behavior.

§

2.0 Processor Land Listings

Table 2-1. Lands by Name (Sheet 1 of 94)

Land Name	Land No.
BCLK0_DN	CT27
BCLK0_DP	CV27
BIST_ENABLE	CV31
BPM_N[0]	CE24
BPM_N[1]	CG24
BPM_N[2]	CF23
BPM_N[3]	CE22
BPM_N[4]	CG22
BPM_N[5]	CF21
BPM_N[6]	CG20
BPM_N[7]	CE20
CATERR_N	CP27
CD_HFI_REFCLK_DN	DA86
CD_HFI_REFCLK_DP	DC86
CD_HFI0_I2CCLK	G78
CD_HFI0_I2CDAT	H77
CD_HFI0_INT_N	C72
CD_HFI0_LED_N	B71
CD_HFI0_MODPRST_N	D71
CD_HFI0_RESET_N	G72
CD_HFI1_I2CCLK	Y55
CD_HFI1_I2CDAT	V55
CD_HFI1_INT_N	U54
CD_HFI1_LED_N	W54
CD_HFI1_MODPRST_N	T53
CD_HFI1_RESET_N	AA54
CD_PE_REFCLK_DN	CL86
CD_PE_REFCLK_DP	CJ86
CD_PERST_N	C76
CD_PRESENT_N	B73
CD_TCLK	G76

Table 2-1. Lands by Name (Sheet 2 of 94)

Land Name	Land No.
CD_TDI	D77
CD_TDO	D79
CD_TMS	B77
CD_TRST_N	C78
CPUPWRGD	CR24
DDR0_ACT_N	U50
DDR0_ALERT_N	Y49
DDR0_AP_MA[10]	T35
DDR0_BA0	Y35
DDR0_BA1	W36
DDR0_BC_N_MA[12]	U48
DDR0_BG0	T49
DDR0_BG1	W50
DDR0_C0_CS_N[2]	Y29
DDR0_C1_CS_N[3]	T29
DDR0_C2	W30
DDR0_CAS_N_MA[15]	Y33
DDR0_CKE[0]	Y51
DDR0_CKE[1]	T51
DDR0_CLK_DN[0]	T39
DDR0_CLK_DN[2]	W38
DDR0_CLK_DP[0]	U38
DDR0_CLK_DP[2]	Y37
DDR0_CS_N[0]	W34
DDR0_CS_N[1]	T31
DDR0_DQ[0]	AE82
DDR0_DQ[1]	AD81
DDR0_DQ[10]	AH73
DDR0_DQ[11]	AG72
DDR0_DQ[12]	AG76
DDR0_DQ[13]	AH75
DDR0_DQ[14]	AE72

Table 2-1. Lands by Name (Sheet 3 of 94)

Land Name	Land No.
DDR0_DQ[15]	AD73
DDR0_DQ[16]	AE70
DDR0_DQ[17]	AD69
DDR0_DQ[18]	AH67
DDR0_DQ[19]	AG66
DDR0_DQ[2]	AH79
DDR0_DQ[20]	AH69
DDR0_DQ[21]	AG70
DDR0_DQ[22]	AE66
DDR0_DQ[23]	AD67
DDR0_DQ[24]	AE64
DDR0_DQ[25]	AD63
DDR0_DQ[26]	AH61
DDR0_DQ[27]	AG60
DDR0_DQ[28]	AG64
DDR0_DQ[29]	AH63
DDR0_DQ[3]	AG78
DDR0_DQ[30]	AE60
DDR0_DQ[31]	AD61
DDR0_DQ[32]	AC26
DDR0_DQ[33]	AB25
DDR0_DQ[34]	AF23
DDR0_DQ[35]	AE22
DDR0_DQ[36]	AE26
DDR0_DQ[37]	AF25
DDR0_DQ[38]	AC22
DDR0_DQ[39]	AB23
DDR0_DQ[4]	AG82
DDR0_DQ[40]	AC20
DDR0_DQ[41]	AB19
DDR0_DQ[42]	AF17
DDR0_DQ[43]	AE16
DDR0_DQ[44]	AE20
DDR0_DQ[45]	AF19
DDR0_DQ[46]	AC16
DDR0_DQ[47]	AB17
DDR0_DQ[48]	AC14
DDR0_DQ[49]	AB13
DDR0_DQ[5]	AH81

Table 2-1. Lands by Name (Sheet 4 of 94)

Land Name	Land No.
DDR0_DQ[50]	AF11
DDR0_DQ[51]	AE10
DDR0_DQ[52]	AF13
DDR0_DQ[53]	AE14
DDR0_DQ[54]	AC10
DDR0_DQ[55]	AB11
DDR0_DQ[56]	AC8
DDR0_DQ[57]	AB7
DDR0_DQ[58]	AF5
DDR0_DQ[59]	AE4
DDR0_DQ[6]	AE78
DDR0_DQ[60]	AE8
DDR0_DQ[61]	AF7
DDR0_DQ[62]	AC4
DDR0_DQ[63]	AB5
DDR0_DQ[7]	AD79
DDR0_DQ[8]	AE76
DDR0_DQ[9]	AD75
DDR0_DQS_DN[0]	AG80
DDR0_DQS_DN[1]	AJ74
DDR0_DQS_DN[10]	AE74
DDR0_DQS_DN[11]	AC68
DDR0_DQS_DN[12]	AE62
DDR0_DQS_DN[13]	AA24
DDR0_DQS_DN[14]	AC18
DDR0_DQS_DN[15]	AA12
DDR0_DQS_DN[16]	AC6
DDR0_DQS_DN[17]	AC56
DDR0_DQS_DN[2]	AG68
DDR0_DQS_DN[3]	AJ62
DDR0_DQS_DN[4]	AE24
DDR0_DQS_DN[5]	AG18
DDR0_DQS_DN[6]	AE12
DDR0_DQS_DN[7]	AG6
DDR0_DQS_DN[8]	AG56
DDR0_DQS_DN[9]	AC80
DDR0_DQS_DP[0]	AJ80
DDR0_DQS_DP[1]	AG74
DDR0_DQS_DP[10]	AC74

Table 2-1. Lands by Name (Sheet 5 of 94)

Land Name	Land No.
DDR0_DQS_DP[11]	AE68
DDR0_DQS_DP[12]	AC62
DDR0_DQS_DP[13]	AC24
DDR0_DQS_DP[14]	AA18
DDR0_DQS_DP[15]	AC12
DDR0_DQS_DP[16]	AA6
DDR0_DQS_DP[17]	AE56
DDR0_DQS_DP[2]	AJ68
DDR0_DQS_DP[3]	AG62
DDR0_DQS_DP[4]	AG24
DDR0_DQS_DP[5]	AE18
DDR0_DQS_DP[6]	AG12
DDR0_DQS_DP[7]	AE6
DDR0_DQS_DP[8]	AJ56
DDR0_DQS_DP[9]	AE80
DDR0_ECC[0]	AE58
DDR0_ECC[1]	AD57
DDR0_ECC[2]	AH55
DDR0_ECC[3]	AG54
DDR0_ECC[4]	AH57
DDR0_ECC[5]	AG58
DDR0_ECC[6]	AE54
DDR0_ECC[7]	AD55
DDR0_MA[0]	U36
DDR0_MA[1]	Y39
DDR0_MA[11]	W48
DDR0_MA[13]	W32
DDR0_MA[17]	Y31
DDR0_MA[2]	U40
DDR0_MA[3]	W40
DDR0_MA[4]	Y41
DDR0_MA[5]	T41
DDR0_MA[6]	W46
DDR0_MA[7]	Y47
DDR0_MA[8]	U46
DDR0_MA[9]	T47
DDR0_ODT[0]	U32
DDR0_ODT[1]	U30
DDR0_PAR	T37

Table 2-1. Lands by Name (Sheet 6 of 94)

Land Name	Land No.
DDR0_RAS_N_MA[16]	U34
DDR0_WE_N_MA[14]	T33
DDR012_DRAM_PWR_OK	AE42
DDR012_MEMHOT_N	W52
DDR012_RCOMP[0]	AE40
DDR012_RCOMP[1]	AE36
DDR012_RCOMP[2]	AE38
DDR012_RESET_N	U52
DDR012_VREFCA	Y53
DDR1_ACT_N	L50
DDR1_ALERT_N	P49
DDR1_AP_MA[10]	K35
DDR1_BA0	P35
DDR1_BA1	N36
DDR1_BC_N_MA[12]	L48
DDR1_BG0	K49
DDR1_BG1	N50
DDR1_C0_CS_N[2]	P29
DDR1_C1_CS_N[3]	K29
DDR1_C2	N30
DDR1_CAS_N_MA[15]	P33
DDR1_CKE[0]	P51
DDR1_CKE[1]	K51
DDR1_CLK_DN[0]	K39
DDR1_CLK_DN[2]	N38
DDR1_CLK_DP[0]	L38
DDR1_CLK_DP[2]	P37
DDR1_CS_N[0]	N34
DDR1_CS_N[1]	K31
DDR1_DQ[0]	V85
DDR1_DQ[1]	U84
DDR1_DQ[10]	AA76
DDR1_DQ[11]	Y75
DDR1_DQ[12]	Y79
DDR1_DQ[13]	AA78
DDR1_DQ[14]	V75
DDR1_DQ[15]	U76
DDR1_DQ[16]	V73
DDR1_DQ[17]	U72

Table 2-1. Lands by Name (Sheet 7 of 94)

Land Name	Land No.
DDR1_DQ[18]	AA70
DDR1_DQ[19]	Y69
DDR1_DQ[2]	AA82
DDR1_DQ[20]	AA72
DDR1_DQ[21]	Y73
DDR1_DQ[22]	V69
DDR1_DQ[23]	U70
DDR1_DQ[24]	V67
DDR1_DQ[25]	U66
DDR1_DQ[26]	AA64
DDR1_DQ[27]	Y63
DDR1_DQ[28]	Y67
DDR1_DQ[29]	AA66
DDR1_DQ[3]	Y81
DDR1_DQ[30]	V63
DDR1_DQ[31]	U64
DDR1_DQ[32]	T23
DDR1_DQ[33]	R22
DDR1_DQ[34]	W20
DDR1_DQ[35]	V19
DDR1_DQ[36]	V23
DDR1_DQ[37]	W22
DDR1_DQ[38]	T19
DDR1_DQ[39]	R20
DDR1_DQ[4]	Y85
DDR1_DQ[40]	T17
DDR1_DQ[41]	R16
DDR1_DQ[42]	W14
DDR1_DQ[43]	V13
DDR1_DQ[44]	V17
DDR1_DQ[45]	W16
DDR1_DQ[46]	T13
DDR1_DQ[47]	R14
DDR1_DQ[48]	T11
DDR1_DQ[49]	R10
DDR1_DQ[5]	AA84
DDR1_DQ[50]	W8
DDR1_DQ[51]	V7
DDR1_DQ[52]	W10

Table 2-1. Lands by Name (Sheet 8 of 94)

Land Name	Land No.
DDR1_DQ[53]	V11
DDR1_DQ[54]	T7
DDR1_DQ[55]	R8
DDR1_DQ[56]	T5
DDR1_DQ[57]	R4
DDR1_DQ[58]	W2
DDR1_DQ[59]	V1
DDR1_DQ[6]	V81
DDR1_DQ[60]	V5
DDR1_DQ[61]	W4
DDR1_DQ[62]	T1
DDR1_DQ[63]	R2
DDR1_DQ[7]	U82
DDR1_DQ[8]	V79
DDR1_DQ[9]	U78
DDR1_DQS_DN[0]	Y83
DDR1_DQS_DN[1]	AB77
DDR1_DQS_DN[10]	V77
DDR1_DQS_DN[11]	T71
DDR1_DQS_DN[12]	V65
DDR1_DQS_DN[13]	P21
DDR1_DQS_DN[14]	T15
DDR1_DQS_DN[15]	P9
DDR1_DQS_DN[16]	T3
DDR1_DQS_DN[17]	T59
DDR1_DQS_DN[2]	AB71
DDR1_DQS_DN[3]	AB65
DDR1_DQS_DN[4]	V21
DDR1_DQS_DN[5]	Y15
DDR1_DQS_DN[6]	V9
DDR1_DQS_DN[7]	Y3
DDR1_DQS_DN[8]	Y59
DDR1_DQS_DN[9]	T83
DDR1_DQS_DP[0]	AB83
DDR1_DQS_DP[1]	Y77
DDR1_DQS_DP[10]	T77
DDR1_DQS_DP[11]	V71
DDR1_DQS_DP[12]	T65
DDR1_DQS_DP[13]	T21

Table 2-1. Lands by Name (Sheet 9 of 94)

Land Name	Land No.
DDR1_DQS_DP[14]	P15
DDR1_DQS_DP[15]	T9
DDR1_DQS_DP[16]	P3
DDR1_DQS_DP[17]	V59
DDR1_DQS_DP[2]	Y71
DDR1_DQS_DP[3]	Y65
DDR1_DQS_DP[4]	Y21
DDR1_DQS_DP[5]	V15
DDR1_DQS_DP[6]	Y9
DDR1_DQS_DP[7]	V3
DDR1_DQS_DP[8]	AB59
DDR1_DQS_DP[9]	V83
DDR1_ECC[0]	V61
DDR1_ECC[1]	U60
DDR1_ECC[2]	AA58
DDR1_ECC[3]	Y57
DDR1_ECC[4]	AA60
DDR1_ECC[5]	Y61
DDR1_ECC[6]	V57
DDR1_ECC[7]	U58
DDR1_MA[0]	L36
DDR1_MA[1]	P39
DDR1_MA[11]	N48
DDR1_MA[13]	N32
DDR1_MA[17]	P31
DDR1_MA[2]	L40
DDR1_MA[3]	N40
DDR1_MA[4]	P41
DDR1_MA[5]	K41
DDR1_MA[6]	N46
DDR1_MA[7]	P47
DDR1_MA[8]	L46
DDR1_MA[9]	K47
DDR1_ODT[0]	L32
DDR1_ODT[1]	L30
DDR1_PAR	K37
DDR1_RAS_N_MA[16]	L34
DDR1_WE_N_MA[14]	K33
DDR2_ACT_N	E52

Table 2-1. Lands by Name (Sheet 10 of 94)

Land Name	Land No.
DDR2_ALERT_N	H51
DDR2_AP_MA[10]	H35
DDR2_BA0	E34
DDR2_BA1	G36
DDR2_BC_N_MA[12]	E50
DDR2_BG0	D51
DDR2_BG1	G52
DDR2_C0_CS_N[2]	H29
DDR2_C1_CS_N[3]	E28
DDR2_C2	D29
DDR2_CAS_N_MA[15]	E32
DDR2_CKE[0]	H53
DDR2_CKE[1]	D53
DDR2_CLK_DN[0]	H37
DDR2_CLK_DN[2]	E38
DDR2_CLK_DP[0]	G38
DDR2_CLK_DP[2]	D37
DDR2_CS_N[0]	D33
DDR2_CS_N[1]	H31
DDR2_DQ[0]	L82
DDR2_DQ[1]	K81
DDR2_DQ[10]	P73
DDR2_DQ[11]	N72
DDR2_DQ[12]	N76
DDR2_DQ[13]	P75
DDR2_DQ[14]	L72
DDR2_DQ[15]	K73
DDR2_DQ[16]	L70
DDR2_DQ[17]	K69
DDR2_DQ[18]	P67
DDR2_DQ[19]	N66
DDR2_DQ[2]	P79
DDR2_DQ[20]	P69
DDR2_DQ[21]	N70
DDR2_DQ[22]	L66
DDR2_DQ[23]	K67
DDR2_DQ[24]	L64
DDR2_DQ[25]	K63
DDR2_DQ[26]	P61

Table 2-1. Lands by Name (Sheet 11 of 94)

Land Name	Land No.
DDR2_DQ[27]	N60
DDR2_DQ[28]	N64
DDR2_DQ[29]	P63
DDR2_DQ[3]	N78
DDR2_DQ[30]	L60
DDR2_DQ[31]	K61
DDR2_DQ[32]	J26
DDR2_DQ[33]	H25
DDR2_DQ[34]	M23
DDR2_DQ[35]	L22
DDR2_DQ[36]	L26
DDR2_DQ[37]	M25
DDR2_DQ[38]	J22
DDR2_DQ[39]	H23
DDR2_DQ[4]	N82
DDR2_DQ[40]	J20
DDR2_DQ[41]	H19
DDR2_DQ[42]	M17
DDR2_DQ[43]	L16
DDR2_DQ[44]	L20
DDR2_DQ[45]	M19
DDR2_DQ[46]	J16
DDR2_DQ[47]	H17
DDR2_DQ[48]	J14
DDR2_DQ[49]	H13
DDR2_DQ[5]	P81
DDR2_DQ[50]	M11
DDR2_DQ[51]	L10
DDR2_DQ[52]	M13
DDR2_DQ[53]	L14
DDR2_DQ[54]	J10
DDR2_DQ[55]	H11
DDR2_DQ[56]	J8
DDR2_DQ[57]	H7
DDR2_DQ[58]	L4
DDR2_DQ[59]	M5
DDR2_DQ[6]	L78
DDR2_DQ[60]	L8
DDR2_DQ[61]	M7

Table 2-1. Lands by Name (Sheet 12 of 94)

Land Name	Land No.
DDR2_DQ[62]	H5
DDR2_DQ[63]	J4
DDR2_DQ[7]	K79
DDR2_DQ[8]	L76
DDR2_DQ[9]	K75
DDR2_DQS_DN[0]	N80
DDR2_DQS_DN[1]	R74
DDR2_DQS_DN[10]	L74
DDR2_DQS_DN[11]	J68
DDR2_DQS_DN[12]	L62
DDR2_DQS_DN[13]	G24
DDR2_DQS_DN[14]	J18
DDR2_DQS_DN[15]	G12
DDR2_DQS_DN[16]	J6
DDR2_DQS_DN[17]	J56
DDR2_DQS_DN[2]	N68
DDR2_DQS_DN[3]	R62
DDR2_DQS_DN[4]	L24
DDR2_DQS_DN[5]	N18
DDR2_DQS_DN[6]	L12
DDR2_DQS_DN[7]	N6
DDR2_DQS_DN[8]	N56
DDR2_DQS_DN[9]	J80
DDR2_DQS_DP[0]	R80
DDR2_DQS_DP[1]	N74
DDR2_DQS_DP[10]	J74
DDR2_DQS_DP[11]	L68
DDR2_DQS_DP[12]	J62
DDR2_DQS_DP[13]	J24
DDR2_DQS_DP[14]	G18
DDR2_DQS_DP[15]	J12
DDR2_DQS_DP[16]	G6
DDR2_DQS_DP[17]	L56
DDR2_DQS_DP[2]	R68
DDR2_DQS_DP[3]	N62
DDR2_DQS_DP[4]	N24
DDR2_DQS_DP[5]	L18
DDR2_DQS_DP[6]	N12
DDR2_DQS_DP[7]	L6

Table 2-1. Lands by Name (Sheet 13 of 94)

Land Name	Land No.
DDR2_DQS_DP[8]	R56
DDR2_DQS_DP[9]	L80
DDR2_ECC[0]	L58
DDR2_ECC[1]	K57
DDR2_ECC[2]	P55
DDR2_ECC[3]	N54
DDR2_ECC[4]	P57
DDR2_ECC[5]	N58
DDR2_ECC[6]	L54
DDR2_ECC[7]	K55
DDR2_MA[0]	D35
DDR2_MA[1]	H39
DDR2_MA[11]	G50
DDR2_MA[13]	D31
DDR2_MA[17]	E30
DDR2_MA[2]	G40
DDR2_MA[3]	H41
DDR2_MA[4]	G46
DDR2_MA[5]	H47
DDR2_MA[6]	G48
DDR2_MA[7]	H49
DDR2_MA[8]	E48
DDR2_MA[9]	D49
DDR2_ODT[0]	G32
DDR2_ODT[1]	G30
DDR2_PAR	E36
DDR2_RAS_N_MA[16]	G34
DDR2_WE_N_MA[14]	H33
DDR3_ACT_N	DL52
DDR3_ALERT_N	DG50
DDR3_AP_MA[10]	DH37
DDR3_BA0	DL36
DDR3_BA1	DG38
DDR3_BC_N_MA[12]	DL50
DDR3_BG0	DK51
DDR3_BG1	DH51
DDR3_C0_CS_N[2]	DL30
DDR3_C1_CS_N[3]	DH31
DDR3_C2	DK31

Table 2-1. Lands by Name (Sheet 14 of 94)

Land Name	Land No.
DDR3_CAS_N_MA[15]	DL34
DDR3_CKE[0]	DG52
DDR3_CKE[1]	DK53
DDR3_CLK_DN[0]	DK41
DDR3_CLK_DN[2]	DG40
DDR3_CLK_DP[0]	DL40
DDR3_CLK_DP[2]	DH39
DDR3_CS_N[0]	DK35
DDR3_CS_N[1]	DH33
DDR3_DQ[0]	DE82
DDR3_DQ[1]	DA82
DDR3_DQ[10]	DB73
DDR3_DQ[11]	DA74
DDR3_DQ[12]	DB77
DDR3_DQ[13]	DA76
DDR3_DQ[14]	DE74
DDR3_DQ[15]	DD73
DDR3_DQ[16]	DE70
DDR3_DQ[17]	DA70
DDR3_DQ[18]	DB67
DDR3_DQ[19]	DA68
DDR3_DQ[2]	DA80
DDR3_DQ[20]	DD71
DDR3_DQ[21]	DB71
DDR3_DQ[22]	DE68
DDR3_DQ[23]	DD67
DDR3_DQ[24]	DE64
DDR3_DQ[25]	DD65
DDR3_DQ[26]	DB61
DDR3_DQ[27]	DA62
DDR3_DQ[28]	DB65
DDR3_DQ[29]	DA64
DDR3_DQ[3]	DB79
DDR3_DQ[30]	DE62
DDR3_DQ[31]	DD61
DDR3_DQ[32]	DD25
DDR3_DQ[33]	DC26
DDR3_DQ[34]	CY23
DDR3_DQ[35]	DA22

Table 2-1. Lands by Name (Sheet 15 of 94)

Land Name	Land No.
DDR3_DQ[36]	DA26
DDR3_DQ[37]	CY25
DDR3_DQ[38]	DD23
DDR3_DQ[39]	DC22
DDR3_DQ[4]	DD83
DDR3_DQ[40]	DC20
DDR3_DQ[41]	DD19
DDR3_DQ[42]	CY17
DDR3_DQ[43]	DA16
DDR3_DQ[44]	DA20
DDR3_DQ[45]	CY19
DDR3_DQ[46]	DD17
DDR3_DQ[47]	DC16
DDR3_DQ[48]	DD13
DDR3_DQ[49]	DC14
DDR3_DQ[5]	DB83
DDR3_DQ[50]	CY11
DDR3_DQ[51]	DA10
DDR3_DQ[52]	DA14
DDR3_DQ[53]	CY13
DDR3_DQ[54]	DD11
DDR3_DQ[55]	DC10
DDR3_DQ[56]	DC8
DDR3_DQ[57]	DD7
DDR3_DQ[58]	DC4
DDR3_DQ[59]	DA4
DDR3_DQ[6]	DE80
DDR3_DQ[60]	DA8
DDR3_DQ[61]	CY7
DDR3_DQ[62]	DD5
DDR3_DQ[63]	CY5
DDR3_DQ[7]	DD79
DDR3_DQ[8]	DE76
DDR3_DQ[9]	DD77
DDR3_DQS_DN[0]	DF81
DDR3_DQS_DN[1]	DF75
DDR3_DQS_DN[10]	DB75
DDR3_DQS_DN[11]	CY69
DDR3_DQS_DN[12]	DB63

Table 2-1. Lands by Name (Sheet 16 of 94)

Land Name	Land No.
DDR3_DQS_DN[13]	DA24
DDR3_DQS_DN[14]	DA18
DDR3_DQS_DN[15]	DA12
DDR3_DQS_DN[16]	DA6
DDR3_DQS_DN[17]	DB57
DDR3_DQS_DN[2]	DF69
DDR3_DQS_DN[3]	DF63
DDR3_DQS_DN[4]	DE24
DDR3_DQS_DN[5]	DE18
DDR3_DQS_DN[6]	DE12
DDR3_DQS_DN[7]	DE6
DDR3_DQS_DN[8]	DF57
DDR3_DQS_DN[9]	CY81
DDR3_DQS_DP[0]	DD81
DDR3_DQS_DP[1]	DD75
DDR3_DQS_DP[10]	CY75
DDR3_DQS_DP[11]	DB69
DDR3_DQS_DP[12]	CY63
DDR3_DQS_DP[13]	CW24
DDR3_DQS_DP[14]	CW18
DDR3_DQS_DP[15]	CW12
DDR3_DQS_DP[16]	CW6
DDR3_DQS_DP[17]	CY57
DDR3_DQS_DP[2]	DD69
DDR3_DQS_DP[3]	DD63
DDR3_DQS_DP[4]	DC24
DDR3_DQS_DP[5]	DC18
DDR3_DQS_DP[6]	DC12
DDR3_DQS_DP[7]	DC6
DDR3_DQS_DP[8]	DD57
DDR3_DQS_DP[9]	DB81
DDR3_ECC[0]	DD59
DDR3_ECC[1]	DE58
DDR3_ECC[2]	DA56
DDR3_ECC[3]	DB55
DDR3_ECC[4]	DB59
DDR3_ECC[5]	DA58
DDR3_ECC[6]	DE56
DDR3_ECC[7]	DD55

Table 2-1. Lands by Name (Sheet 17 of 94)

Land Name	Land No.
DDR3_MA[0]	DK37
DDR3_MA[1]	DK45
DDR3_MA[11]	DH49
DDR3_MA[13]	DK33
DDR3_MA[17]	DL32
DDR3_MA[2]	DH45
DDR3_MA[3]	DL46
DDR3_MA[4]	DG46
DDR3_MA[5]	DK47
DDR3_MA[6]	DH47
DDR3_MA[7]	DG48
DDR3_MA[8]	DL48
DDR3_MA[9]	DK49
DDR3_ODT[0]	DG34
DDR3_ODT[1]	DG32
DDR3_PAR	DL38
DDR3_RAS_N_MA[16]	DG36
DDR3_WE_N_MA[14]	DH35
DDR345_DRAM_PWR_OK	CY47
DDR345_MEMHOT_N	CY49
DDR345_RCOMP[0]	DA46
DDR345_RCOMP[1]	DB47
DDR345_RCOMP[2]	DB45
DDR345_RESET_N	DA48
DDR345_VREFCA	DB49
DDR4_ACT_N	DU52
DDR4_ALERT_N	DN50
DDR4_AP_MA[10]	DT37
DDR4_BA0	DN36
DDR4_BA1	DN38
DDR4_BC_N_MA[12]	DU50
DDR4_BG0	DT51
DDR4_BG1	DP51
DDR4_C0_CS_N[2]	DN30
DDR4_C1_CS_N[3]	DT31
DDR4_C2	DP31
DDR4_CAS_N_MA[15]	DN34
DDR4_CKE[0]	DN52
DDR4_CKE[1]	DP53

Table 2-1. Lands by Name (Sheet 18 of 94)

Land Name	Land No.
DDR4_CLK_DN[0]	DT41
DDR4_CLK_DN[2]	DN40
DDR4_CLK_DP[0]	DU40
DDR4_CLK_DP[2]	DP39
DDR4_CS_N[0]	DP35
DDR4_CS_N[1]	DT33
DDR4_DQ[0]	DM85
DDR4_DQ[1]	DH85
DDR4_DQ[10]	DJ76
DDR4_DQ[11]	DH77
DDR4_DQ[12]	DJ80
DDR4_DQ[13]	DH79
DDR4_DQ[14]	DM77
DDR4_DQ[15]	DL76
DDR4_DQ[16]	DM73
DDR4_DQ[17]	DH73
DDR4_DQ[18]	DJ70
DDR4_DQ[19]	DH71
DDR4_DQ[2]	DH83
DDR4_DQ[20]	DL74
DDR4_DQ[21]	DJ74
DDR4_DQ[22]	DM71
DDR4_DQ[23]	DL70
DDR4_DQ[24]	DM67
DDR4_DQ[25]	DL68
DDR4_DQ[26]	DJ64
DDR4_DQ[27]	DH65
DDR4_DQ[28]	DJ68
DDR4_DQ[29]	DH67
DDR4_DQ[3]	DJ82
DDR4_DQ[30]	DM65
DDR4_DQ[31]	DL64
DDR4_DQ[32]	DL22
DDR4_DQ[33]	DK23
DDR4_DQ[34]	DG20
DDR4_DQ[35]	DH19
DDR4_DQ[36]	DH23
DDR4_DQ[37]	DG22
DDR4_DQ[38]	DL20

Table 2-1. Lands by Name (Sheet 19 of 94)

Land Name	Land No.
DDR4_DQ[39]	DK19
DDR4_DQ[4]	DP85
DDR4_DQ[40]	DK17
DDR4_DQ[41]	DL16
DDR4_DQ[42]	DG14
DDR4_DQ[43]	DH13
DDR4_DQ[44]	DH17
DDR4_DQ[45]	DG16
DDR4_DQ[46]	DL14
DDR4_DQ[47]	DK13
DDR4_DQ[48]	DL10
DDR4_DQ[49]	DK11
DDR4_DQ[5]	DF85
DDR4_DQ[50]	DG8
DDR4_DQ[51]	DH7
DDR4_DQ[52]	DH11
DDR4_DQ[53]	DG10
DDR4_DQ[54]	DL8
DDR4_DQ[55]	DK7
DDR4_DQ[56]	DK5
DDR4_DQ[57]	DL4
DDR4_DQ[58]	DN2
DDR4_DQ[59]	DE2
DDR4_DQ[6]	DM83
DDR4_DQ[60]	DH5
DDR4_DQ[61]	DG4
DDR4_DQ[62]	DL2
DDR4_DQ[63]	DG2
DDR4_DQ[7]	DL82
DDR4_DQ[8]	DM79
DDR4_DQ[9]	DL80
DDR4_DQS_DN[0]	DN84
DDR4_DQS_DN[1]	DN78
DDR4_DQS_DN[10]	DJ78
DDR4_DQS_DN[11]	DJ72
DDR4_DQS_DN[12]	DJ66
DDR4_DQS_DN[13]	DH21
DDR4_DQS_DN[14]	DH15
DDR4_DQS_DN[15]	DH9

Table 2-1. Lands by Name (Sheet 20 of 94)

Land Name	Land No.
DDR4_DQS_DN[16]	DH3
DDR4_DQS_DN[17]	DJ60
DDR4_DQS_DN[2]	DN72
DDR4_DQS_DN[3]	DN66
DDR4_DQS_DN[4]	DM21
DDR4_DQS_DN[5]	DM15
DDR4_DQS_DN[6]	DM9
DDR4_DQS_DN[7]	DM3
DDR4_DQS_DN[8]	DN60
DDR4_DQS_DN[9]	DG84
DDR4_DQS_DP[0]	DL84
DDR4_DQS_DP[1]	DL78
DDR4_DQS_DP[10]	DG78
DDR4_DQS_DP[11]	DG72
DDR4_DQS_DP[12]	DG66
DDR4_DQS_DP[13]	DF21
DDR4_DQS_DP[14]	DF15
DDR4_DQS_DP[15]	DF9
DDR4_DQS_DP[16]	DF3
DDR4_DQS_DP[17]	DG60
DDR4_DQS_DP[2]	DL72
DDR4_DQS_DP[3]	DL66
DDR4_DQS_DP[4]	DK21
DDR4_DQS_DP[5]	DK15
DDR4_DQS_DP[6]	DK9
DDR4_DQS_DP[7]	DK3
DDR4_DQS_DP[8]	DL60
DDR4_DQS_DP[9]	DJ84
DDR4_ECC[0]	DL62
DDR4_ECC[1]	DM61
DDR4_ECC[2]	DH59
DDR4_ECC[3]	DJ58
DDR4_ECC[4]	DJ62
DDR4_ECC[5]	DH61
DDR4_ECC[6]	DM59
DDR4_ECC[7]	DL58
DDR4_MA[0]	DP37
DDR4_MA[1]	DT45
DDR4_MA[11]	DP49

Table 2-1. Lands by Name (Sheet 21 of 94)

Land Name	Land No.
DDR4_MA[13]	DP33
DDR4_MA[17]	DN32
DDR4_MA[2]	DP45
DDR4_MA[3]	DU46
DDR4_MA[4]	DN46
DDR4_MA[5]	DT47
DDR4_MA[6]	DP47
DDR4_MA[7]	DN48
DDR4_MA[8]	DU48
DDR4_MA[9]	DT49
DDR4_ODT[0]	DU34
DDR4_ODT[1]	DU32
DDR4_PAR	DU38
DDR4_RAS_N_MA[16]	DU36
DDR4_WE_N_MA[14]	DT35
DDR5_ACT_N	DY53
DDR5_ALERT_N	EB51
DDR5_AP_MA[10]	EC36
DDR5_BA0	EB35
DDR5_BA1	EB37
DDR5_BC_N_MA[12]	DY51
DDR5_BG0	DW52
DDR5_BG1	EC52
DDR5_C0_CS_N[2]	EB29
DDR5_C1_CS_N[3]	DY29
DDR5_C2	EC30
DDR5_CAS_N_MA[15]	EB33
DDR5_CKE[0]	EB53
DDR5_CKE[1]	EC54
DDR5_CLK_DN[0]	DW40
DDR5_CLK_DN[2]	DY37
DDR5_CLK_DP[0]	DY39
DDR5_CLK_DP[2]	DW38
DDR5_CS_N[0]	EC34
DDR5_CS_N[1]	DY31
DDR5_DQ[0]	DW82
DDR5_DQ[1]	DR82
DDR5_DQ[10]	DT73
DDR5_DQ[11]	DR74

Table 2-1. Lands by Name (Sheet 22 of 94)

Land Name	Land No.
DDR5_DQ[12]	DT77
DDR5_DQ[13]	DR76
DDR5_DQ[14]	DW74
DDR5_DQ[15]	DV73
DDR5_DQ[16]	DW70
DDR5_DQ[17]	DR70
DDR5_DQ[18]	DT67
DDR5_DQ[19]	DR68
DDR5_DQ[2]	DR80
DDR5_DQ[20]	DV71
DDR5_DQ[21]	DT71
DDR5_DQ[22]	DW68
DDR5_DQ[23]	DV67
DDR5_DQ[24]	DW64
DDR5_DQ[25]	DV65
DDR5_DQ[26]	DT61
DDR5_DQ[27]	DR62
DDR5_DQ[28]	DT65
DDR5_DQ[29]	DR64
DDR5_DQ[3]	DT79
DDR5_DQ[30]	DW62
DDR5_DQ[31]	DV61
DDR5_DQ[32]	DV25
DDR5_DQ[33]	DU26
DDR5_DQ[34]	DP23
DDR5_DQ[35]	DR22
DDR5_DQ[36]	DR26
DDR5_DQ[37]	DP25
DDR5_DQ[38]	DV23
DDR5_DQ[39]	DU22
DDR5_DQ[4]	DV83
DDR5_DQ[40]	DU20
DDR5_DQ[41]	DV19
DDR5_DQ[42]	DU16
DDR5_DQ[43]	DW16
DDR5_DQ[44]	DR20
DDR5_DQ[45]	DP19
DDR5_DQ[46]	DP17
DDR5_DQ[47]	DR16

Table 2-1. Lands by Name (Sheet 23 of 94)

Land Name	Land No.
DDR5_DQ[48]	DV13
DDR5_DQ[49]	DU14
DDR5_DQ[5]	DT83
DDR5_DQ[50]	DP11
DDR5_DQ[51]	DR10
DDR5_DQ[52]	DR14
DDR5_DQ[53]	DP13
DDR5_DQ[54]	DV11
DDR5_DQ[55]	DU10
DDR5_DQ[56]	DU8
DDR5_DQ[57]	DV7
DDR5_DQ[58]	DU4
DDR5_DQ[59]	DR4
DDR5_DQ[6]	DW80
DDR5_DQ[60]	DR8
DDR5_DQ[61]	DP7
DDR5_DQ[62]	DV5
DDR5_DQ[63]	DP5
DDR5_DQ[7]	DV79
DDR5_DQ[8]	DW76
DDR5_DQ[9]	DV77
DDR5_DQS_DN[0]	DY81
DDR5_DQS_DN[1]	DY75
DDR5_DQS_DN[10]	DT75
DDR5_DQS_DN[11]	DP69
DDR5_DQS_DN[12]	DT63
DDR5_DQS_DN[13]	DN24
DDR5_DQS_DN[14]	DR18
DDR5_DQS_DN[15]	DN12
DDR5_DQS_DN[16]	DR6
DDR5_DQS_DN[17]	DT57
DDR5_DQS_DN[2]	DY69
DDR5_DQS_DN[3]	DY63
DDR5_DQS_DN[4]	DU24
DDR5_DQS_DN[5]	DU18
DDR5_DQS_DN[6]	DW12
DDR5_DQS_DN[7]	DW6
DDR5_DQS_DN[8]	DY57
DDR5_DQS_DN[9]	DP81

Table 2-1. Lands by Name (Sheet 24 of 94)

Land Name	Land No.
DDR5_DQS_DP[0]	DV81
DDR5_DQS_DP[1]	DV75
DDR5_DQS_DP[10]	DP75
DDR5_DQS_DP[11]	DT69
DDR5_DQS_DP[12]	DP63
DDR5_DQS_DP[13]	DR24
DDR5_DQS_DP[14]	DN18
DDR5_DQS_DP[15]	DR12
DDR5_DQS_DP[16]	DN6
DDR5_DQS_DP[17]	DP57
DDR5_DQS_DP[2]	DV69
DDR5_DQS_DP[3]	DV63
DDR5_DQS_DP[4]	DW24
DDR5_DQS_DP[5]	DV17
DDR5_DQS_DP[6]	DU12
DDR5_DQS_DP[7]	DU6
DDR5_DQS_DP[8]	DV57
DDR5_DQS_DP[9]	DT81
DDR5_ECC[0]	DV59
DDR5_ECC[1]	DW58
DDR5_ECC[2]	DR56
DDR5_ECC[3]	DT55
DDR5_ECC[4]	DT59
DDR5_ECC[5]	DR58
DDR5_ECC[6]	DW56
DDR5_ECC[7]	DV55
DDR5_MA[0]	DY35
DDR5_MA[1]	DY45
DDR5_MA[11]	EC50
DDR5_MA[13]	EC32
DDR5_MA[17]	EB31
DDR5_MA[2]	DW46
DDR5_MA[3]	DY47
DDR5_MA[4]	EB47
DDR5_MA[5]	DW48
DDR5_MA[6]	EC48
DDR5_MA[7]	EB49
DDR5_MA[8]	DY49
DDR5_MA[9]	DW50

Table 2-1. Lands by Name (Sheet 25 of 94)

Land Name	Land No.
DDR5_ODT[0]	DW32
DDR5_ODT[1]	DW30
DDR5_PAR	DW36
DDR5_RAS_N_MA[16]	DW34
DDR5_WE_N_MA[14]	DY33
DEBUG_EN_N	DB31
DMI_RX_DN[0]	BG72
DMI_RX_DN[1]	BF73
DMI_RX_DN[2]	BG74
DMI_RX_DN[3]	BF75
DMI_RX_DP[0]	BE72
DMI_RX_DP[1]	BD73
DMI_RX_DP[2]	BE74
DMI_RX_DP[3]	BD75
DMI_TX_DN[0]	AY75
DMI_TX_DN[1]	BA76
DMI_TX_DN[2]	AY73
DMI_TX_DN[3]	BA74
DMI_TX_DP[0]	AV75
DMI_TX_DP[1]	AW76
DMI_TX_DP[2]	AV73
DMI_TX_DP[3]	AW74
EAR_N	EA4
ERROR_N[0]	AD33
ERROR_N[1]	AC34
ERROR_N[2]	AB33
OBS[0]	CE10
OBS[1]	CG8
OBS[10]	CL8
OBS[11]	CL6
OBS[12]	CK5
OBS[13]	CL4
OBS[14]	CJ6
OBS[15]	CE6
OBS[2]	CJ8
OBS[3]	CM9
OBS[4]	CG10
OBS[5]	CK9
OBS[6]	CF11

Table 2-1. Lands by Name (Sheet 26 of 94)

Land Name	Land No.
OBS[7]	CF9
OBS[8]	CE8
OBS[9]	CK7
OBSSTB_N[0]	CF7
OBSSTB_N[1]	CF5
OBSSTB_P[0]	CG6
OBSSTB_P[1]	CE4
PE_REFCLK_DN	AW70
PE_REFCLK_DP	BA70
PE1A_RX_DN[0]	BA86
PE1A_RX_DN[1]	AY85
PE1A_RX_DN[2]	BA84
PE1A_RX_DN[3]	AY83
PE1A_RX_DP[0]	AW86
PE1A_RX_DP[1]	AV85
PE1A_RX_DP[2]	AW84
PE1A_RX_DP[3]	AV83
PE1A_TX_DN[0]	BF85
PE1A_TX_DN[1]	BG84
PE1A_TX_DN[2]	BF83
PE1A_TX_DN[3]	BG82
PE1A_TX_DP[0]	BD85
PE1A_TX_DP[1]	BE84
PE1A_TX_DP[2]	BD83
PE1A_TX_DP[3]	BE82
PE1B_RX_DN[4]	BA82
PE1B_RX_DN[5]	AY81
PE1B_RX_DN[6]	BA80
PE1B_RX_DN[7]	AY79
PE1B_RX_DP[4]	AW82
PE1B_RX_DP[5]	AV81
PE1B_RX_DP[6]	AW80
PE1B_RX_DP[7]	AV79
PE1B_TX_DN[4]	BF81
PE1B_TX_DN[5]	BG80
PE1B_TX_DN[6]	BF79
PE1B_TX_DN[7]	BG78
PE1B_TX_DP[4]	BD81
PE1B_TX_DP[5]	BE80

Table 2-1. Lands by Name (Sheet 27 of 94)

Land Name	Land No.
PE1B_TX_DP[6]	BD79
PE1B_TX_DP[7]	BE78
PE2A_RX_DN[0]	CK81
PE2A_RX_DN[1]	CL82
PE2A_RX_DN[2]	CK83
PE2A_RX_DN[3]	CL84
PE2A_RX_DP[0]	CH81
PE2A_RX_DP[1]	CJ82
PE2A_RX_DP[2]	CH83
PE2A_RX_DP[3]	CJ84
PE2A_TX_DN[0]	CD79
PE2A_TX_DN[1]	CE80
PE2A_TX_DN[2]	CD81
PE2A_TX_DN[3]	CE82
PE2A_TX_DP[0]	CB79
PE2A_TX_DP[1]	CC80
PE2A_TX_DP[2]	CB81
PE2A_TX_DP[3]	CC82
PE2B_RX_DN[4]	CL80
PE2B_RX_DN[5]	CK79
PE2B_RX_DN[6]	CL78
PE2B_RX_DN[7]	CK77
PE2B_RX_DP[4]	CJ80
PE2B_RX_DP[5]	CH79
PE2B_RX_DP[6]	CJ78
PE2B_RX_DP[7]	CH77
PE2B_TX_DN[4]	CE84
PE2B_TX_DN[5]	CD83
PE2B_TX_DN[6]	CE78
PE2B_TX_DN[7]	CD77
PE2B_TX_DP[4]	CC84
PE2B_TX_DP[5]	CB83
PE2B_TX_DP[6]	CC78
PE2B_TX_DP[7]	CB77
PE2C_RX_DN[10]	CL74
PE2C_RX_DN[11]	CK73
PE2C_RX_DN[8]	CL76
PE2C_RX_DN[9]	CK75
PE2C_RX_DP[10]	CJ74

Table 2-1. Lands by Name (Sheet 28 of 94)

Land Name	Land No.
PE2C_RX_DP[11]	CH73
PE2C_RX_DP[8]	CJ76
PE2C_RX_DP[9]	CH75
PE2C_TX_DN[10]	CE74
PE2C_TX_DN[11]	CD73
PE2C_TX_DN[8]	CE76
PE2C_TX_DN[9]	CD75
PE2C_TX_DP[10]	CC74
PE2C_TX_DP[11]	CB73
PE2C_TX_DP[8]	CC76
PE2C_TX_DP[9]	CB75
PE2D_RX_DN[12]	CL72
PE2D_RX_DN[13]	CK71
PE2D_RX_DN[14]	CL70
PE2D_RX_DN[15]	CK69
PE2D_RX_DP[12]	CJ72
PE2D_RX_DP[13]	CH71
PE2D_RX_DP[14]	CJ70
PE2D_RX_DP[15]	CH69
PE2D_TX_DN[12]	CE72
PE2D_TX_DN[13]	CD71
PE2D_TX_DN[14]	CE70
PE2D_TX_DN[15]	CD69
PE2D_TX_DP[12]	CC72
PE2D_TX_DP[13]	CB71
PE2D_TX_DP[14]	CC70
PE2D_TX_DP[15]	CB69
PE3A_RX_DN[0]	BM83
PE3A_RX_DN[1]	BN82
PE3A_RX_DN[2]	BM81
PE3A_RX_DN[3]	BN80
PE3A_RX_DP[0]	BK83
PE3A_RX_DP[1]	BL82
PE3A_RX_DP[2]	BK81
PE3A_RX_DP[3]	BL80
PE3A_TX_DN[0]	BW84
PE3A_TX_DN[1]	BV83
PE3A_TX_DN[2]	BW82
PE3A_TX_DN[3]	BV81

Table 2-1. Lands by Name (Sheet 29 of 94)

Land Name	Land No.
PE3A_TX_DP[0]	BU84
PE3A_TX_DP[1]	BT83
PE3A_TX_DP[2]	BU82
PE3A_TX_DP[3]	BT81
PE3B_RX_DN[4]	BM79
PE3B_RX_DN[5]	BN78
PE3B_RX_DN[6]	BM77
PE3B_RX_DN[7]	BN76
PE3B_RX_DP[4]	BK79
PE3B_RX_DP[5]	BL78
PE3B_RX_DP[6]	BK77
PE3B_RX_DP[7]	BL76
PE3B_TX_DN[4]	BW80
PE3B_TX_DN[5]	BV79
PE3B_TX_DN[6]	BW78
PE3B_TX_DN[7]	BV77
PE3B_TX_DP[4]	BU80
PE3B_TX_DP[5]	BT79
PE3B_TX_DP[6]	BU78
PE3B_TX_DP[7]	BT77
PE3C_RX_DN[10]	BM73
PE3C_RX_DN[11]	BN72
PE3C_RX_DN[8]	BM75
PE3C_RX_DN[9]	BN74
PE3C_RX_DP[10]	BK73
PE3C_RX_DP[11]	BL72
PE3C_RX_DP[8]	BK75
PE3C_RX_DP[9]	BL74
PE3C_TX_DN[10]	BW74
PE3C_TX_DN[11]	BV73
PE3C_TX_DN[8]	BW76
PE3C_TX_DN[9]	BV75
PE3C_TX_DP[10]	BU74
PE3C_TX_DP[11]	BT73
PE3C_TX_DP[8]	BU76
PE3C_TX_DP[9]	BT75
PE3D_RX_DN[12]	BM71
PE3D_RX_DN[13]	BN70
PE3D_RX_DN[14]	BM69

Table 2-1. Lands by Name (Sheet 30 of 94)

Land Name	Land No.
PE3D_RX_DN[15]	BN68
PE3D_RX_DP[12]	BK71
PE3D_RX_DP[13]	BL70
PE3D_RX_DP[14]	BK69
PE3D_RX_DP[15]	BL68
PE3D_TX_DN[12]	BW72
PE3D_TX_DN[13]	BV71
PE3D_TX_DN[14]	BW70
PE3D_TX_DN[15]	BV69
PE3D_TX_DP[12]	BU72
PE3D_TX_DP[13]	BT71
PE3D_TX_DP[14]	BU70
PE3D_TX_DP[15]	BT69
PECI	CV29
PMSYNC	CU30
PRDY_N	CN26
PREQ_N	DE28
PROCHOT_N	CP25
RESET_N	DC30
RSVD	D11
RSVD	D13
RSVD	D15
RSVD	D25
RSVD	D27
RSVD	D3
RSVD	D5
RSVD	D55
RSVD	D57
RSVD	D59
RSVD	D7
RSVD	B79
RSVD	B81
RSVD	D9
RSVD	AD1
RSVD	AD31
RSVD	AD85
RSVD	AE2
RSVD	AE32
RSVD	AE84

Table 2-1. Lands by Name (Sheet 31 of 94)

Land Name	Land No.
RSVD	AE86
RSVD	AF1
RSVD	AG2
RSVD	AH21
RSVD	AH27
RSVD	AJ22
RSVD	AK23
RSVD	AK25
RSVD	AK27
RSVD	AK59
RSVD	AL24
RSVD	AL60
RSVD	AM61
RSVD	AM63
RSVD	AN26
RSVD	AN62
RSVD	AN64
RSVD	AP1
RSVD	AP25
RSVD	AP27
RSVD	AR2
RSVD	AR64
RSVD	AU64
RSVD	AW64
RSVD	AV65
RSVD	BC70
RSVD	E10
RSVD	E14
RSVD	E16
RSVD	E26
RSVD	E4
RSVD	E56
RSVD	E58
RSVD	E60
RSVD	C74
RSVD	E8
RSVD	C80
RSVD	C82
RSVD	BD69

Table 2-1. Lands by Name (Sheet 32 of 94)

Land Name	Land No.
RSVD	BF69
RSVD	BF71
RSVD	BG70
RSVD	BH69
RSVD	BJ84
RSVD	BN84
RSVD	F15
RSVD	F55
RSVD	F57
RSVD	F59
RSVD	F61
RSVD	D73
RSVD	D81
RSVD	F9
RSVD	CE12
RSVD	CE16
RSVD	CE18
RSVD	CE66
RSVD	CF13
RSVD	CF17
RSVD	CF3
RSVD	CF67
RSVD	CG12
RSVD	CG18
RSVD	CG2
RSVD	CG4
RSVD	CG66
RSVD	CH13
RSVD	CH3
RSVD	CH5
RSVD	CH67
RSVD	CJ4
RSVD	CK3
RSVD	CL2
RSVD	CL24
RSVD	CN24
RSVD	CN28
RSVD	CY1
RSVD	DA28

Table 2-1. Lands by Name (Sheet 33 of 94)

Land Name	Land No.
RSVD	DB1
RSVD	DC28
RSVD	G2
RSVD	G58
RSVD	G60
RSVD	G82
RSVD	DG54
RSVD	DH29
RSVD	DH53
RSVD	DH55
RSVD	DK29
RSVD	DK55
RSVD	DL28
RSVD	DL54
RSVD	DM55
RSVD	DN28
RSVD	DN54
RSVD	DP29
RSVD	DT29
RSVD	DT53
RSVD	DU2
RSVD	DU28
RSVD	DV85
RSVD	DW2
RSVD	DW28
RSVD	DY85
RSVD	EA10
RSVD	EA78
RSVD	EB13
RSVD	EB15
RSVD	EB61
RSVD	EB7
RSVD	EB73
RSVD	EB77
RSVD	EB79
RSVD	EB83
RSVD	EB85
RSVD	EB9
RSVD	EC10

Table 2-1. Lands by Name (Sheet 34 of 94)

Land Name	Land No.
RSVD	EC12
RSVD	EC14
RSVD	EC16
RSVD	EC6
RSVD	EC62
RSVD	EC72
RSVD	EC74
RSVD	EC76
RSVD	EC78
RSVD	EC8
RSVD	EC82
RSVD	H1
RSVD	H59
RSVD	H71
RSVD	J84
RSVD	J86
RSVD	K1
RSVD	L2
RSVD	L28
RSVD	L84
RSVD	L86
RSVD	M1
RSVD	M85
RSVD	N52
RSVD	N84
RSVD	N86
RSVD	P27
RSVD	P85
RSVD	R26
RSVD	R86
RSVD	T27
RSVD	U26
RSVD	V27
RSVD	AB1
RSVD	AC2
RSVD	AC86
RSVD	EF83
RSVD	EF59
RSVD	EA66

Table 2-1. Lands by Name (Sheet 35 of 94)

Land Name	Land No.
RSVD	EA64
RSVD	EA24
RSVD	EA22
RSVD	EA20
RSVD	EA18
RSVD	DY67
RSVD	DY65
RSVD	DY23
RSVD	DY21
RSVD	EF57
RSVD	DY19
RSVD	DY17
RSVD	DW22
RSVD	DW20
RSVD	DW18
RSVD	CU42
RSVD	EF55
RSVD	CT41
RSVD	EF53
RSVD	EF51
RSVD	EF49
RSVD	H69
RSVD	H67
RSVD	H65
RSVD	G70
RSVD	G68
RSVD	G66
RSVD	G64
RSVD	EF47
RSVD	G22
RSVD	G20
RSVD	F69
RSVD	F67
RSVD	F65
RSVD	F63
RSVD	F23
RSVD	F21
RSVD	F19
RSVD	E84

Table 2-1. Lands by Name (Sheet 36 of 94)

Land Name	Land No.
RSVD	EF45
RSVD	E66
RSVD	E64
RSVD	E62
RSVD	E22
RSVD	E20
RSVD	E18
RSVD	D83
RSVD	D65
RSVD	D63
RSVD	D61
RSVD	EE84
RSVD	D45
RSVD	D43
RSVD	D17
RSVD	C64
RSVD	C62
RSVD	C60
RSVD	C58
RSVD	C56
RSVD	C54
RSVD	C52
RSVD	EE82
RSVD	C50
RSVD	C48
RSVD	C46
RSVD	C42
RSVD	C40
RSVD	C38
RSVD	C36
RSVD	C34
RSVD	C32
RSVD	C30
RSVD	EF81
RSVD	EE80
RSVD	C28
RSVD	C26
RSVD	C24
RSVD	C18

Table 2-1. Lands by Name (Sheet 37 of 94)

Land Name	Land No.
RSVD	C16
RSVD	C14
RSVD	C12
RSVD	C10
RSVD	C8
RSVD	C6
RSVD	EE78
RSVD	C4
RSVD	B63
RSVD	B61
RSVD	B59
RSVD	B57
RSVD	B55
RSVD	B53
RSVD	B51
RSVD	B49
RSVD	B47
RSVD	EE76
RSVD	B43
RSVD	B41
RSVD	B39
RSVD	B37
RSVD	B35
RSVD	B33
RSVD	B31
RSVD	B29
RSVD	B27
RSVD	B25
RSVD	EE74
RSVD	B17
RSVD	B15
RSVD	B13
RSVD	B11
RSVD	B9
RSVD	B7
RSVD	B5
RSVD	B3
RSVD	A42
RSVD	A40

Table 2-1. Lands by Name (Sheet 38 of 94)

Land Name	Land No.
RSVD	EE72
RSVD	A38
RSVD	A36
RSVD	A34
RSVD	A32
RSVD	A30
RSVD	A28
RSVD	A26
RSVD	A24
RSVD	A16
RSVD	A14
RSVD	EE70
RSVD	A12
RSVD	A10
RSVD	A8
RSVD	A6
RSVD	A4
RSVD	EE62
RSVD	EE60
RSVD	EE58
RSVD	EE56
RSVD	EF79
RSVD	EE54
RSVD	EE52
RSVD	EE50
RSVD	EE48
RSVD	EE46
RSVD	EE44
RSVD	EE40
RSVD	EE38
RSVD	EE36
RSVD	EE34
RSVD	EF77
RSVD	EE32
RSVD	EE30
RSVD	EE28
RSVD	EE26
RSVD	EE24
RSVD	EE16

Table 2-1. Lands by Name (Sheet 39 of 94)

Land Name	Land No.
RSVD	EE14
RSVD	EE12
RSVD	EE10
RSVD	EE8
RSVD	EF75
RSVD	EE6
RSVD	ED83
RSVD	ED81
RSVD	ED79
RSVD	ED77
RSVD	ED75
RSVD	ED73
RSVD	ED71
RSVD	ED69
RSVD	ED63
RSVD	EF73
RSVD	ED61
RSVD	ED59
RSVD	ED57
RSVD	ED55
RSVD	ED53
RSVD	ED51
RSVD	ED49
RSVD	ED47
RSVD	ED45
RSVD	ED41
RSVD	EF71
RSVD	ED39
RSVD	ED37
RSVD	ED35
RSVD	ED33
RSVD	ED31
RSVD	ED29
RSVD	ED27
RSVD	ED25
RSVD	ED23
RSVD	ED15
RSVD	EF63
RSVD	ED13

Table 2-1. Lands by Name (Sheet 40 of 94)

Land Name	Land No.
RSVD	ED11
RSVD	ED9
RSVD	ED7
RSVD	ED5
RSVD	EC70
RSVD	EC44
RSVD	EC42
RSVD	EC26
RSVD	EC24
RSVD	EF61
RSVD	EC22
RSVD	EC4
RSVD	EB69
RSVD	EB67
RSVD	EB65
RSVD	EB25
RSVD	EB23
RSVD	EB21
RSVD	EB3
RSVD	EA68
RSVD	DF29
RSVD	DG26
RSVD	DG28
RSVD	DH25
RSVD	DH27
RSVD	DJ26
RSVD	DJ28
RSVD	DK25
RSVD	DK27
RSVD	DL26
RSVD	DM27
RSVD	DY27
RSVD	EA26
RSVD	EA60
RSVD	EB27
RSVD	EB59
RSVD	EC56
RSVD	EC58
RSVD	EC60

Table 2-1. Lands by Name (Sheet 41 of 94)

Land Name	Land No.
SKTOCC_N	DA2
SPDSCL0	CK23
SPDSDA0	CM23
SVIDALERT_N	AR24
SVIDCLK	AJ26
SVIDDATA	AN24
TCK	DB29
TDI	CP29
TDO	DA30
TEST[0]	B75
TEST[10]	AT75
TEST[11]	AT77
TEST[13]	D75
TEST[14]	CE14
TEST[15]	CE2
TEST[16]	CF15
TEST[17]	CG14
TEST[18]	CG16
TEST[19]	CJ66
TEST[20]	CK67
TEST[21]	CL66
TEST[22]	CM67
TEST[26]	CT25
TEST[27]	AR26
TEST[28]	CM25
TEST[29]	DB33
TEST[30]	DA32
TEST[31]	DC32
TEST[32]	CY31
TEST[4]	AP3
TEST[5]	AP5
TEST[6]	AR4
TEST[7]	AR6
TEST[8]	AR76
TEST[9]	AR78
THERMTRIP_N	AM25
TMS	CT29
TRST_N	CY29
VCC_CDCORE	BW66

Table 2-1. Lands by Name (Sheet 42 of 94)

Land Name	Land No.
VCC_CDCORE	BV67
VCC_CDCORE	BV65
VCC_CDCORE	BU66
VCC_CDCORE	BT67
VCC_CDCORE	BT65
VCC_CDCORE	BR66
VCC_CDCORE	BN66
VCC_CDCORE	BM65
VCC_CDCORE	BL66
VCC_CDCORE	BK65
VCC_CDCORE	BJ66
VCC_CDCORE	BH67
VCC_CDCORE_SENSE	CA66
VCCCLR	CJ64
VCCCLR	CJ62
VCCCLR	CH63
VCCCLR	CH61
VCCCLR	CG64
VCCCLR	CG62
VCCCLR	CG60
VCCCLR	CF63
VCCCLR	CF61
VCCCLR	CE64
VCCCLR	CE60
VCCCLR	CD63
VCCCLR	CD61
VCCCLR	CC62
VCCCLR	CB63
VCCCLR	CB61
VCCCLR	CA64
VCCCLR	CA62
VCCCLR	CA60
VCCCLR	BY61
VCCCLR	BW64
VCCCLR	BW62
VCCCLR	BW60
VCCCLR	BV63
VCCCLR	BV61
VCCCLR	BU62

Table 2-1. Lands by Name (Sheet 43 of 94)

Land Name	Land No.
VCCCLR	BT61
VCCCLR	BR64
VCCCLR	BR62
VCCCLR	BR60
VCCCLR	BP63
VCCCLR	BP61
VCCCLR	BN64
VCCCLR	BN62
VCCCLR	BN60
VCCCLR	BM61
VCCCLR	BL62
VCCCLR	BK63
VCCCLR	BK61
VCCCLR	BJ64
VCCCLR	BJ62
VCCCLR	BJ60
VCCCLR	BH63
VCCCLR	BH61
VCCCLR	BG64
VCCCLR	BG62
VCCCLR	BG60
VCCCLR	BF61
VCCCLR	BE62
VCCCLR	BD63
VCCCLR	BD61
VCCCLR	BC62
VCCCLR	BC60
VCCCLR	BB63
VCCCLR	BB61
VCCCLR	BA62
VCCCLR	AY63
VCCCLR	AY61
VCCCLR	AW62
VCCCLR	AV61
VCCCLR	AV59
VCCCLR	AU62
VCCCLR	AU60
VCCCLR	AU58
VCCCLR	AT61

Table 2-1. Lands by Name (Sheet 44 of 94)

Land Name	Land No.
VCCCLR	AT59
VCCCLR	AT57
VCCCLR	AR60
VCCCLR	AR56
VCCCLR	AP59
VCCCLR	AP57
VCCCLR	AP55
VCCCLR	AN58
VCCCLR	AN56
VCCCLR	AN54
VCCCLR	AM53
VCCCLR	AL54
VCCCLR	AL52
VCCCLR	AL50
VCCCLR	AL48
VCCCLR	AL46
VCCCLR	AK53
VCCCLR	AK51
VCCCLR	AK49
VCCCLR	AK47
VCCCLR	AK45
VCCCLR	AJ50
VCCCLR	AJ48
VCCCLR	AJ46
VCCCLR	AH51
VCCCLR	AH49
VCCCLR	AH47
VCCCLR	AH45
VCCCLR	AG50
VCCCLR	AG48
VCCCLR	AG46
VCCCLR	AF51
VCCCLR	AF49
VCCCLR	AF47
VCCCLR	AF45
VCCCLR	AE50
VCCCLR	AE48
VCCCLR	AE46
VCCCLR	AD49

Table 2-1. Lands by Name (Sheet 45 of 94)

Land Name	Land No.
VCCCLR	AD47
VCCCLR	AD45
VCCCLR_SENSE	AM57
VCCD012	AA30
VCCD012	AA32
VCCD012	AA34
VCCD012	AA36
VCCD012	AA38
VCCD012	AA40
VCCD012	AA42
VCCD012	AA46
VCCD012	AA48
VCCD012	AA50
VCCD012	AA52
VCCD012	D39
VCCD012	E40
VCCD012	F29
VCCD012	F31
VCCD012	F33
VCCD012	F35
VCCD012	F37
VCCD012	F39
VCCD012	F41
VCCD012	F47
VCCD012	F49
VCCD012	F51
VCCD012	F53
VCCD012	G28
VCCD012	G42
VCCD012	H43
VCCD012	H45
VCCD012	J28
VCCD012	J30
VCCD012	J32
VCCD012	J34
VCCD012	J36
VCCD012	J38
VCCD012	J40
VCCD012	J42

Table 2-1. Lands by Name (Sheet 46 of 94)

Land Name	Land No.
VCCD012	J46
VCCD012	J48
VCCD012	J50
VCCD012	J52
VCCD012	K43
VCCD012	K45
VCCD012	L42
VCCD012	L52
VCCD012	M29
VCCD012	M31
VCCD012	M33
VCCD012	M35
VCCD012	M37
VCCD012	M39
VCCD012	M41
VCCD012	M43
VCCD012	M45
VCCD012	M47
VCCD012	M49
VCCD012	M51
VCCD012	N28
VCCD012	N42
VCCD012	P43
VCCD012	P45
VCCD012	R30
VCCD012	R32
VCCD012	R34
VCCD012	R36
VCCD012	R38
VCCD012	R40
VCCD012	R42
VCCD012	R46
VCCD012	R48
VCCD012	R50
VCCD012	R52
VCCD012	T43
VCCD012	T45
VCCD012	U42
VCCD012	V29

Table 2-1. Lands by Name (Sheet 47 of 94)

Land Name	Land No.
VCCD012	V31
VCCD012	V33
VCCD012	V35
VCCD012	V37
VCCD012	V39
VCCD012	V41
VCCD012	V43
VCCD012	V45
VCCD012	V47
VCCD012	V49
VCCD012	V51
VCCD012	V53
VCCD012	W42
VCCD012	Y43
VCCD012	Y45
VCCD345	DF31
VCCD345	DF33
VCCD345	DF35
VCCD345	DF37
VCCD345	DF39
VCCD345	DF41
VCCD345	DF45
VCCD345	DF47
VCCD345	DF49
VCCD345	DF51
VCCD345	DF53
VCCD345	DG30
VCCD345	DG42
VCCD345	DG44
VCCD345	DH41
VCCD345	DJ30
VCCD345	DJ32
VCCD345	DJ34
VCCD345	DJ36
VCCD345	DJ38
VCCD345	DJ40
VCCD345	DJ42
VCCD345	DJ44
VCCD345	DJ46

Table 2-1. Lands by Name (Sheet 48 of 94)

Land Name	Land No.
VCCD345	DJ48
VCCD345	DJ50
VCCD345	DJ52
VCCD345	DK39
VCCD345	DL42
VCCD345	DL44
VCCD345	DM29
VCCD345	DM31
VCCD345	DM33
VCCD345	DM35
VCCD345	DM37
VCCD345	DM39
VCCD345	DM41
VCCD345	DM45
VCCD345	DM47
VCCD345	DM49
VCCD345	DM51
VCCD345	DM53
VCCD345	DN42
VCCD345	DN44
VCCD345	DP41
VCCD345	DR28
VCCD345	DR30
VCCD345	DR32
VCCD345	DR34
VCCD345	DR36
VCCD345	DR38
VCCD345	DR40
VCCD345	DR42
VCCD345	DR44
VCCD345	DR46
VCCD345	DR48
VCCD345	DR50
VCCD345	DR52
VCCD345	DT39
VCCD345	DU30
VCCD345	DU42
VCCD345	DU44
VCCD345	DV29

Table 2-1. Lands by Name (Sheet 49 of 94)

Land Name	Land No.
VCCD345	DV31
VCCD345	DV33
VCCD345	DV35
VCCD345	DV37
VCCD345	DV39
VCCD345	DV41
VCCD345	DV45
VCCD345	DV47
VCCD345	DV49
VCCD345	DV51
VCCD345	DV53
VCCD345	DW42
VCCD345	DW44
VCCD345	DY41
VCCD345	EA28
VCCD345	EA30
VCCD345	EA32
VCCD345	EA34
VCCD345	EA36
VCCD345	EA38
VCCD345	EA40
VCCD345	EA46
VCCD345	EA48
VCCD345	EA50
VCCD345	EA52
VCCD345	EA54
VCCD345	EB39
VCCD345	EC28
VCCD345	EC38
VCCDDRIO012	AB35
VCCDDRIO012	AB37
VCCDDRIO012	AB39
VCCDDRIO012	AB41
VCCDDRIO012	AB45
VCCDDRIO012	AB47
VCCDDRIO012	AB49
VCCDDRIO012	AB51
VCCDDRIO012	AB53
VCCDDRIO012	AC36

Table 2-1. Lands by Name (Sheet 50 of 94)

Land Name	Land No.
VCCDDRIO012	AC38
VCCDDRIO012	AC40
VCCDDRIO012	AC42
VCCDDRIO345	DD35
VCCDDRIO345	DD37
VCCDDRIO345	DD39
VCCDDRIO345	DD41
VCCDDRIO345	DD45
VCCDDRIO345	DD47
VCCDDRIO345	DD49
VCCDDRIO345	DE32
VCCDDRIO345	DE34
VCCDDRIO345	DE36
VCCDDRIO345	DE38
VCCDDRIO345	DE40
VCCDDRIO345	DE44
VCCDDRIO345	DE46
VCCDDRIO345	DE48
VCCDDRIO345	DE50
VCCDDRIO345	DE52
VCCE_1P0	BE66
VCCE_1P0	BD65
VCCE_1P0	BC66
VCCE_1P0	BB65
VCCE_1P0	BA66
VCCE_1P0	BG68
VCCE_1P0	BE68
VCCH_1P8	CC66
VCCH_1P8	CB65
VCCH_2P5	BA68
VCCH_2P5	AW68
VCCIIO	CR54
VCCIIO	CT53
VCCIIO	CU52
VCCIIO	CU54
VCCIIO	CV51
VCCIIO	CV53
VCCIIO	CW52
VCCLVR	DA52

Table 2-1. Lands by Name (Sheet 51 of 94)

Land Name	Land No.
VCCLVR	DB51
VCCLVR	DB53
VCCLVR	DC52
VCCMF	AP63
VCCMF	AP7
VCCMF	AR8
VCCMF	AT63
VCCMF	CJ10
VCCMF	CK11
VCCMF	CV55
VCCMF	CW54
VCCMH01	AV67
VCCMH01	AU68
VCCMH23	CW66
VCCMH23	CV67
VCCMH45	CR18
VCCMH45	CN18
VCCMH67	AR12
VCCMH67	AR10
VCCMIO0123	AP73
VCCMIO0123	AR72
VCCMIO0123	AR74
VCCMIO0123	AT71
VCCMIO0123	AT73
VCCMIO0123	CN68
VCCMIO0123	CP69
VCCMIO0123	CR68
VCCMIO0123	CT69
VCCMIO0123	CU68
VCCMIO4567	AK19
VCCMIO4567	AL18
VCCMIO4567	AN18
VCCMIO4567	AP17
VCCMIO4567	AR18
VCCMIO4567	CJ20
VCCMIO4567	CK21
VCCMIO4567	CL20
VCCMIO4567	CL22
VCCMIO4567	CM21

Table 2-1. Lands by Name (Sheet 52 of 94)

Land Name	Land No.
VCCMIOQ0123	AM69
VCCMIOQ0123	AP69
VCCMIOQ0123	AT69
VCCMIOQ0123	CN66
VCCMIOQ0123	CR66
VCCMIOQ0123	CU66
VCCMIOQ4567	AN14
VCCMIOQ4567	AR14
VCCMIOQ4567	AR16
VCCMIOQ4567	CJ16
VCCMIOQ4567	CK17
VCCMIOQ4567	CL18
VCCMLB0123	AK77
VCCMLB0123	AL78
VCCMLB0123	AL82
VCCMLB0123	AM77
VCCMLB0123	AM79
VCCMLB0123	AM81
VCCMLB0123	AN78
VCCMLB0123	AN80
VCCMLB0123	AN82
VCCMLB0123	AP81
VCCMLB0123	AR80
VCCMLB0123	AR82
VCCMLB0123	CP73
VCCMLB0123	CP75
VCCMLB0123	CP77
VCCMLB0123	CP79
VCCMLB0123	CR74
VCCMLB0123	CR76
VCCMLB0123	CR78
VCCMLB0123	CT73
VCCMLB0123	CT75
VCCMLB0123	CT77
VCCMLB0123	CT79
VCCMLB0123	CU74
VCCMLB0123_SENSE	CV73
VCCMLB4567	AJ10
VCCMLB4567	AJ14

Table 2-1. Lands by Name (Sheet 53 of 94)

Land Name	Land No.
VCCMLB4567	AK11
VCCMLB4567	AK13
VCCMLB4567	AL10
VCCMLB4567	AL12
VCCMLB4567	AL14
VCCMLB4567	AM11
VCCMLB4567	AM13
VCCMLB4567	AM9
VCCMLB4567	AN10
VCCMLB4567	AN12
VCCMLB4567	CK13
VCCMLB4567	CL14
VCCMLB4567	CM13
VCCMLB4567	CM15
VCCMLB4567	CN12
VCCMLB4567	CN14
VCCMLB4567	CP11
VCCMLB4567	CP13
VCCMLB4567	CR12
VCCMLB4567	CR14
VCCMLB4567	CT11
VCCMLB4567	CT13
VCCMLB4567_SENSE	AL8
VCCMP0123	AH85
VCCMP0123	AJ84
VCCMP0123	AJ86
VCCMP0123	AK85
VCCMP0123	AL84
VCCMP0123	AL86
VCCMP0123	AM85
VCCMP0123	AN84
VCCMP0123	AN86
VCCMP0123	AP85
VCCMP0123	AR84
VCCMP0123	AR86
VCCMP0123	CR82
VCCMP0123	CR84
VCCMP0123	CR86
VCCMP0123	CT81

Table 2-1. Lands by Name (Sheet 54 of 94)

Land Name	Land No.
VCCMP0123	CT83
VCCMP0123	CT85
VCCMP0123	CU82
VCCMP0123	CU84
VCCMP0123	CU86
VCCMP0123	CV83
VCCMP0123	CV85
VCCMP0123	CW84
VCCMP0123_SENSE	AG86
VCCMP4567	AH1
VCCMP4567	AH3
VCCMP4567	AJ2
VCCMP4567	AJ4
VCCMP4567	AK1
VCCMP4567	AK3
VCCMP4567	AK5
VCCMP4567	AL2
VCCMP4567	AL4
VCCMP4567	AM3
VCCMP4567	AM5
VCCMP4567	AN4
VCCMP4567	CN4
VCCMP4567	CP1
VCCMP4567	CP3
VCCMP4567	CP5
VCCMP4567	CR2
VCCMP4567	CR4
VCCMP4567	CT1
VCCMP4567	CT3
VCCMP4567	CT5
VCCMP4567	CU2
VCCMP4567	CU4
VCCMP4567	CV3
VCCMP4567_SENSE	CR6
VCCMPLL01	AM75
VCCMPLL01	AM73
VCCMPLL23	CW78
VCCMPLL23	CV77
VCCMPLL45	CT9

Table 2-1. Lands by Name (Sheet 55 of 94)

Land Name	Land No.
VCCMPLL45	CP9
VCCMPLL67	AM7
VCCMPLL67	AK7
VCCOPIO01	AK65
VCCOPIO01	AL66
VCCOPIO01	AM65
VCCOPIO01	AM67
VCCOPIO01	AN66
VCCOPIO01	AP65
VCCOPIO01	AP67
VCCOPIO01	AR66
VCCOPIO23	CN64
VCCOPIO23	CP63
VCCOPIO23	CR62
VCCOPIO23	CR64
VCCOPIO23	CT61
VCCOPIO23	CT63
VCCOPIO23	CU62
VCCOPIO23	CU64
VCCOPIO45	CP21
VCCOPIO45	CR20
VCCOPIO45	CR22
VCCOPIO45	CT21
VCCOPIO45	CT23
VCCOPIO45	CU20
VCCOPIO45	CU22
VCCOPIO45	CV21
VCCOPIO67	AL20
VCCOPIO67	AL22
VCCOPIO67	AM21
VCCOPIO67	AN20
VCCOPIO67	AN22
VCCOPIO67	AP21
VCCOPIO67	AR20
VCCOPIO67	AR22
VCCP	CW40
VCCP	CW38
VCCP	CW36
VCCP	CW34

Table 2-1. Lands by Name (Sheet 56 of 94)

Land Name	Land No.
VCCP	CV39
VCCP	CV37
VCCP	CV35
VCCP	CV33
VCCP	CU40
VCCP	CU38
VCCP	CU36
VCCP	CU34
VCCP	CT39
VCCP	CT37
VCCP	CT35
VCCP	CT33
VCCP	CR34
VCCP	CR32
VCCP	CP33
VCCP	CP31
VCCP	CN32
VCCP	CN30
VCCP	CM31
VCCP	CM29
VCCP	CL30
VCCP	CL28
VCCP	CK29
VCCP	CK27
VCCP	CJ28
VCCP	CJ26
VCCP	CH27
VCCP	CG26
VCCP	CF27
VCCP	CE26
VCCP	CB27
VCCP	CB25
VCCP	CB23
VCCP	CB21
VCCP	CB19
VCCP	CB17
VCCP	CB15
VCCP	CB13
VCCP	CB11

Table 2-1. Lands by Name (Sheet 57 of 94)

Land Name	Land No.
VCCP	CB9
VCCP	CB7
VCCP	CB5
VCCP	CB3
VCCP	CA26
VCCP	CA24
VCCP	CA22
VCCP	CA20
VCCP	CA18
VCCP	CA16
VCCP	CA14
VCCP	CA12
VCCP	CA10
VCCP	CA8
VCCP	CA6
VCCP	CA4
VCCP	CA2
VCCP	BY27
VCCP	BY25
VCCP	BY23
VCCP	BY21
VCCP	BY19
VCCP	BY17
VCCP	BY15
VCCP	BY13
VCCP	BY11
VCCP	BY9
VCCP	BY7
VCCP	BY5
VCCP	BY3
VCCP	BW26
VCCP	BW24
VCCP	BW22
VCCP	BW20
VCCP	BW18
VCCP	BW16
VCCP	BW14
VCCP	BW12
VCCP	BW10

Table 2-1. Lands by Name (Sheet 58 of 94)

Land Name	Land No.
VCCP	BW8
VCCP	BW6
VCCP	BW4
VCCP	BV27
VCCP	BV25
VCCP	BV23
VCCP	BV21
VCCP	BV19
VCCP	BV17
VCCP	BV15
VCCP	BV13
VCCP	BV11
VCCP	BV9
VCCP	BV7
VCCP	BV5
VCCP	BV3
VCCP	BT3
VCCP	BR26
VCCP	BR24
VCCP	BR22
VCCP	BR20
VCCP	BR18
VCCP	BR16
VCCP	BR14
VCCP	BR12
VCCP	BR10
VCCP	BR8
VCCP	BR6
VCCP	BR4
VCCP	BP27
VCCP	BP25
VCCP	BP23
VCCP	BP21
VCCP	BP19
VCCP	BP17
VCCP	BP15
VCCP	BP13
VCCP	BP11
VCCP	BP9

Table 2-1. Lands by Name (Sheet 59 of 94)

Land Name	Land No.
VCCP	BP7
VCCP	BP5
VCCP	BP3
VCCP	BN26
VCCP	BN24
VCCP	BN22
VCCP	BN20
VCCP	BN18
VCCP	BN16
VCCP	BN14
VCCP	BN12
VCCP	BN10
VCCP	BN8
VCCP	BN6
VCCP	BN4
VCCP	BM27
VCCP	BM25
VCCP	BM23
VCCP	BM21
VCCP	BM19
VCCP	BM17
VCCP	BM15
VCCP	BM13
VCCP	BM11
VCCP	BM9
VCCP	BM7
VCCP	BM5
VCCP	BM3
VCCP	BK3
VCCP	BJ26
VCCP	BJ24
VCCP	BJ22
VCCP	BJ20
VCCP	BJ18
VCCP	BJ16
VCCP	BJ14
VCCP	BJ12
VCCP	BJ10
VCCP	BJ8

Table 2-1. Lands by Name (Sheet 60 of 94)

Land Name	Land No.
VCCP	BJ6
VCCP	BJ4
VCCP	BH27
VCCP	BH25
VCCP	BH23
VCCP	BH21
VCCP	BH19
VCCP	BH17
VCCP	BH15
VCCP	BH13
VCCP	BH11
VCCP	BH9
VCCP	BH7
VCCP	BH5
VCCP	BH3
VCCP	BG26
VCCP	BG24
VCCP	BG22
VCCP	BG20
VCCP	BG18
VCCP	BG16
VCCP	BG14
VCCP	BG12
VCCP	BG10
VCCP	BG8
VCCP	BG6
VCCP	BG4
VCCP	BF27
VCCP	BF25
VCCP	BF23
VCCP	BF21
VCCP	BF19
VCCP	BF17
VCCP	BF15
VCCP	BF13
VCCP	BF11
VCCP	BF9
VCCP	BF7
VCCP	BF5

Table 2-1. Lands by Name (Sheet 61 of 94)

Land Name	Land No.
VCCP	BF3
VCCP	BC26
VCCP	BC24
VCCP	BC22
VCCP	BC20
VCCP	BC18
VCCP	BC16
VCCP	BC14
VCCP	BC12
VCCP	BC10
VCCP	BC8
VCCP	BC6
VCCP	BC4
VCCP	BC2
VCCP	BB27
VCCP	BB25
VCCP	BB23
VCCP	BB21
VCCP	BB19
VCCP	BB17
VCCP	BB15
VCCP	BB13
VCCP	BB11
VCCP	BB9
VCCP	BB7
VCCP	BB5
VCCP	BB3
VCCP	BA26
VCCP	BA24
VCCP	BA22
VCCP	BA20
VCCP	BA18
VCCP	BA16
VCCP	BA14
VCCP	BA12
VCCP	BA10
VCCP	BA8
VCCP	BA6
VCCP	BA4

Table 2-1. Lands by Name (Sheet 62 of 94)

Land Name	Land No.
VCCP	BA2
VCCP	AY27
VCCP	AY25
VCCP	AY23
VCCP	AY21
VCCP	AY19
VCCP	AY17
VCCP	AY15
VCCP	AY13
VCCP	AY11
VCCP	AY9
VCCP	AY7
VCCP	AY5
VCCP	AY3
VCCP	AW26
VCCP	AW24
VCCP	AW22
VCCP	AW20
VCCP	AW18
VCCP	AW16
VCCP	AW14
VCCP	AW12
VCCP	AW10
VCCP	AW8
VCCP	AW6
VCCP	AW4
VCCP	AW2
VCCP	AV27
VCCP	AV25
VCCP	AV23
VCCP	AV21
VCCP	AV19
VCCP	AV17
VCCP	AV15
VCCP	AV13
VCCP	AV11
VCCP	AV9
VCCP	AV7
VCCP	AV5

Table 2-1. Lands by Name (Sheet 63 of 94)

Land Name	Land No.
VCCP	AV3
VCCP	AU28
VCCP	AT29
VCCP	AR30
VCCP	AP31
VCCP	AN32
VCCP	AM33
VCCP	AM31
VCCP	AL34
VCCP	AL32
VCCP	AK35
VCCP	AK33
VCCP	AK31
VCCP	AJ36
VCCP	AJ34
VCCP	AJ32
VCCP	AH41
VCCP	AH39
VCCP	AH37
VCCP	AH35
VCCP	AH33
VCCP	AG42
VCCP	AG40
VCCP	AG38
VCCP	AG36
VCCP	AG34
VCCP_1P0	CL60
VCCP_1P0	CL62
VCCP_1P0	CL64
VCCP_1P0	CM61
VCCP_1P0	CM63
VCCP_1P0	CN60
VCCP_SENSE	AV1
VCCPIO	CL58
VCCPIO	CM57
VCCPIO	CM59
VCCPIO	CN56
VCCPIO	CN58
VCCPIO	CP57

Table 2-1. Lands by Name (Sheet 64 of 94)

Land Name	Land No.
VCCPIO	CP59
VCCPIO	CR56
VCCPIO	CR58
VCCPIO	CR60
VCCPIO	CT57
VCCPIO	CT59
VCCPIO	CU58
VCCPIO_SENSE	CV59
VCCU	CH1
VCCU	CJ2
VCCU	CK1
VCCU	CW42
VCCU	CV41
VCCU	AG30
VCCU	AH29
VCCU	AK29
VCCU	AL28
VCCU	AM29
VCCU	AN28
VCCU	DA36
VCCU	DA38
VCCU	DA40
VCCU_SENSE	AP29
VSS	EC84
VSS	EC80
VSS	EC46
VSS	EC40
VSS	EB81
VSS	EB75
VSS	EB71
VSS	EB63
VSS	EB57
VSS	EB55
VSS	EB45
VSS	EB41
VSS	EB11
VSS	EB5
VSS	EA84
VSS	EA82

Table 2-1. Lands by Name (Sheet 65 of 94)

Land Name	Land No.
VSS	EA80
VSS	EA76
VSS	EA74
VSS	EA72
VSS	EA70
VSS	EA62
VSS	EA58
VSS	EA56
VSS	EA44
VSS	EA42
VSS	EA16
VSS	EA14
VSS	EA12
VSS	EA8
VSS	EA6
VSS	DY83
VSS	DY79
VSS	DY77
VSS	DY73
VSS	DY71
VSS	DY61
VSS	DY59
VSS	DY55
VSS	DY25
VSS	DY15
VSS	DY13
VSS	DY11
VSS	DY9
VSS	DY7
VSS	DY5
VSS	DY3
VSS	DW84
VSS	DW78
VSS	DW72
VSS	DW66
VSS	DW60
VSS	DW54
VSS	DW26
VSS	DW14

Table 2-1. Lands by Name (Sheet 66 of 94)

Land Name	Land No.
VSS	DW10
VSS	DW8
VSS	DW4
VSS	DV27
VSS	DV21
VSS	DV15
VSS	DV9
VSS	DV3
VSS	DU84
VSS	DU82
VSS	DU80
VSS	DU78
VSS	DU76
VSS	DU74
VSS	DU72
VSS	DU70
VSS	DU68
VSS	DU66
VSS	DU64
VSS	DU62
VSS	DU60
VSS	DU58
VSS	DU56
VSS	DU54
VSS	DT85
VSS	DT27
VSS	DT25
VSS	DT23
VSS	DT21
VSS	DT19
VSS	DT17
VSS	DT15
VSS	DT13
VSS	DT11
VSS	DT9
VSS	DT7
VSS	DT5
VSS	DT3
VSS	DR84

Table 2-1. Lands by Name (Sheet 67 of 94)

Land Name	Land No.
VSS	DR78
VSS	DR72
VSS	DR66
VSS	DR60
VSS	DR54
VSS	DR2
VSS	DP83
VSS	DP79
VSS	DP77
VSS	DP73
VSS	DP71
VSS	DP67
VSS	DP65
VSS	DP61
VSS	DP59
VSS	DP55
VSS	DP27
VSS	DP21
VSS	DP15
VSS	DP9
VSS	DP3
VSS	DN82
VSS	DN80
VSS	DN76
VSS	DN74
VSS	DN70
VSS	DN68
VSS	DN64
VSS	DN62
VSS	DN58
VSS	DN56
VSS	DN26
VSS	DN22
VSS	DN20
VSS	DN16
VSS	DN14
VSS	DN10
VSS	DN8
VSS	DN4

Table 2-1. Lands by Name (Sheet 68 of 94)

Land Name	Land No.
VSS	DM81
VSS	DM75
VSS	DM69
VSS	DM63
VSS	DM57
VSS	DM25
VSS	DM23
VSS	DM19
VSS	DM17
VSS	DM13
VSS	DM11
VSS	DM7
VSS	DM5
VSS	DL56
VSS	DL24
VSS	DL18
VSS	DL12
VSS	DL6
VSS	DK85
VSS	DK83
VSS	DK81
VSS	DK79
VSS	DK77
VSS	DK75
VSS	DK73
VSS	DK71
VSS	DK69
VSS	DK67
VSS	DK65
VSS	DK63
VSS	DK61
VSS	DK59
VSS	DK57
VSS	DJ56
VSS	DJ54
VSS	DJ24
VSS	DJ22
VSS	DJ20
VSS	DJ18

Table 2-1. Lands by Name (Sheet 69 of 94)

Land Name	Land No.
VSS	DJ16
VSS	DJ14
VSS	DJ12
VSS	DJ10
VSS	DJ8
VSS	DJ6
VSS	DJ4
VSS	DJ2
VSS	DH81
VSS	DH75
VSS	DH69
VSS	DH63
VSS	DH57
VSS	DG82
VSS	DG80
VSS	DG76
VSS	DG74
VSS	DG70
VSS	DG68
VSS	DG64
VSS	DG62
VSS	DG58
VSS	DG56
VSS	DG24
VSS	DG18
VSS	DG12
VSS	DG6
VSS	DF83
VSS	DF79
VSS	DF77
VSS	DF73
VSS	DF71
VSS	DF67
VSS	DF65
VSS	DF61
VSS	DF59
VSS	DF55
VSS	DF27
VSS	DF25

Table 2-1. Lands by Name (Sheet 70 of 94)

Land Name	Land No.
VSS	DF23
VSS	DF19
VSS	DF17
VSS	DF13
VSS	DF11
VSS	DF7
VSS	DF5
VSS	DE84
VSS	DE78
VSS	DE72
VSS	DE66
VSS	DE60
VSS	DE54
VSS	DE42
VSS	DE30
VSS	DE26
VSS	DE22
VSS	DE20
VSS	DE16
VSS	DE14
VSS	DE10
VSS	DE8
VSS	DE4
VSS	DD85
VSS	DD53
VSS	DD51
VSS	DD33
VSS	DD31
VSS	DD29
VSS	DD27
VSS	DD21
VSS	DD15
VSS	DD9
VSS	DD3
VSS	DC84
VSS	DC82
VSS	DC80
VSS	DC78
VSS	DC76

Table 2-1. Lands by Name (Sheet 71 of 94)

Land Name	Land No.
VSS	DC74
VSS	DC72
VSS	DC70
VSS	DC68
VSS	DC66
VSS	DC64
VSS	DC62
VSS	DC60
VSS	DC58
VSS	DC56
VSS	DC54
VSS	DC50
VSS	DC48
VSS	DC46
VSS	DC44
VSS	DC42
VSS	DC40
VSS	DC38
VSS	DC36
VSS	DC34
VSS	DC2
VSS	DB85
VSS	DB41
VSS	DB39
VSS	DB37
VSS	DB35
VSS	DB27
VSS	DB25
VSS	DB23
VSS	DB21
VSS	DB19
VSS	DB17
VSS	DB15
VSS	DB13
VSS	DB11
VSS	DB9
VSS	DB7
VSS	DB5
VSS	DB3

Table 2-1. Lands by Name (Sheet 72 of 94)

Land Name	Land No.
VSS	DA84
VSS	DA78
VSS	DA72
VSS	DA66
VSS	DA60
VSS	DA54
VSS	DA50
VSS	DA44
VSS	DA42
VSS	DA34
VSS	CY85
VSS	CY83
VSS	CY79
VSS	CY77
VSS	CY73
VSS	CY71
VSS	CY67
VSS	CY65
VSS	CY61
VSS	CY59
VSS	CY55
VSS	CY53
VSS	CY51
VSS	CY45
VSS	CY41
VSS	CY39
VSS	CY37
VSS	CY35
VSS	CY33
VSS	CY27
VSS	CY21
VSS	CY15
VSS	CY9
VSS	CY3
VSS	CW86
VSS	CW82
VSS	CW80
VSS	CW76
VSS	CW74

Table 2-1. Lands by Name (Sheet 73 of 94)

Land Name	Land No.
VSS	CW68
VSS	CW64
VSS	CW62
VSS	CW58
VSS	CW56
VSS	CW50
VSS	CW48
VSS	CW46
VSS	CW32
VSS	CW30
VSS	CW28
VSS	CW26
VSS	CW22
VSS	CW20
VSS	CW16
VSS	CW14
VSS	CW10
VSS	CW8
VSS	CW4
VSS	CW2
VSS	CV81
VSS	CV79
VSS	CV75
VSS	CV69
VSS	CV65
VSS	CV63
VSS	CV61
VSS	CV57
VSS	CV25
VSS	CV23
VSS	CV19
VSS	CV17
VSS	CV13
VSS	CV11
VSS	CV9
VSS	CV7
VSS	CV5
VSS	CV1
VSS	CU80

Table 2-1. Lands by Name (Sheet 74 of 94)

Land Name	Land No.
VSS	CU78
VSS	CU76
VSS	CU60
VSS	CU56
VSS	CU32
VSS	CU28
VSS	CU26
VSS	CU24
VSS	CU18
VSS	CU14
VSS	CU12
VSS	CU10
VSS	CU8
VSS	CU6
VSS	CT67
VSS	CT65
VSS	CT55
VSS	CT31
VSS	CT19
VSS	CT7
VSS	CR80
VSS	CR30
VSS	CR28
VSS	CR26
VSS	CR10
VSS	CR8
VSS	CP85
VSS	CP83
VSS	CP81
VSS	CP67
VSS	CP65
VSS	CP61
VSS	CP55
VSS	CP23
VSS	CP19
VSS	CN86
VSS	CN84
VSS	CN82
VSS	CN80

Table 2-1. Lands by Name (Sheet 75 of 94)

Land Name	Land No.
VSS	CN78
VSS	CN76
VSS	CN74
VSS	CN70
VSS	CN62
VSS	CN22
VSS	CN20
VSS	CN10
VSS	CN8
VSS	CN6
VSS	CN2
VSS	CM85
VSS	CM83
VSS	CM81
VSS	CM79
VSS	CM77
VSS	CM75
VSS	CM73
VSS	CM71
VSS	CM69
VSS	CM65
VSS	CM27
VSS	CM19
VSS	CM11
VSS	CM7
VSS	CM5
VSS	CM3
VSS	CM1
VSS	CL68
VSS	CL26
VSS	CL16
VSS	CL12
VSS	CL10
VSS	CK85
VSS	CK65
VSS	CK63
VSS	CK61
VSS	CK59
VSS	CK25

Table 2-1. Lands by Name (Sheet 76 of 94)

Land Name	Land No.
VSS	CK19
VSS	CK15
VSS	CJ68
VSS	CJ60
VSS	CJ24
VSS	CJ22
VSS	CJ18
VSS	CJ14
VSS	CJ12
VSS	CH85
VSS	CH65
VSS	CH25
VSS	CH23
VSS	CH21
VSS	CH19
VSS	CH17
VSS	CH15
VSS	CH11
VSS	CH9
VSS	CH7
VSS	CG84
VSS	CG82
VSS	CG80
VSS	CG78
VSS	CG76
VSS	CG74
VSS	CG72
VSS	CG70
VSS	CG68
VSS	CF85
VSS	CF83
VSS	CF81
VSS	CF79
VSS	CF77
VSS	CF75
VSS	CF73
VSS	CF71
VSS	CF69
VSS	CF65

Table 2-1. Lands by Name (Sheet 77 of 94)

Land Name	Land No.
VSS	CF25
VSS	CF19
VSS	CE68
VSS	CE62
VSS	CD85
VSS	CD67
VSS	CD65
VSS	CD27
VSS	CD25
VSS	CD23
VSS	CD21
VSS	CD19
VSS	CD17
VSS	CD15
VSS	CD13
VSS	CD11
VSS	CD9
VSS	CD7
VSS	CD5
VSS	CD3
VSS	CC68
VSS	CC64
VSS	CC60
VSS	CC26
VSS	CC24
VSS	CC22
VSS	CC20
VSS	CC18
VSS	CC16
VSS	CC14
VSS	CC12
VSS	CC10
VSS	CC8
VSS	CC6
VSS	CC4
VSS	CC2
VSS	CB67
VSS	CA84
VSS	CA82

Table 2-1. Lands by Name (Sheet 78 of 94)

Land Name	Land No.
VSS	CA80
VSS	CA78
VSS	CA76
VSS	CA74
VSS	CA72
VSS	CA70
VSS	CA68
VSS	BY83
VSS	BY81
VSS	BY79
VSS	BY77
VSS	BY75
VSS	BY73
VSS	BY71
VSS	BY69
VSS	BY65
VSS	BY63
VSS	BW68
VSS	BU68
VSS	BU64
VSS	BU60
VSS	BU26
VSS	BU24
VSS	BU22
VSS	BU20
VSS	BU18
VSS	BU16
VSS	BU14
VSS	BU12
VSS	BU10
VSS	BU8
VSS	BU6
VSS	BU4
VSS	BT63
VSS	BT27
VSS	BT25
VSS	BT23
VSS	BT21
VSS	BT19

Table 2-1. Lands by Name (Sheet 79 of 94)

Land Name	Land No.
VSS	BT17
VSS	BT15
VSS	BT13
VSS	BT11
VSS	BT9
VSS	BT7
VSS	BT5
VSS	BR84
VSS	BR82
VSS	BR80
VSS	BR78
VSS	BR76
VSS	BR74
VSS	BR72
VSS	BR70
VSS	BR68
VSS	BP83
VSS	BP81
VSS	BP79
VSS	BP77
VSS	BP75
VSS	BP73
VSS	BP71
VSS	BP69
VSS	BP67
VSS	BP65
VSS	BM67
VSS	BM63
VSS	BL84
VSS	BL64
VSS	BL60
VSS	BL26
VSS	BL24
VSS	BL22
VSS	BL20
VSS	BL18
VSS	BL16
VSS	BL14
VSS	BL12

Table 2-1. Lands by Name (Sheet 80 of 94)

Land Name	Land No.
VSS	BL10
VSS	BL8
VSS	BL6
VSS	BL4
VSS	BK67
VSS	BK27
VSS	BK25
VSS	BK23
VSS	BK21
VSS	BK19
VSS	BK17
VSS	BK15
VSS	BK13
VSS	BK11
VSS	BK9
VSS	BK7
VSS	BK5
VSS	BJ82
VSS	BJ80
VSS	BJ78
VSS	BJ76
VSS	BJ74
VSS	BJ72
VSS	BJ70
VSS	BJ68
VSS	BH83
VSS	BH81
VSS	BH79
VSS	BH77
VSS	BH75
VSS	BH73
VSS	BH71
VSS	BH65
VSS	BG76
VSS	BF77
VSS	BF63
VSS	BE76
VSS	BE70
VSS	BE64

Table 2-1. Lands by Name (Sheet 81 of 94)

Land Name	Land No.
VSS	BE60
VSS	BE26
VSS	BE24
VSS	BE22
VSS	BE20
VSS	BE18
VSS	BE16
VSS	BE14
VSS	BE12
VSS	BE10
VSS	BE8
VSS	BE6
VSS	BE4
VSS	BD77
VSS	BD71
VSS	BD27
VSS	BD25
VSS	BD23
VSS	BD21
VSS	BD19
VSS	BD17
VSS	BD15
VSS	BD13
VSS	BD11
VSS	BD9
VSS	BD7
VSS	BD5
VSS	BD3
VSS	BC84
VSS	BC82
VSS	BC80
VSS	BC78
VSS	BC76
VSS	BC74
VSS	BC72
VSS	BC68
VSS	BC64
VSS	BB85
VSS	BB83

Table 2-1. Lands by Name (Sheet 82 of 94)

Land Name	Land No.
VSS	BB81
VSS	BB79
VSS	BB77
VSS	BB75
VSS	BB73
VSS	BB71
VSS	BB69
VSS	BA78
VSS	BA72
VSS	BA64
VSS	BA60
VSS	AY77
VSS	AY71
VSS	AY69
VSS	AW78
VSS	AW72
VSS	AW60
VSS	AV77
VSS	AV71
VSS	AV69
VSS	AV63
VSS	AU86
VSS	AU84
VSS	AU82
VSS	AU80
VSS	AU78
VSS	AU76
VSS	AU74
VSS	AU72
VSS	AU70
VSS	AU66
VSS	AU26
VSS	AU24
VSS	AU22
VSS	AU20
VSS	AU18
VSS	AU16
VSS	AU14
VSS	AU12

Table 2-1. Lands by Name (Sheet 83 of 94)

Land Name	Land No.
VSS	AU10
VSS	AU8
VSS	AU6
VSS	AU4
VSS	AT85
VSS	AT83
VSS	AT81
VSS	AT79
VSS	AT67
VSS	AT65
VSS	AT27
VSS	AT25
VSS	AT23
VSS	AT21
VSS	AT19
VSS	AT17
VSS	AT15
VSS	AT13
VSS	AT11
VSS	AT9
VSS	AT7
VSS	AT5
VSS	AT3
VSS	AT1
VSS	AR68
VSS	AR62
VSS	AR58
VSS	AP83
VSS	AP79
VSS	AP77
VSS	AP75
VSS	AP61
VSS	AP23
VSS	AP19
VSS	AP13
VSS	AP11
VSS	AP9
VSS	AN76
VSS	AN74

Table 2-1. Lands by Name (Sheet 84 of 94)

Land Name	Land No.
VSS	AN68
VSS	AN60
VSS	AN30
VSS	AN8
VSS	AN6
VSS	AN2
VSS	AM83
VSS	AM59
VSS	AM55
VSS	AM27
VSS	AM23
VSS	AM19
VSS	AM1
VSS	AL80
VSS	AL76
VSS	AL74
VSS	AL68
VSS	AL64
VSS	AL62
VSS	AL56
VSS	AL30
VSS	AL26
VSS	AL6
VSS	AK83
VSS	AK81
VSS	AK79
VSS	AK75
VSS	AK73
VSS	AK69
VSS	AK67
VSS	AK63
VSS	AK61
VSS	AK57
VSS	AK55
VSS	AK21
VSS	AJ82
VSS	AJ78
VSS	AJ76
VSS	AJ70

Table 2-1. Lands by Name (Sheet 85 of 94)

Land Name	Land No.
VSS	AJ66
VSS	AJ64
VSS	AJ60
VSS	AJ58
VSS	AJ54
VSS	AJ52
VSS	AJ30
VSS	AJ28
VSS	AJ24
VSS	AJ20
VSS	AJ18
VSS	AJ12
VSS	AJ8
VSS	AJ6
VSS	AH83
VSS	AH77
VSS	AH71
VSS	AH65
VSS	AH59
VSS	AH53
VSS	AH31
VSS	AH25
VSS	AH23
VSS	AH19
VSS	AH15
VSS	AH13
VSS	AH11
VSS	AH9
VSS	AH7
VSS	AH5
VSS	AG84
VSS	AG52
VSS	AG32
VSS	AG28
VSS	AG26
VSS	AG22
VSS	AG20
VSS	AG16
VSS	AG14

Table 2-1. Lands by Name (Sheet 86 of 94)

Land Name	Land No.
VSS	AG10
VSS	AG8
VSS	AG4
VSS	AF83
VSS	AF81
VSS	AF79
VSS	AF77
VSS	AF75
VSS	AF73
VSS	AF71
VSS	AF69
VSS	AF67
VSS	AF65
VSS	AF63
VSS	AF61
VSS	AF59
VSS	AF57
VSS	AF55
VSS	AF53
VSS	AF43
VSS	AF41
VSS	AF39
VSS	AF37
VSS	AF35
VSS	AF33
VSS	AF31
VSS	AF29
VSS	AF27
VSS	AF21
VSS	AF15
VSS	AF9
VSS	AF3
VSS	AE52
VSS	AE34
VSS	AE30
VSS	AE28
VSS	AD83
VSS	AD77
VSS	AD71

Table 2-1. Lands by Name (Sheet 87 of 94)

Land Name	Land No.
VSS	AD65
VSS	AD59
VSS	AD53
VSS	AD51
VSS	AD43
VSS	AD41
VSS	AD39
VSS	AD37
VSS	AD35
VSS	AD29
VSS	AD27
VSS	AD25
VSS	AD23
VSS	AD21
VSS	AD19
VSS	AD17
VSS	AD15
VSS	AD13
VSS	AD11
VSS	AD9
VSS	AD7
VSS	AD5
VSS	AD3
VSS	AC84
VSS	AC82
VSS	AC78
VSS	AC76
VSS	AC72
VSS	AC70
VSS	AC66
VSS	AC64
VSS	AC60
VSS	AC58
VSS	AC54
VSS	AC52
VSS	AC50
VSS	AC48
VSS	AC46
VSS	AC32

Table 2-1. Lands by Name (Sheet 88 of 94)

Land Name	Land No.
VSS	AC30
VSS	AC28
VSS	AB85
VSS	AB81
VSS	AB79
VSS	AB75
VSS	AB73
VSS	AB69
VSS	AB67
VSS	AB63
VSS	AB61
VSS	AB57
VSS	AB55
VSS	AB43
VSS	AB31
VSS	AB29
VSS	AB27
VSS	AB21
VSS	AB15
VSS	AB9
VSS	AB3
VSS	AA86
VSS	AA80
VSS	AA74
VSS	AA68
VSS	AA62
VSS	AA56
VSS	AA28
VSS	AA26
VSS	AA22
VSS	AA20
VSS	AA16
VSS	AA14
VSS	AA10
VSS	AA8
VSS	AA4
VSS	AA2
VSS	Y27
VSS	Y25

Table 2-1. Lands by Name (Sheet 89 of 94)

Land Name	Land No.
VSS	Y23
VSS	Y19
VSS	Y17
VSS	Y13
VSS	Y11
VSS	Y7
VSS	Y5
VSS	Y1
VSS	W86
VSS	W84
VSS	W82
VSS	W80
VSS	W78
VSS	W76
VSS	W74
VSS	W72
VSS	W70
VSS	W68
VSS	W66
VSS	W64
VSS	W62
VSS	W60
VSS	W58
VSS	W56
VSS	W28
VSS	W26
VSS	W24
VSS	W18
VSS	W12
VSS	W6
VSS	V25
VSS	U86
VSS	U80
VSS	U74
VSS	U68
VSS	U62
VSS	U56
VSS	U28
VSS	U24

Table 2-1. Lands by Name (Sheet 90 of 94)

Land Name	Land No.
VSS	U22
VSS	U20
VSS	U18
VSS	U16
VSS	U14
VSS	U12
VSS	U10
VSS	U8
VSS	U6
VSS	U4
VSS	U2
VSS	T85
VSS	T81
VSS	T79
VSS	T75
VSS	T73
VSS	T69
VSS	T67
VSS	T63
VSS	T61
VSS	T57
VSS	T55
VSS	T25
VSS	R84
VSS	R82
VSS	R78
VSS	R76
VSS	R72
VSS	R70
VSS	R66
VSS	R64
VSS	R60
VSS	R58
VSS	R54
VSS	R28
VSS	R24
VSS	R18
VSS	R12
VSS	R6

Table 2-1. Lands by Name (Sheet 91 of 94)

Land Name	Land No.
VSS	P83
VSS	P77
VSS	P71
VSS	P65
VSS	P59
VSS	P53
VSS	P25
VSS	P23
VSS	P19
VSS	P17
VSS	P13
VSS	P11
VSS	P7
VSS	P5
VSS	P1
VSS	N26
VSS	N22
VSS	N20
VSS	N16
VSS	N14
VSS	N10
VSS	N8
VSS	N4
VSS	N2
VSS	M83
VSS	M81
VSS	M79
VSS	M77
VSS	M75
VSS	M73
VSS	M71
VSS	M69
VSS	M67
VSS	M65
VSS	M63
VSS	M61
VSS	M59
VSS	M57
VSS	M55

Table 2-1. Lands by Name (Sheet 92 of 94)

Land Name	Land No.
VSS	M53
VSS	M27
VSS	M21
VSS	M15
VSS	M9
VSS	M3
VSS	K85
VSS	K83
VSS	K77
VSS	K71
VSS	K65
VSS	K59
VSS	K53
VSS	K27
VSS	K25
VSS	K23
VSS	K21
VSS	K19
VSS	K17
VSS	K15
VSS	K13
VSS	K11
VSS	K9
VSS	K7
VSS	K5
VSS	K3
VSS	J82
VSS	J78
VSS	J76
VSS	J72
VSS	J70
VSS	J66
VSS	J64
VSS	J60
VSS	J58
VSS	J54
VSS	J2
VSS	H85
VSS	H83

Table 2-1. Lands by Name (Sheet 93 of 94)

Land Name	Land No.
VSS	H81
VSS	H79
VSS	H75
VSS	H73
VSS	H63
VSS	H61
VSS	H57
VSS	H55
VSS	H27
VSS	H21
VSS	H15
VSS	H9
VSS	H3
VSS	G84
VSS	G80
VSS	G74
VSS	G62
VSS	G56
VSS	G54
VSS	G26
VSS	G16
VSS	G14
VSS	G10
VSS	G8
VSS	G4
VSS	F83
VSS	F81
VSS	F79
VSS	F77
VSS	F75
VSS	F73
VSS	F71
VSS	F45
VSS	F43
VSS	F27
VSS	F25
VSS	F17
VSS	F13
VSS	F11

Table 2-1. Lands by Name (Sheet 94 of 94)

Land Name	Land No.
VSS	F7
VSS	F5
VSS	F3
VSS	E82
VSS	E80
VSS	E78
VSS	E76
VSS	E74
VSS	E72
VSS	E54
VSS	E46
VSS	E42
VSS	E24
VSS	E12
VSS	E6
VSS	E2
VSS	D47
VSS	D41
VSS	BG66
VSS	BF67
VSS	BF65
VSS	BD67
VSS	BB67
VSS	AY67
VSS	AY65
VSS	AW66
VSS_VCC_CDCORE_SENSE	BY67
VSS_VCCCLR_SENSE	AL58
VSS_VCCMLB0123_SENSE	CW72
VSS_VCCMLB4567_SENSE	AK9
VSS_VCCMP0123_SENSE	AF85
VSS_VCCMP4567_SENSE	CP7
VSS_VCCP_SENSE	AU2
VSS_VCCPIO_SENSE	CW60
VSS_VCCU_SENSE	AR28

Table 2-2. Lands by Number (Sheet 1 of 94)

Land No.	Land Name
A10	RSVD
A12	RSVD
A14	RSVD
A16	RSVD
A24	RSVD
A26	RSVD
A28	RSVD
A30	RSVD
A32	RSVD
A34	RSVD
A36	RSVD
A38	RSVD
A4	RSVD
A40	RSVD
A42	RSVD
A6	RSVD
A8	RSVD
AA10	VSS
AA12	DDR0_DQS_DN[15]
AA14	VSS
AA16	VSS
AA18	DDR0_DQS_DP[14]
AA2	VSS
AA20	VSS
AA22	VSS
AA24	DDR0_DQS_DN[13]
AA26	VSS
AA28	VSS
AA30	VCCD012
AA32	VCCD012
AA34	VCCD012
AA36	VCCD012
AA38	VCCD012
AA4	VSS
AA40	VCCD012
AA42	VCCD012
AA46	VCCD012
AA48	VCCD012

Table 2-2. Lands by Number (Sheet 2 of 94)

Land No.	Land Name
AA50	VCCD012
AA52	VCCD012
AA54	CD_HFI1_RESET_N
AA56	VSS
AA58	DDR1_ECC[2]
AA6	DDR0_DQS_DP[16]
AA60	DDR1_ECC[4]
AA62	VSS
AA64	DDR1_DQ[26]
AA66	DDR1_DQ[29]
AA68	VSS
AA70	DDR1_DQ[18]
AA72	DDR1_DQ[20]
AA74	VSS
AA76	DDR1_DQ[10]
AA78	DDR1_DQ[13]
AA8	VSS
AA80	VSS
AA82	DDR1_DQ[2]
AA84	DDR1_DQ[5]
AA86	VSS
AB1	RSVD
AB11	DDR0_DQ[55]
AB13	DDR0_DQ[49]
AB15	VSS
AB17	DDR0_DQ[47]
AB19	DDR0_DQ[41]
AB21	VSS
AB23	DDR0_DQ[39]
AB25	DDR0_DQ[33]
AB27	VSS
AB29	VSS
AB3	VSS
AB31	VSS
AB33	ERROR_N[2]
AB35	VCCDDRIO012
AB37	VCCDDRIO012
AB39	VCCDDRIO012
AB41	VCCDDRIO012

Table 2-2. Lands by Number (Sheet 3 of 94)

Land No.	Land Name
AB43	VSS
AB45	VCCDDRIO012
AB47	VCCDDRIO012
AB49	VCCDDRIO012
AB5	DDR0_DQ[63]
AB51	VCCDDRIO012
AB53	VCCDDRIO012
AB55	VSS
AB57	VSS
AB59	DDR1_DQS_DP[8]
AB61	VSS
AB63	VSS
AB65	DDR1_DQS_DN[3]
AB67	VSS
AB69	VSS
AB7	DDR0_DQ[57]
AB71	DDR1_DQS_DN[2]
AB73	VSS
AB75	VSS
AB77	DDR1_DQS_DN[1]
AB79	VSS
AB81	VSS
AB83	DDR1_DQS_DP[0]
AB85	VSS
AB9	VSS
AC10	DDR0_DQ[54]
AC12	DDR0_DQS_DP[15]
AC14	DDR0_DQ[48]
AC16	DDR0_DQ[46]
AC18	DDR0_DQS_DN[14]
AC2	RSVD
AC20	DDR0_DQ[40]
AC22	DDR0_DQ[38]
AC24	DDR0_DQS_DP[13]
AC26	DDR0_DQ[32]
AC28	VSS
AC30	VSS
AC32	VSS
AC34	ERROR_N[1]

Table 2-2. Lands by Number (Sheet 4 of 94)

Land No.	Land Name
AC36	VCCDDRIO012
AC38	VCCDDRIO012
AC4	DDR0_DQ[62]
AC40	VCCDDRIO012
AC42	VCCDDRIO012
AC46	VSS
AC48	VSS
AC50	VSS
AC52	VSS
AC54	VSS
AC56	DDR0_DQS_DN[17]
AC58	VSS
AC6	DDR0_DQS_DN[16]
AC60	VSS
AC62	DDR0_DQS_DP[12]
AC64	VSS
AC66	VSS
AC68	DDR0_DQS_DN[11]
AC70	VSS
AC72	VSS
AC74	DDR0_DQS_DP[10]
AC76	VSS
AC78	VSS
AC8	DDR0_DQ[56]
AC80	DDR0_DQS_DN[9]
AC82	VSS
AC84	VSS
AC86	RSVD
AD1	RSVD
AD11	VSS
AD13	VSS
AD15	VSS
AD17	VSS
AD19	VSS
AD21	VSS
AD23	VSS
AD25	VSS
AD27	VSS
AD29	VSS

Table 2-2. Lands by Number (Sheet 5 of 94)

Land No.	Land Name
AD3	VSS
AD31	RSVD
AD33	ERROR_N[0]
AD35	VSS
AD37	VSS
AD39	VSS
AD41	VSS
AD43	VSS
AD45	VCCCLR
AD47	VCCCLR
AD49	VCCCLR
AD5	VSS
AD51	VSS
AD53	VSS
AD55	DDR0_ECC[7]
AD57	DDR0_ECC[1]
AD59	VSS
AD61	DDR0_DQ[31]
AD63	DDR0_DQ[25]
AD65	VSS
AD67	DDR0_DQ[23]
AD69	DDR0_DQ[17]
AD7	VSS
AD71	VSS
AD73	DDR0_DQ[15]
AD75	DDR0_DQ[9]
AD77	VSS
AD79	DDR0_DQ[7]
AD81	DDR0_DQ[1]
AD83	VSS
AD85	RSVD
AD9	VSS
AE10	DDR0_DQ[51]
AE12	DDR0_DQS_DN[6]
AE14	DDR0_DQ[53]
AE16	DDR0_DQ[43]
AE18	DDR0_DQS_DP[5]
AE2	RSVD
AE20	DDR0_DQ[44]

Table 2-2. Lands by Number (Sheet 6 of 94)

Land No.	Land Name
AE22	DDR0_DQ[35]
AE24	DDR0_DQS_DN[4]
AE26	DDR0_DQ[36]
AE28	VSS
AE30	VSS
AE32	RSVD
AE34	VSS
AE36	DDR012_RCOMP[1]
AE38	DDR012_RCOMP[2]
AE4	DDR0_DQ[59]
AE40	DDR012_RCOMP[0]
AE42	DDR012_DRAM_PWR_OK
AE46	VCCCLR
AE48	VCCCLR
AE50	VCCCLR
AE52	VSS
AE54	DDR0_ECC[6]
AE56	DDR0_DQS_DP[17]
AE58	DDR0_ECC[0]
AE6	DDR0_DQS_DP[7]
AE60	DDR0_DQ[30]
AE62	DDR0_DQS_DN[12]
AE64	DDR0_DQ[24]
AE66	DDR0_DQ[22]
AE68	DDR0_DQS_DP[11]
AE70	DDR0_DQ[16]
AE72	DDR0_DQ[14]
AE74	DDR0_DQS_DN[10]
AE76	DDR0_DQ[8]
AE78	DDR0_DQ[6]
AE8	DDR0_DQ[60]
AE80	DDR0_DQS_DP[9]
AE82	DDR0_DQ[0]
AE84	RSVD
AE86	RSVD
AF1	RSVD
AF11	DDR0_DQ[50]
AF13	DDR0_DQ[52]
AF15	VSS

Table 2-2. Lands by Number (Sheet 7 of 94)

Land No.	Land Name
AF17	DDR0_DQ[42]
AF19	DDR0_DQ[45]
AF21	VSS
AF23	DDR0_DQ[34]
AF25	DDR0_DQ[37]
AF27	VSS
AF29	VSS
AF3	VSS
AF31	VSS
AF33	VSS
AF35	VSS
AF37	VSS
AF39	VSS
AF41	VSS
AF43	VSS
AF45	VCCCLR
AF47	VCCCLR
AF49	VCCCLR
AF5	DDR0_DQ[58]
AF51	VCCCLR
AF53	VSS
AF55	VSS
AF57	VSS
AF59	VSS
AF61	VSS
AF63	VSS
AF65	VSS
AF67	VSS
AF69	VSS
AF7	DDR0_DQ[61]
AF71	VSS
AF73	VSS
AF75	VSS
AF77	VSS
AF79	VSS
AF81	VSS
AF83	VSS
AF85	VSS_VCCMP0123_SENSE
AF9	VSS

Table 2-2. Lands by Number (Sheet 8 of 94)

Land No.	Land Name
AG10	VSS
AG12	DDR0_DQS_DP[6]
AG14	VSS
AG16	VSS
AG18	DDR0_DQS_DN[5]
AG2	RSVD
AG20	VSS
AG22	VSS
AG24	DDR0_DQS_DP[4]
AG26	VSS
AG28	VSS
AG30	VCCU
AG32	VSS
AG34	VCCP
AG36	VCCP
AG38	VCCP
AG4	VSS
AG40	VCCP
AG42	VCCP
AG46	VCCCLR
AG48	VCCCLR
AG50	VCCCLR
AG52	VSS
AG54	DDR0_ECC[3]
AG56	DDR0_DQS_DN[8]
AG58	DDR0_ECC[5]
AG6	DDR0_DQS_DN[7]
AG60	DDR0_DQ[27]
AG62	DDR0_DQS_DP[3]
AG64	DDR0_DQ[28]
AG66	DDR0_DQ[19]
AG68	DDR0_DQS_DN[2]
AG70	DDR0_DQ[21]
AG72	DDR0_DQ[11]
AG74	DDR0_DQS_DP[1]
AG76	DDR0_DQ[12]
AG78	DDR0_DQ[3]
AG8	VSS
AG80	DDR0_DQS_DN[0]

Table 2-2. Lands by Number (Sheet 9 of 94)

Land No.	Land Name
AG82	DDR0_DQ[4]
AG84	VSS
AG86	VCCMP0123_SENSE
AH1	VCCMP4567
AH11	VSS
AH13	VSS
AH15	VSS
AH19	VSS
AH21	RSVD
AH23	VSS
AH25	VSS
AH27	RSVD
AH29	VCCU
AH3	VCCMP4567
AH31	VSS
AH33	VCCP
AH35	VCCP
AH37	VCCP
AH39	VCCP
AH41	VCCP
AH45	VCCCLR
AH47	VCCCLR
AH49	VCCCLR
AH5	VSS
AH51	VCCCLR
AH53	VSS
AH55	DDR0_ECC[2]
AH57	DDR0_ECC[4]
AH59	VSS
AH61	DDR0_DQ[26]
AH63	DDR0_DQ[29]
AH65	VSS
AH67	DDR0_DQ[18]
AH69	DDR0_DQ[20]
AH7	VSS
AH71	VSS
AH73	DDR0_DQ[10]
AH75	DDR0_DQ[13]
AH77	VSS

Table 2-2. Lands by Number (Sheet 10 of 94)

Land No.	Land Name
AH79	DDR0_DQ[2]
AH81	DDR0_DQ[5]
AH83	VSS
AH85	VCCMP0123
AH9	VSS
AJ10	VCCMLB4567
AJ12	VSS
AJ14	VCCMLB4567
AJ18	VSS
AJ2	VCCMP4567
AJ20	VSS
AJ22	RSVD
AJ24	VSS
AJ26	SVIDCLK
AJ28	VSS
AJ30	VSS
AJ32	VCCP
AJ34	VCCP
AJ36	VCCP
AJ4	VCCMP4567
AJ46	VCCCLR
AJ48	VCCCLR
AJ50	VCCCLR
AJ52	VSS
AJ54	VSS
AJ56	DDR0_DQS_DP[8]
AJ58	VSS
AJ6	VSS
AJ60	VSS
AJ62	DDR0_DQS_DN[3]
AJ64	VSS
AJ66	VSS
AJ68	DDR0_DQS_DP[2]
AJ70	VSS
AJ74	DDR0_DQS_DN[1]
AJ76	VSS
AJ78	VSS
AJ8	VSS
AJ80	DDR0_DQS_DP[0]

Table 2-2. Lands by Number (Sheet 11 of 94)

Land No.	Land Name
AJ82	VSS
AJ84	VCCMP0123
AJ86	VCCMP0123
AK1	VCCMP4567
AK11	VCCMLB4567
AK13	VCCMLB4567
AK19	VCCMIO4567
AK21	VSS
AK23	RSVD
AK25	RSVD
AK27	RSVD
AK29	VCCU
AK3	VCCMP4567
AK31	VCCP
AK33	VCCP
AK35	VCCP
AK45	VCCCLR
AK47	VCCCLR
AK49	VCCCLR
AK5	VCCMP4567
AK51	VCCCLR
AK53	VCCCLR
AK55	VSS
AK57	VSS
AK59	RSVD
AK61	VSS
AK63	VSS
AK65	VCCOPIO01
AK67	VSS
AK69	VSS
AK7	VCCMPLL67
AK73	VSS
AK75	VSS
AK77	VCCMLB0123
AK79	VSS
AK81	VSS
AK83	VSS
AK85	VCCMP0123
AK9	VSS_VCCMLB4567_SENSE

Table 2-2. Lands by Number (Sheet 12 of 94)

Land No.	Land Name
AL10	VCCMLB4567
AL12	VCCMLB4567
AL14	VCCMLB4567
AL18	VCCMIO4567
AL2	VCCMP4567
AL20	VCCOPIO67
AL22	VCCOPIO67
AL24	RSVD
AL26	VSS
AL28	VCCU
AL30	VSS
AL32	VCCP
AL34	VCCP
AL4	VCCMP4567
AL46	VCCCLR
AL48	VCCCLR
AL50	VCCCLR
AL52	VCCCLR
AL54	VCCCLR
AL56	VSS
AL58	VSS_VCCCLR_SENSE
AL6	VSS
AL60	RSVD
AL62	VSS
AL64	VSS
AL66	VCCOPIO01
AL68	VSS
AL74	VSS
AL76	VSS
AL78	VCCMLB0123
AL8	VCCMLB4567_SENSE
AL80	VSS
AL82	VCCMLB0123
AL84	VCCMP0123
AL86	VCCMP0123
AM1	VSS
AM11	VCCMLB4567
AM13	VCCMLB4567
AM19	VSS

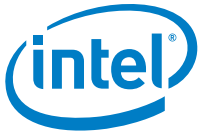


Table 2-2. Lands by Number (Sheet 13 of 94)

Land No.	Land Name
AM21	VCCOPIO67
AM23	VSS
AM25	THERMTRIP_N
AM27	VSS
AM29	VCCU
AM3	VCCMP4567
AM31	VCCP
AM33	VCCP
AM5	VCCMP4567
AM53	VCCCLR
AM55	VSS
AM57	VCCCLR_SENSE
AM59	VSS
AM61	RSVD
AM63	RSVD
AM65	VCCOPIO01
AM67	VCCOPIO01
AM69	VCCMIOQ0123
AM7	VCCMPLL67
AM73	VCCMPLL01
AM75	VCCMPLL01
AM77	VCCMLB0123
AM79	VCCMLB0123
AM81	VCCMLB0123
AM83	VSS
AM85	VCCMP0123
AM9	VCCMLB4567
AN10	VCCMLB4567
AN12	VCCMLB4567
AN14	VCCMIOQ4567
AN18	VCCMIO4567
AN2	VSS
AN20	VCCOPIO67
AN22	VCCOPIO67
AN24	SVIDDATA
AN26	RSVD
AN28	VCCU
AN30	VSS
AN32	VCCP

Table 2-2. Lands by Number (Sheet 14 of 94)

Land No.	Land Name
AN4	VCCMP4567
AN54	VCCCLR
AN56	VCCCLR
AN58	VCCCLR
AN6	VSS
AN60	VSS
AN62	RSVD
AN64	RSVD
AN66	VCCOPIO01
AN68	VSS
AN74	VSS
AN76	VSS
AN78	VCCMLB0123
AN8	VSS
AN80	VCCMLB0123
AN82	VCCMLB0123
AN84	VCCMP0123
AN86	VCCMP0123
AP1	RSVD
AP11	VSS
AP13	VSS
AP17	VCCMIO4567
AP19	VSS
AP21	VCCOPIO67
AP23	VSS
AP25	RSVD
AP27	RSVD
AP29	VCCU_SENSE
AP3	TEST[4]
AP31	VCCP
AP5	TEST[5]
AP55	VCCCLR
AP57	VCCCLR
AP59	VCCCLR
AP61	VSS
AP63	VCCMF
AP65	VCCOPIO01
AP67	VCCOPIO01
AP69	VCCMIOQ0123

Table 2-2. Lands by Number (Sheet 15 of 94)

Land No.	Land Name
AP7	VCCMF
AP73	VCCMIO0123
AP75	VSS
AP77	VSS
AP79	VSS
AP81	VCCMLB0123
AP83	VSS
AP85	VCCMP0123
AP9	VSS
AR10	VCCMH67
AR12	VCCMH67
AR14	VCCMIOQ4567
AR16	VCCMIOQ4567
AR18	VCCMIO4567
AR2	RSVD
AR20	VCCOPIO67
AR22	VCCOPIO67
AR24	SVIDALERT_N
AR26	TEST[27]
AR28	VSS_VCCU_SENSE
AR30	VCCP
AR4	TEST[6]
AR56	VCCCLR
AR58	VSS
AR6	TEST[7]
AR60	VCCCLR
AR62	VSS
AR64	RSVD
AR66	VCCOPIO01
AR68	VSS
AR72	VCCMIO0123
AR74	VCCMIO0123
AR76	TEST[8]
AR78	TEST[9]
AR8	VCCMF
AR80	VCCMLB0123
AR82	VCCMLB0123
AR84	VCCMP0123
AR86	VCCMP0123

Table 2-2. Lands by Number (Sheet 16 of 94)

Land No.	Land Name
AT1	VSS
AT11	VSS
AT13	VSS
AT15	VSS
AT17	VSS
AT19	VSS
AT21	VSS
AT23	VSS
AT25	VSS
AT27	VSS
AT29	VCCP
AT3	VSS
AT5	VSS
AT57	VCCCLR
AT59	VCCCLR
AT61	VCCCLR
AT63	VCCMF
AT65	VSS
AT67	VSS
AT69	VCCMIOQ0123
AT7	VSS
AT71	VCCMIO0123
AT73	VCCMIO0123
AT75	TEST[10]
AT77	TEST[11]
AT79	VSS
AT81	VSS
AT83	VSS
AT85	VSS
AT9	VSS
AU10	VSS
AU12	VSS
AU14	VSS
AU16	VSS
AU18	VSS
AU2	VSS_VCCP_SENSE
AU20	VSS
AU22	VSS
AU24	VSS

Table 2-2. Lands by Number (Sheet 17 of 94)

Land No.	Land Name
AU26	VSS
AU28	VCCP
AU4	VSS
AU58	VCCCLR
AU6	VSS
AU60	VCCCLR
AU62	VCCCLR
AU64	RSVD
AU66	VSS
AU68	VCCMH01
AU70	VSS
AU72	VSS
AU74	VSS
AU76	VSS
AU78	VSS
AU8	VSS
AU80	VSS
AU82	VSS
AU84	VSS
AU86	VSS
AV1	VCCP_SENSE
AV11	VCCP
AV13	VCCP
AV15	VCCP
AV17	VCCP
AV19	VCCP
AV21	VCCP
AV23	VCCP
AV25	VCCP
AV27	VCCP
AV3	VCCP
AV5	VCCP
AV59	VCCCLR
AV61	VCCCLR
AV63	VSS
AV65	RSVD
AV67	VCCMH01
AV69	VSS
AV7	VCCP

Table 2-2. Lands by Number (Sheet 18 of 94)

Land No.	Land Name
AV71	VSS
AV73	DMI_TX_DP[2]
AV75	DMI_TX_DP[0]
AV77	VSS
AV79	PE1B_RX_DP[7]
AV81	PE1B_RX_DP[5]
AV83	PE1A_RX_DP[3]
AV85	PE1A_RX_DP[1]
AV9	VCCP
AW10	VCCP
AW12	VCCP
AW14	VCCP
AW16	VCCP
AW18	VCCP
AW2	VCCP
AW20	VCCP
AW22	VCCP
AW24	VCCP
AW26	VCCP
AW4	VCCP
AW6	VCCP
AW60	VSS
AW62	VCCCLR
AW64	RSVD
AW66	VSS
AW68	VCCH_2P5
AW70	PE_REFCLK_DN
AW72	VSS
AW74	DMI_TX_DP[3]
AW76	DMI_TX_DP[1]
AW78	VSS
AW8	VCCP
AW80	PE1B_RX_DP[6]
AW82	PE1B_RX_DP[4]
AW84	PE1A_RX_DP[2]
AW86	PE1A_RX_DP[0]
AY11	VCCP
AY13	VCCP
AY15	VCCP

Table 2-2. Lands by Number (Sheet 19 of 94)

Land No.	Land Name
AY17	VCCP
AY19	VCCP
AY21	VCCP
AY23	VCCP
AY25	VCCP
AY27	VCCP
AY3	VCCP
AY5	VCCP
AY61	VCCCLR
AY63	VCCCLR
AY65	VSS
AY67	VSS
AY69	VSS
AY7	VCCP
AY71	VSS
AY73	DMI_TX_DN[2]
AY75	DMI_TX_DN[0]
AY77	VSS
AY79	PE1B_RX_DN[7]
AY81	PE1B_RX_DN[5]
AY83	PE1A_RX_DN[3]
AY85	PE1A_RX_DN[1]
AY9	VCCP
B11	RSVD
B13	RSVD
B15	RSVD
B17	RSVD
B25	RSVD
B27	RSVD
B29	RSVD
B3	RSVD
B31	RSVD
B33	RSVD
B35	RSVD
B37	RSVD
B39	RSVD
B41	RSVD
B43	RSVD
B47	RSVD

Table 2-2. Lands by Number (Sheet 20 of 94)

Land No.	Land Name
B49	RSVD
B5	RSVD
B51	RSVD
B53	RSVD
B55	RSVD
B57	RSVD
B59	RSVD
B61	RSVD
B63	RSVD
B7	RSVD
B71	CD_HFI0_LED_N
B73	CD_PRESENT_N
B75	TEST[0]
B77	CD_TMS
B79	RSVD
B81	RSVD
B9	RSVD
BA10	VCCP
BA12	VCCP
BA14	VCCP
BA16	VCCP
BA18	VCCP
BA2	VCCP
BA20	VCCP
BA22	VCCP
BA24	VCCP
BA26	VCCP
BA4	VCCP
BA6	VCCP
BA60	VSS
BA62	VCCCLR
BA64	VSS
BA66	VCCE_1P0
BA68	VCCH_2P5
BA70	PE_REFCLK_DP
BA72	VSS
BA74	DMI_TX_DN[3]
BA76	DMI_TX_DN[1]
BA78	VSS

Table 2-2. Lands by Number (Sheet 21 of 94)

Land No.	Land Name
BA8	VCCP
BA80	PE1B_RX_DN[6]
BA82	PE1B_RX_DN[4]
BA84	PE1A_RX_DN[2]
BA86	PE1A_RX_DN[0]
BB11	VCCP
BB13	VCCP
BB15	VCCP
BB17	VCCP
BB19	VCCP
BB21	VCCP
BB23	VCCP
BB25	VCCP
BB27	VCCP
BB3	VCCP
BB5	VCCP
BB61	VCCCLR
BB63	VCCCLR
BB65	VCCE_1P0
BB67	VSS
BB69	VSS
BB7	VCCP
BB71	VSS
BB73	VSS
BB75	VSS
BB77	VSS
BB79	VSS
BB81	VSS
BB83	VSS
BB85	VSS
BB9	VCCP
BC10	VCCP
BC12	VCCP
BC14	VCCP
BC16	VCCP
BC18	VCCP
BC2	VCCP
BC20	VCCP
BC22	VCCP

Table 2-2. Lands by Number (Sheet 22 of 94)

Land No.	Land Name
BC24	VCCP
BC26	VCCP
BC4	VCCP
BC6	VCCP
BC60	VCCCLR
BC62	VCCCLR
BC64	VSS
BC66	VCCE_1P0
BC68	VSS
BC70	RSVD
BC72	VSS
BC74	VSS
BC76	VSS
BC78	VSS
BC8	VCCP
BC80	VSS
BC82	VSS
BC84	VSS
BD11	VSS
BD13	VSS
BD15	VSS
BD17	VSS
BD19	VSS
BD21	VSS
BD23	VSS
BD25	VSS
BD27	VSS
BD3	VSS
BD5	VSS
BD61	VCCCLR
BD63	VCCCLR
BD65	VCCE_1P0
BD67	VSS
BD69	RSVD
BD7	VSS
BD71	VSS
BD73	DMI_RX_DP[1]
BD75	DMI_RX_DP[3]
BD77	VSS

Table 2-2. Lands by Number (Sheet 23 of 94)

Land No.	Land Name
BD79	PE1B_TX_DP[6]
BD81	PE1B_TX_DP[4]
BD83	PE1A_TX_DP[2]
BD85	PE1A_TX_DP[0]
BD9	VSS
BE10	VSS
BE12	VSS
BE14	VSS
BE16	VSS
BE18	VSS
BE20	VSS
BE22	VSS
BE24	VSS
BE26	VSS
BE4	VSS
BE6	VSS
BE60	VSS
BE62	VCCCLR
BE64	VSS
BE66	VCCE_1P0
BE68	VCCE_1P0
BE70	VSS
BE72	DMI_RX_DP[0]
BE74	DMI_RX_DP[2]
BE76	VSS
BE78	PE1B_TX_DP[7]
BE8	VSS
BE80	PE1B_TX_DP[5]
BE82	PE1A_TX_DP[3]
BE84	PE1A_TX_DP[1]
BF11	VCCP
BF13	VCCP
BF15	VCCP
BF17	VCCP
BF19	VCCP
BF21	VCCP
BF23	VCCP
BF25	VCCP
BF27	VCCP

Table 2-2. Lands by Number (Sheet 24 of 94)

Land No.	Land Name
BF3	VCCP
BF5	VCCP
BF61	VCCCLR
BF63	VSS
BF65	VSS
BF67	VSS
BF69	RSVD
BF7	VCCP
BF71	RSVD
BF73	DMI_RX_DN[1]
BF75	DMI_RX_DN[3]
BF77	VSS
BF79	PE1B_TX_DN[6]
BF81	PE1B_TX_DN[4]
BF83	PE1A_TX_DN[2]
BF85	PE1A_TX_DN[0]
BF9	VCCP
BG10	VCCP
BG12	VCCP
BG14	VCCP
BG16	VCCP
BG18	VCCP
BG20	VCCP
BG22	VCCP
BG24	VCCP
BG26	VCCP
BG4	VCCP
BG6	VCCP
BG60	VCCCLR
BG62	VCCCLR
BG64	VCCCLR
BG66	VSS
BG68	VCCE_1P0
BG70	RSVD
BG72	DMI_RX_DN[0]
BG74	DMI_RX_DN[2]
BG76	VSS
BG78	PE1B_TX_DN[7]
BG8	VCCP

Table 2-2. Lands by Number (Sheet 25 of 94)

Land No.	Land Name
BG80	PE1B_TX_DN[5]
BG82	PE1A_TX_DN[3]
BG84	PE1A_TX_DN[1]
BH11	VCCP
BH13	VCCP
BH15	VCCP
BH17	VCCP
BH19	VCCP
BH21	VCCP
BH23	VCCP
BH25	VCCP
BH27	VCCP
BH3	VCCP
BH5	VCCP
BH61	VCCCLR
BH63	VCCCLR
BH65	VSS
BH67	VCC_CDCORE
BH69	RSVD
BH7	VCCP
BH71	VSS
BH73	VSS
BH75	VSS
BH77	VSS
BH79	VSS
BH81	VSS
BH83	VSS
BH9	VCCP
BJ10	VCCP
BJ12	VCCP
BJ14	VCCP
BJ16	VCCP
BJ18	VCCP
BJ20	VCCP
BJ22	VCCP
BJ24	VCCP
BJ26	VCCP
BJ4	VCCP
BJ6	VCCP

Table 2-2. Lands by Number (Sheet 26 of 94)

Land No.	Land Name
BJ60	VCCCLR
BJ62	VCCCLR
BJ64	VCCCLR
BJ66	VCC_CDCORE
BJ68	VSS
BJ70	VSS
BJ72	VSS
BJ74	VSS
BJ76	VSS
BJ78	VSS
BJ8	VCCP
BJ80	VSS
BJ82	VSS
BJ84	RSVD
BK11	VSS
BK13	VSS
BK15	VSS
BK17	VSS
BK19	VSS
BK21	VSS
BK23	VSS
BK25	VSS
BK27	VSS
BK3	VCCP
BK5	VSS
BK61	VCCCLR
BK63	VCCCLR
BK65	VCC_CDCORE
BK67	VSS
BK69	PE3D_RX_DP[14]
BK7	VSS
BK71	PE3D_RX_DP[12]
BK73	PE3C_RX_DP[10]
BK75	PE3C_RX_DP[8]
BK77	PE3B_RX_DP[6]
BK79	PE3B_RX_DP[4]
BK81	PE3A_RX_DP[2]
BK83	PE3A_RX_DP[0]
BK9	VSS

Table 2-2. Lands by Number (Sheet 27 of 94)

Land No.	Land Name
BL10	VSS
BL12	VSS
BL14	VSS
BL16	VSS
BL18	VSS
BL20	VSS
BL22	VSS
BL24	VSS
BL26	VSS
BL4	VSS
BL6	VSS
BL60	VSS
BL62	VCCCLR
BL64	VSS
BL66	VCC_CDCORE
BL68	PE3D_RX_DP[15]
BL70	PE3D_RX_DP[13]
BL72	PE3C_RX_DP[11]
BL74	PE3C_RX_DP[9]
BL76	PE3B_RX_DP[7]
BL78	PE3B_RX_DP[5]
BL8	VSS
BL80	PE3A_RX_DP[3]
BL82	PE3A_RX_DP[1]
BL84	VSS
BM11	VCCP
BM13	VCCP
BM15	VCCP
BM17	VCCP
BM19	VCCP
BM21	VCCP
BM23	VCCP
BM25	VCCP
BM27	VCCP
BM3	VCCP
BM5	VCCP
BM61	VCCCLR
BM63	VSS
BM65	VCC_CDCORE

Table 2-2. Lands by Number (Sheet 28 of 94)

Land No.	Land Name
BM67	VSS
BM69	PE3D_RX_DN[14]
BM7	VCCP
BM71	PE3D_RX_DN[12]
BM73	PE3C_RX_DN[10]
BM75	PE3C_RX_DN[8]
BM77	PE3B_RX_DN[6]
BM79	PE3B_RX_DN[4]
BM81	PE3A_RX_DN[2]
BM83	PE3A_RX_DN[0]
BM9	VCCP
BN10	VCCP
BN12	VCCP
BN14	VCCP
BN16	VCCP
BN18	VCCP
BN20	VCCP
BN22	VCCP
BN24	VCCP
BN26	VCCP
BN4	VCCP
BN6	VCCP
BN60	VCCCLR
BN62	VCCCLR
BN64	VCCCLR
BN66	VCC_CDCORE
BN68	PE3D_RX_DN[15]
BN70	PE3D_RX_DN[13]
BN72	PE3C_RX_DN[11]
BN74	PE3C_RX_DN[9]
BN76	PE3B_RX_DN[7]
BN78	PE3B_RX_DN[5]
BN8	VCCP
BN80	PE3A_RX_DN[3]
BN82	PE3A_RX_DN[1]
BN84	RSVD
BP11	VCCP
BP13	VCCP
BP15	VCCP

Table 2-2. Lands by Number (Sheet 29 of 94)

Land No.	Land Name
BP17	VCCP
BP19	VCCP
BP21	VCCP
BP23	VCCP
BP25	VCCP
BP27	VCCP
BP3	VCCP
BP5	VCCP
BP61	VCCCLR
BP63	VCCCLR
BP65	VSS
BP67	VSS
BP69	VSS
BP7	VCCP
BP71	VSS
BP73	VSS
BP75	VSS
BP77	VSS
BP79	VSS
BP81	VSS
BP83	VSS
BP9	VCCP
BR10	VCCP
BR12	VCCP
BR14	VCCP
BR16	VCCP
BR18	VCCP
BR20	VCCP
BR22	VCCP
BR24	VCCP
BR26	VCCP
BR4	VCCP
BR6	VCCP
BR60	VCCCLR
BR62	VCCCLR
BR64	VCCCLR
BR66	VCC_CDCORE
BR68	VSS
BR70	VSS

Table 2-2. Lands by Number (Sheet 30 of 94)

Land No.	Land Name
BR72	VSS
BR74	VSS
BR76	VSS
BR78	VSS
BR8	VCCP
BR80	VSS
BR82	VSS
BR84	VSS
BT11	VSS
BT13	VSS
BT15	VSS
BT17	VSS
BT19	VSS
BT21	VSS
BT23	VSS
BT25	VSS
BT27	VSS
BT3	VCCP
BT5	VSS
BT61	VCCCLR
BT63	VSS
BT65	VCC_CDCORE
BT67	VCC_CDCORE
BT69	PE3D_TX_DP[15]
BT7	VSS
BT71	PE3D_TX_DP[13]
BT73	PE3C_TX_DP[11]
BT75	PE3C_TX_DP[9]
BT77	PE3B_TX_DP[7]
BT79	PE3B_TX_DP[5]
BT81	PE3A_TX_DP[3]
BT83	PE3A_TX_DP[1]
BT9	VSS
BU10	VSS
BU12	VSS
BU14	VSS
BU16	VSS
BU18	VSS
BU20	VSS

Table 2-2. Lands by Number (Sheet 31 of 94)

Land No.	Land Name
BU22	VSS
BU24	VSS
BU26	VSS
BU4	VSS
BU6	VSS
BU60	VSS
BU62	VCCCLR
BU64	VSS
BU66	VCC_CDCORE
BU68	VSS
BU70	PE3D_TX_DP[14]
BU72	PE3D_TX_DP[12]
BU74	PE3C_TX_DP[10]
BU76	PE3C_TX_DP[8]
BU78	PE3B_TX_DP[6]
BU8	VSS
BU80	PE3B_TX_DP[4]
BU82	PE3A_TX_DP[2]
BU84	PE3A_TX_DP[0]
BV11	VCCP
BV13	VCCP
BV15	VCCP
BV17	VCCP
BV19	VCCP
BV21	VCCP
BV23	VCCP
BV25	VCCP
BV27	VCCP
BV3	VCCP
BV5	VCCP
BV61	VCCCLR
BV63	VCCCLR
BV65	VCC_CDCORE
BV67	VCC_CDCORE
BV69	PE3D_TX_DN[15]
BV7	VCCP
BV71	PE3D_TX_DN[13]
BV73	PE3C_TX_DN[11]
BV75	PE3C_TX_DN[9]

Table 2-2. Lands by Number (Sheet 32 of 94)

Land No.	Land Name
BV77	PE3B_TX_DN[7]
BV79	PE3B_TX_DN[5]
BV81	PE3A_TX_DN[3]
BV83	PE3A_TX_DN[1]
BV9	VCCP
BW10	VCCP
BW12	VCCP
BW14	VCCP
BW16	VCCP
BW18	VCCP
BW20	VCCP
BW22	VCCP
BW24	VCCP
BW26	VCCP
BW4	VCCP
BW6	VCCP
BW60	VCCCLR
BW62	VCCCLR
BW64	VCCCLR
BW66	VCC_CDCORE
BW68	VSS
BW70	PE3D_TX_DN[14]
BW72	PE3D_TX_DN[12]
BW74	PE3C_TX_DN[10]
BW76	PE3C_TX_DN[8]
BW78	PE3B_TX_DN[6]
BW8	VCCP
BW80	PE3B_TX_DN[4]
BW82	PE3A_TX_DN[2]
BW84	PE3A_TX_DN[0]
BY11	VCCP
BY13	VCCP
BY15	VCCP
BY17	VCCP
BY19	VCCP
BY21	VCCP
BY23	VCCP
BY25	VCCP
BY27	VCCP

Table 2-2. Lands by Number (Sheet 33 of 94)

Land No.	Land Name
BY3	VCCP
BY5	VCCP
BY61	VCCCLR
BY63	VSS
BY65	VSS
BY67	VSS_VCC_CDCORE_SENSE
BY69	VSS
BY7	VCCP
BY71	VSS
BY73	VSS
BY75	VSS
BY77	VSS
BY79	VSS
BY81	VSS
BY83	VSS
BY9	VCCP
C10	RSVD
C12	RSVD
C14	RSVD
C16	RSVD
C18	RSVD
C24	RSVD
C26	RSVD
C28	RSVD
C30	RSVD
C32	RSVD
C34	RSVD
C36	RSVD
C38	RSVD
C4	RSVD
C40	RSVD
C42	RSVD
C46	RSVD
C48	RSVD
C50	RSVD
C52	RSVD
C54	RSVD
C56	RSVD
C58	RSVD

Table 2-2. Lands by Number (Sheet 34 of 94)

Land No.	Land Name
C6	RSVD
C60	RSVD
C62	RSVD
C64	RSVD
C72	CD_HFI0_INT_N
C74	RSVD
C76	CD_PERST_N
C78	CD_TRST_N
C8	RSVD
C80	RSVD
C82	RSVD
CA10	VCCP
CA12	VCCP
CA14	VCCP
CA16	VCCP
CA18	VCCP
CA2	VCCP
CA20	VCCP
CA22	VCCP
CA24	VCCP
CA26	VCCP
CA4	VCCP
CA6	VCCP
CA60	VCCCLR
CA62	VCCCLR
CA64	VCCCLR
CA66	VCC_CDCORE_SENSE
CA68	VSS
CA70	VSS
CA72	VSS
CA74	VSS
CA76	VSS
CA78	VSS
CA8	VCCP
CA80	VSS
CA82	VSS
CA84	VSS
CB11	VCCP
CB13	VCCP

Table 2-2. Lands by Number (Sheet 35 of 94)

Land No.	Land Name
CB15	VCCP
CB17	VCCP
CB19	VCCP
CB21	VCCP
CB23	VCCP
CB25	VCCP
CB27	VCCP
CB3	VCCP
CB5	VCCP
CB61	VCCCLR
CB63	VCCCLR
CB65	VCCH_1P8
CB67	VSS
CB69	PE2D_TX_DP[15]
CB7	VCCP
CB71	PE2D_TX_DP[13]
CB73	PE2C_TX_DP[11]
CB75	PE2C_TX_DP[9]
CB77	PE2B_TX_DP[7]
CB79	PE2A_TX_DP[0]
CB81	PE2A_TX_DP[2]
CB83	PE2B_TX_DP[5]
CB9	VCCP
CC10	VSS
CC12	VSS
CC14	VSS
CC16	VSS
CC18	VSS
CC2	VSS
CC20	VSS
CC22	VSS
CC24	VSS
CC26	VSS
CC4	VSS
CC6	VSS
CC60	VSS
CC62	VCCCLR
CC64	VSS
CC66	VCCH_1P8

Table 2-2. Lands by Number (Sheet 36 of 94)

Land No.	Land Name
CC68	VSS
CC70	PE2D_TX_DP[14]
CC72	PE2D_TX_DP[12]
CC74	PE2C_TX_DP[10]
CC76	PE2C_TX_DP[8]
CC78	PE2B_TX_DP[6]
CC8	VSS
CC80	PE2A_TX_DP[1]
CC82	PE2A_TX_DP[3]
CC84	PE2B_TX_DP[4]
CD11	VSS
CD13	VSS
CD15	VSS
CD17	VSS
CD19	VSS
CD21	VSS
CD23	VSS
CD25	VSS
CD27	VSS
CD3	VSS
CD5	VSS
CD61	VCCCLR
CD63	VCCCLR
CD65	VSS
CD67	VSS
CD69	PE2D_TX_DN[15]
CD7	VSS
CD71	PE2D_TX_DN[13]
CD73	PE2C_TX_DN[11]
CD75	PE2C_TX_DN[9]
CD77	PE2B_TX_DN[7]
CD79	PE2A_TX_DN[0]
CD81	PE2A_TX_DN[2]
CD83	PE2B_TX_DN[5]
CD85	VSS
CD9	VSS
CE10	OBS[0]
CE12	RSVD
CE14	TEST[14]

Table 2-2. Lands by Number (Sheet 37 of 94)

Land No.	Land Name
CE16	RSVD
CE18	RSVD
CE2	TEST[15]
CE20	BPM_N[7]
CE22	BPM_N[3]
CE24	BPM_N[0]
CE26	VCCP
CE4	OBSSTB_P[1]
CE6	OBS[15]
CE60	VCCCLR
CE62	VSS
CE64	VCCCLR
CE66	RSVD
CE68	VSS
CE70	PE2D_TX_DN[14]
CE72	PE2D_TX_DN[12]
CE74	PE2C_TX_DN[10]
CE76	PE2C_TX_DN[8]
CE78	PE2B_TX_DN[6]
CE8	OBS[8]
CE80	PE2A_TX_DN[1]
CE82	PE2A_TX_DN[3]
CE84	PE2B_TX_DN[4]
CF11	OBS[6]
CF13	RSVD
CF15	TEST[16]
CF17	RSVD
CF19	VSS
CF21	BPM_N[5]
CF23	BPM_N[2]
CF25	VSS
CF27	VCCP
CF3	RSVD
CF5	OBSSTB_N[1]
CF61	VCCCLR
CF63	VCCCLR
CF65	VSS
CF67	RSVD
CF69	VSS

Table 2-2. Lands by Number (Sheet 38 of 94)

Land No.	Land Name
CF7	OBSSTB_N[0]
CF71	VSS
CF73	VSS
CF75	VSS
CF77	VSS
CF79	VSS
CF81	VSS
CF83	VSS
CF85	VSS
CF9	OBS[7]
CG10	OBS[4]
CG12	RSVD
CG14	TEST[17]
CG16	TEST[18]
CG18	RSVD
CG2	RSVD
CG20	BPM_N[6]
CG22	BPM_N[4]
CG24	BPM_N[1]
CG26	VCCP
CG4	RSVD
CG6	OBSSTB_P[0]
CG60	VCCCLR
CG62	VCCCLR
CG64	VCCCLR
CG66	RSVD
CG68	VSS
CG70	VSS
CG72	VSS
CG74	VSS
CG76	VSS
CG78	VSS
CG8	OBS[1]
CG80	VSS
CG82	VSS
CG84	VSS
CH1	VCCU
CH11	VSS
CH13	RSVD

Table 2-2. Lands by Number (Sheet 39 of 94)

Land No.	Land Name
CH15	VSS
CH17	VSS
CH19	VSS
CH21	VSS
CH23	VSS
CH25	VSS
CH27	VCCP
CH3	RSVD
CH5	RSVD
CH61	VCCCLR
CH63	VCCCLR
CH65	VSS
CH67	RSVD
CH69	PE2D_RX_DP[15]
CH7	VSS
CH71	PE2D_RX_DP[13]
CH73	PE2C_RX_DP[11]
CH75	PE2C_RX_DP[9]
CH77	PE2B_RX_DP[7]
CH79	PE2B_RX_DP[5]
CH81	PE2A_RX_DP[0]
CH83	PE2A_RX_DP[2]
CH85	VSS
CH9	VSS
CJ10	VCCMF
CJ12	VSS
CJ14	VSS
CJ16	VCCMIOQ4567
CJ18	VSS
CJ2	VCCU
CJ20	VCCMIO4567
CJ22	VSS
CJ24	VSS
CJ26	VCCP
CJ28	VCCP
CJ4	RSVD
CJ6	OBS[14]
CJ60	VSS
CJ62	VCCCLR

Table 2-2. Lands by Number (Sheet 40 of 94)

Land No.	Land Name
CJ64	VCCCLR
CJ66	TEST[19]
CJ68	VSS
CJ70	PE2D_RX_DP[14]
CJ72	PE2D_RX_DP[12]
CJ74	PE2C_RX_DP[10]
CJ76	PE2C_RX_DP[8]
CJ78	PE2B_RX_DP[6]
CJ8	OBS[2]
CJ80	PE2B_RX_DP[4]
CJ82	PE2A_RX_DP[1]
CJ84	PE2A_RX_DP[3]
CJ86	CD_PE_REFCLK_DP
CK1	VCCU
CK11	VCCMF
CK13	VCCMLB4567
CK15	VSS
CK17	VCCMIOQ4567
CK19	VSS
CK21	VCCMIO4567
CK23	SPDSCL0
CK25	VSS
CK27	VCCP
CK29	VCCP
CK3	RSVD
CK5	OBS[12]
CK59	VSS
CK61	VSS
CK63	VSS
CK65	VSS
CK67	TEST[20]
CK69	PE2D_RX_DN[15]
CK7	OBS[9]
CK71	PE2D_RX_DN[13]
CK73	PE2C_RX_DN[11]
CK75	PE2C_RX_DN[9]
CK77	PE2B_RX_DN[7]
CK79	PE2B_RX_DN[5]
CK81	PE2A_RX_DN[0]

Table 2-2. Lands by Number (Sheet 41 of 94)

Land No.	Land Name
CK83	PE2A_RX_DN[2]
CK85	VSS
CK9	OBS[5]
CL10	VSS
CL12	VSS
CL14	VCCMLB4567
CL16	VSS
CL18	VCCMIOQ4567
CL2	RSVD
CL20	VCCMIO4567
CL22	VCCMIO4567
CL24	RSVD
CL26	VSS
CL28	VCCP
CL30	VCCP
CL4	OBS[13]
CL58	VCCPIO
CL6	OBS[11]
CL60	VCCP_1P0
CL62	VCCP_1P0
CL64	VCCP_1P0
CL66	TEST[21]
CL68	VSS
CL70	PE2D_RX_DN[14]
CL72	PE2D_RX_DN[12]
CL74	PE2C_RX_DN[10]
CL76	PE2C_RX_DN[8]
CL78	PE2B_RX_DN[6]
CL8	OBS[10]
CL80	PE2B_RX_DN[4]
CL82	PE2A_RX_DN[1]
CL84	PE2A_RX_DN[3]
CL86	CD_PE_REFCLK_DN
CM1	VSS
CM11	VSS
CM13	VCCMLB4567
CM15	VCCMLB4567
CM19	VSS
CM21	VCCMIO4567

Table 2-2. Lands by Number (Sheet 42 of 94)

Land No.	Land Name
CM23	SPDSDA0
CM25	TEST[28]
CM27	VSS
CM29	VCCP
CM3	VSS
CM31	VCCP
CM5	VSS
CM57	VCCPIO
CM59	VCCPIO
CM61	VCCP_1P0
CM63	VCCP_1P0
CM65	VSS
CM67	TEST[22]
CM69	VSS
CM7	VSS
CM71	VSS
CM73	VSS
CM75	VSS
CM77	VSS
CM79	VSS
CM81	VSS
CM83	VSS
CM85	VSS
CM9	OBS[3]
CN10	VSS
CN12	VCCMLB4567
CN14	VCCMLB4567
CN18	VCCMH45
CN2	VSS
CN20	VSS
CN22	VSS
CN24	RSVD
CN26	PRDY_N
CN28	RSVD
CN30	VCCP
CN32	VCCP
CN4	VCCMP4567
CN56	VCCPIO
CN58	VCCPIO

Table 2-2. Lands by Number (Sheet 43 of 94)

Land No.	Land Name
CN6	VSS
CN60	VCCP_1P0
CN62	VSS
CN64	VCCOPIO23
CN66	VCCMIOQ0123
CN68	VCCMIO0123
CN70	VSS
CN74	VSS
CN76	VSS
CN78	VSS
CN8	VSS
CN80	VSS
CN82	VSS
CN84	VSS
CN86	VSS
CP1	VCCMP4567
CP11	VCCMLB4567
CP13	VCCMLB4567
CP19	VSS
CP21	VCCOPIO45
CP23	VSS
CP25	PROCHOT_N
CP27	CATERR_N
CP29	TDI
CP3	VCCMP4567
CP31	VCCP
CP33	VCCP
CP5	VCCMP4567
CP55	VSS
CP57	VCCPIO
CP59	VCCPIO
CP61	VSS
CP63	VCCOPIO23
CP65	VSS
CP67	VSS
CP69	VCCMIO0123
CP7	VSS_VCCMP4567_SENSE
CP73	VCCMLB0123
CP75	VCCMLB0123

Table 2-2. Lands by Number (Sheet 44 of 94)

Land No.	Land Name
CP77	VCCMLB0123
CP79	VCCMLB0123
CP81	VSS
CP83	VSS
CP85	VSS
CP9	VCCMPLL45
CR10	VSS
CR12	VCCMLB4567
CR14	VCCMLB4567
CR18	VCCMH45
CR2	VCCMP4567
CR20	VCCOPIO45
CR22	VCCOPIO45
CR24	CPUPWRGD
CR26	VSS
CR28	VSS
CR30	VSS
CR32	VCCP
CR34	VCCP
CR4	VCCMP4567
CR54	VCCIIO
CR56	VCCPIO
CR58	VCCPIO
CR6	VCCMP4567_SENSE
CR60	VCCPIO
CR62	VCCOPIO23
CR64	VCCOPIO23
CR66	VCCMIOQ0123
CR68	VCCMIO0123
CR74	VCCMLB0123
CR76	VCCMLB0123
CR78	VCCMLB0123
CR8	VSS
CR80	VSS
CR82	VCCMP0123
CR84	VCCMP0123
CR86	VCCMP0123
CT1	VCCMP4567
CT11	VCCMLB4567

Table 2-2. Lands by Number (Sheet 45 of 94)

Land No.	Land Name
CT13	VCCMLB4567
CT19	VSS
CT21	VCCOPIO45
CT23	VCCOPIO45
CT25	TEST[26]
CT27	BCLK0_DN
CT29	TMS
CT3	VCCMP4567
CT31	VSS
CT33	VCCP
CT35	VCCP
CT37	VCCP
CT39	VCCP
CT41	RSVD
CT5	VCCMP4567
CT53	VCCIIO
CT55	VSS
CT57	VCCPIO
CT59	VCCPIO
CT61	VCCOPIO23
CT63	VCCOPIO23
CT65	VSS
CT67	VSS
CT69	VCCMIO0123
CT7	VSS
CT73	VCCMLB0123
CT75	VCCMLB0123
CT77	VCCMLB0123
CT79	VCCMLB0123
CT81	VCCMP0123
CT83	VCCMP0123
CT85	VCCMP0123
CT9	VCCMPLL45
CU10	VSS
CU12	VSS
CU14	VSS
CU18	VSS
CU2	VCCMP4567
CU20	VCCOPIO45

Table 2-2. Lands by Number (Sheet 46 of 94)

Land No.	Land Name
CU22	VCCOPIO45
CU24	VSS
CU26	VSS
CU28	VSS
CU30	PMSYNC
CU32	VSS
CU34	VCCP
CU36	VCCP
CU38	VCCP
CU4	VCCMP4567
CU40	VCCP
CU42	RSVD
CU52	VCCIIO
CU54	VCCIIO
CU56	VSS
CU58	VCCPIO
CU6	VSS
CU60	VSS
CU62	VCCOPIO23
CU64	VCCOPIO23
CU66	VCCMIOQ0123
CU68	VCCMIO0123
CU74	VCCMLB0123
CU76	VSS
CU78	VSS
CU8	VSS
CU80	VSS
CU82	VCCMP0123
CU84	VCCMP0123
CU86	VCCMP0123
CV1	VSS
CV11	VSS
CV13	VSS
CV17	VSS
CV19	VSS
CV21	VCCOPIO45
CV23	VSS
CV25	VSS
CV27	BCLK0_DP

Table 2-2. Lands by Number (Sheet 47 of 94)

Land No.	Land Name
CV29	PECI
CV3	VCCMP4567
CV31	BIST_ENABLE
CV33	VCCP
CV35	VCCP
CV37	VCCP
CV39	VCCP
CV41	VCCU
CV5	VSS
CV51	VCCIIO
CV53	VCCIIO
CV55	VCCMF
CV57	VSS
CV59	VCCPIO_SENSE
CV61	VSS
CV63	VSS
CV65	VSS
CV67	VCCMH23
CV69	VSS
CV7	VSS
CV73	VCCMLB0123_SENSE
CV75	VSS
CV77	VCCMPLL23
CV79	VSS
CV81	VSS
CV83	VCCMP0123
CV85	VCCMP0123
CV9	VSS
CW10	VSS
CW12	DDR3_DQS_DP[15]
CW14	VSS
CW16	VSS
CW18	DDR3_DQS_DP[14]
CW2	VSS
CW20	VSS
CW22	VSS
CW24	DDR3_DQS_DP[13]
CW26	VSS
CW28	VSS

Table 2-2. Lands by Number (Sheet 48 of 94)

Land No.	Land Name
CW30	VSS
CW32	VSS
CW34	VCCP
CW36	VCCP
CW38	VCCP
CW4	VSS
CW40	VCCP
CW42	VCCU
CW46	VSS
CW48	VSS
CW50	VSS
CW52	VCCIIO
CW54	VCCMF
CW56	VSS
CW58	VSS
CW6	DDR3_DQS_DP[16]
CW60	VSS_VCCPIO_SENSE
CW62	VSS
CW64	VSS
CW66	VCCMH23
CW68	VSS
CW72	VSS_VCCMLB0123_SENSE
CW74	VSS
CW76	VSS
CW78	VCCMPLL23
CW8	VSS
CW80	VSS
CW82	VSS
CW84	VCCMP0123
CW86	VSS
CY1	RSVD
CY11	DDR3_DQ[50]
CY13	DDR3_DQ[53]
CY15	VSS
CY17	DDR3_DQ[42]
CY19	DDR3_DQ[45]
CY21	VSS
CY23	DDR3_DQ[34]
CY25	DDR3_DQ[37]

Table 2-2. Lands by Number (Sheet 49 of 94)

Land No.	Land Name
CY27	VSS
CY29	TRST_N
CY3	VSS
CY31	TEST[32]
CY33	VSS
CY35	VSS
CY37	VSS
CY39	VSS
CY41	VSS
CY45	VSS
CY47	DDR345_DRAM_PWR_OK
CY49	DDR345_MEMHOT_N
CY5	DDR3_DQ[63]
CY51	VSS
CY53	VSS
CY55	VSS
CY57	DDR3_DQS_DP[17]
CY59	VSS
CY61	VSS
CY63	DDR3_DQS_DP[12]
CY65	VSS
CY67	VSS
CY69	DDR3_DQS_DN[11]
CY7	DDR3_DQ[61]
CY71	VSS
CY73	VSS
CY75	DDR3_DQS_DP[10]
CY77	VSS
CY79	VSS
CY81	DDR3_DQS_DN[9]
CY83	VSS
CY85	VSS
CY9	VSS
D11	RSVD
D13	RSVD
D15	RSVD
D17	RSVD
D25	RSVD
D27	RSVD

Table 2-2. Lands by Number (Sheet 50 of 94)

Land No.	Land Name
D29	DDR2_C2
D3	RSVD
D31	DDR2_MA[13]
D33	DDR2_CS_N[0]
D35	DDR2_MA[0]
D37	DDR2_CLK_DP[2]
D39	VCCD012
D41	VSS
D43	RSVD
D45	RSVD
D47	VSS
D49	DDR2_MA[9]
D5	RSVD
D51	DDR2_BG0
D53	DDR2_CKE[1]
D55	RSVD
D57	RSVD
D59	RSVD
D61	RSVD
D63	RSVD
D65	RSVD
D7	RSVD
D71	CD_HFI0_MODPRST_N
D73	RSVD
D75	TEST[13]
D77	CD_TDI
D79	CD_TDO
D81	RSVD
D83	RSVD
D9	RSVD
DA10	DDR3_DQ[51]
DA12	DDR3_DQS_DN[15]
DA14	DDR3_DQ[52]
DA16	DDR3_DQ[43]
DA18	DDR3_DQS_DN[14]
DA2	SKTOCC_N
DA20	DDR3_DQ[44]
DA22	DDR3_DQ[35]
DA24	DDR3_DQS_DN[13]

Table 2-2. Lands by Number (Sheet 51 of 94)

Land No.	Land Name
DA26	DDR3_DQ[36]
DA28	RSVD
DA30	TDO
DA32	TEST[30]
DA34	VSS
DA36	VCCU
DA38	VCCU
DA4	DDR3_DQ[59]
DA40	VCCU
DA42	VSS
DA44	VSS
DA46	DDR345_RCOMP[0]
DA48	DDR345_RESET_N
DA50	VSS
DA52	VCCLVR
DA54	VSS
DA56	DDR3_ECC[2]
DA58	DDR3_ECC[5]
DA6	DDR3_DQS_DN[16]
DA60	VSS
DA62	DDR3_DQ[27]
DA64	DDR3_DQ[29]
DA66	VSS
DA68	DDR3_DQ[19]
DA70	DDR3_DQ[17]
DA72	VSS
DA74	DDR3_DQ[11]
DA76	DDR3_DQ[13]
DA78	VSS
DA8	DDR3_DQ[60]
DA80	DDR3_DQ[2]
DA82	DDR3_DQ[1]
DA84	VSS
DA86	CD_HFI_REFCLK_DN
DB1	RSVD
DB11	VSS
DB13	VSS
DB15	VSS
DB17	VSS

Table 2-2. Lands by Number (Sheet 52 of 94)

Land No.	Land Name
DB19	VSS
DB21	VSS
DB23	VSS
DB25	VSS
DB27	VSS
DB29	TCK
DB3	VSS
DB31	DEBUG_EN_N
DB33	TEST[29]
DB35	VSS
DB37	VSS
DB39	VSS
DB41	VSS
DB45	DDR345_RCOMP[2]
DB47	DDR345_RCOMP[1]
DB49	DDR345_VREFCA
DB5	VSS
DB51	VCCLVR
DB53	VCCLVR
DB55	DDR3_ECC[3]
DB57	DDR3_DQS_DN[17]
DB59	DDR3_ECC[4]
DB61	DDR3_DQ[26]
DB63	DDR3_DQS_DN[12]
DB65	DDR3_DQ[28]
DB67	DDR3_DQ[18]
DB69	DDR3_DQS_DP[11]
DB7	VSS
DB71	DDR3_DQ[21]
DB73	DDR3_DQ[10]
DB75	DDR3_DQS_DN[10]
DB77	DDR3_DQ[12]
DB79	DDR3_DQ[3]
DB81	DDR3_DQS_DP[9]
DB83	DDR3_DQ[5]
DB85	VSS
DB9	VSS
DC10	DDR3_DQ[55]
DC12	DDR3_DQS_DP[6]

Table 2-2. Lands by Number (Sheet 53 of 94)

Land No.	Land Name
DC14	DDR3_DQ[49]
DC16	DDR3_DQ[47]
DC18	DDR3_DQS_DP[5]
DC2	VSS
DC20	DDR3_DQ[40]
DC22	DDR3_DQ[39]
DC24	DDR3_DQS_DP[4]
DC26	DDR3_DQ[33]
DC28	RSVD
DC30	RESET_N
DC32	TEST[31]
DC34	VSS
DC36	VSS
DC38	VSS
DC4	DDR3_DQ[58]
DC40	VSS
DC42	VSS
DC44	VSS
DC46	VSS
DC48	VSS
DC50	VSS
DC52	VCCLVR
DC54	VSS
DC56	VSS
DC58	VSS
DC6	DDR3_DQS_DP[7]
DC60	VSS
DC62	VSS
DC64	VSS
DC66	VSS
DC68	VSS
DC70	VSS
DC72	VSS
DC74	VSS
DC76	VSS
DC78	VSS
DC8	DDR3_DQ[56]
DC80	VSS
DC82	VSS

Table 2-2. Lands by Number (Sheet 54 of 94)

Land No.	Land Name
DC84	VSS
DC86	CD_HFI_REFCLK_DP
DD11	DDR3_DQ[54]
DD13	DDR3_DQ[48]
DD15	VSS
DD17	DDR3_DQ[46]
DD19	DDR3_DQ[41]
DD21	VSS
DD23	DDR3_DQ[38]
DD25	DDR3_DQ[32]
DD27	VSS
DD29	VSS
DD3	VSS
DD31	VSS
DD33	VSS
DD35	VCCDDRIO345
DD37	VCCDDRIO345
DD39	VCCDDRIO345
DD41	VCCDDRIO345
DD45	VCCDDRIO345
DD47	VCCDDRIO345
DD49	VCCDDRIO345
DD5	DDR3_DQ[62]
DD51	VSS
DD53	VSS
DD55	DDR3_ECC[7]
DD57	DDR3_DQS_DP[8]
DD59	DDR3_ECC[0]
DD61	DDR3_DQ[31]
DD63	DDR3_DQS_DP[3]
DD65	DDR3_DQ[25]
DD67	DDR3_DQ[23]
DD69	DDR3_DQS_DP[2]
DD7	DDR3_DQ[57]
DD71	DDR3_DQ[20]
DD73	DDR3_DQ[15]
DD75	DDR3_DQS_DP[1]
DD77	DDR3_DQ[9]
DD79	DDR3_DQ[7]

Table 2-2. Lands by Number (Sheet 55 of 94)

Land No.	Land Name
DD81	DDR3_DQS_DP[0]
DD83	DDR3_DQ[4]
DD85	VSS
DD9	VSS
DE10	VSS
DE12	DDR3_DQS_DN[6]
DE14	VSS
DE16	VSS
DE18	DDR3_DQS_DN[5]
DE2	DDR4_DQ[59]
DE20	VSS
DE22	VSS
DE24	DDR3_DQS_DN[4]
DE26	VSS
DE28	PREQ_N
DE30	VSS
DE32	VCCDDRIO345
DE34	VCCDDRIO345
DE36	VCCDDRIO345
DE38	VCCDDRIO345
DE4	VSS
DE40	VCCDDRIO345
DE42	VSS
DE44	VCCDDRIO345
DE46	VCCDDRIO345
DE48	VCCDDRIO345
DE50	VCCDDRIO345
DE52	VCCDDRIO345
DE54	VSS
DE56	DDR3_ECC[6]
DE58	DDR3_ECC[1]
DE6	DDR3_DQS_DN[7]
DE60	VSS
DE62	DDR3_DQ[30]
DE64	DDR3_DQ[24]
DE66	VSS
DE68	DDR3_DQ[22]
DE70	DDR3_DQ[16]
DE72	VSS

Table 2-2. Lands by Number (Sheet 56 of 94)

Land No.	Land Name
DE74	DDR3_DQ[14]
DE76	DDR3_DQ[8]
DE78	VSS
DE8	VSS
DE80	DDR3_DQ[6]
DE82	DDR3_DQ[0]
DE84	VSS
DF11	VSS
DF13	VSS
DF15	DDR4_DQS_DP[14]
DF17	VSS
DF19	VSS
DF21	DDR4_DQS_DP[13]
DF23	VSS
DF25	VSS
DF27	VSS
DF29	RSVD
DF3	DDR4_DQS_DP[16]
DF31	VCCD345
DF33	VCCD345
DF35	VCCD345
DF37	VCCD345
DF39	VCCD345
DF41	VCCD345
DF45	VCCD345
DF47	VCCD345
DF49	VCCD345
DF5	VSS
DF51	VCCD345
DF53	VCCD345
DF55	VSS
DF57	DDR3_DQS_DN[8]
DF59	VSS
DF61	VSS
DF63	DDR3_DQS_DN[3]
DF65	VSS
DF67	VSS
DF69	DDR3_DQS_DN[2]
DF7	VSS

Table 2-2. Lands by Number (Sheet 57 of 94)

Land No.	Land Name
DF71	VSS
DF73	VSS
DF75	DDR3_DQS_DN[1]
DF77	VSS
DF79	VSS
DF81	DDR3_DQS_DN[0]
DF83	VSS
DF85	DDR4_DQ[5]
DF9	DDR4_DQS_DP[15]
DG10	DDR4_DQ[53]
DG12	VSS
DG14	DDR4_DQ[42]
DG16	DDR4_DQ[45]
DG18	VSS
DG2	DDR4_DQ[63]
DG20	DDR4_DQ[34]
DG22	DDR4_DQ[37]
DG24	VSS
DG26	RSVD
DG28	RSVD
DG30	VCCD345
DG32	DDR3_ODT[1]
DG34	DDR3_ODT[0]
DG36	DDR3_RAS_N_MA[16]
DG38	DDR3_BA1
DG4	DDR4_DQ[61]
DG40	DDR3_CLK_DN[2]
DG42	VCCD345
DG44	VCCD345
DG46	DDR3_MA[4]
DG48	DDR3_MA[7]
DG50	DDR3_ALERT_N
DG52	DDR3_CKE[0]
DG54	RSVD
DG56	VSS
DG58	VSS
DG6	VSS
DG60	DDR4_DQS_DP[17]
DG62	VSS

Table 2-2. Lands by Number (Sheet 58 of 94)

Land No.	Land Name
DG64	VSS
DG66	DDR4_DQS_DP[12]
DG68	VSS
DG70	VSS
DG72	DDR4_DQS_DP[11]
DG74	VSS
DG76	VSS
DG78	DDR4_DQS_DP[10]
DG8	DDR4_DQ[50]
DG80	VSS
DG82	VSS
DG84	DDR4_DQS_DN[9]
DH11	DDR4_DQ[52]
DH13	DDR4_DQ[43]
DH15	DDR4_DQS_DN[14]
DH17	DDR4_DQ[44]
DH19	DDR4_DQ[35]
DH21	DDR4_DQS_DN[13]
DH23	DDR4_DQ[36]
DH25	RSVD
DH27	RSVD
DH29	RSVD
DH3	DDR4_DQS_DN[16]
DH31	DDR3_C1_CS_N[3]
DH33	DDR3_CS_N[1]
DH35	DDR3_WE_N_MA[14]
DH37	DDR3_AP_MA[10]
DH39	DDR3_CLK_DP[2]
DH41	VCCD345
DH45	DDR3_MA[2]
DH47	DDR3_MA[6]
DH49	DDR3_MA[11]
DH5	DDR4_DQ[60]
DH51	DDR3_BG1
DH53	RSVD
DH55	RSVD
DH57	VSS
DH59	DDR4_ECC[2]
DH61	DDR4_ECC[5]

Table 2-2. Lands by Number (Sheet 59 of 94)

Land No.	Land Name
DH63	VSS
DH65	DDR4_DQ[27]
DH67	DDR4_DQ[29]
DH69	VSS
DH7	DDR4_DQ[51]
DH71	DDR4_DQ[19]
DH73	DDR4_DQ[17]
DH75	VSS
DH77	DDR4_DQ[11]
DH79	DDR4_DQ[13]
DH81	VSS
DH83	DDR4_DQ[2]
DH85	DDR4_DQ[1]
DH9	DDR4_DQS_DN[15]
DJ10	VSS
DJ12	VSS
DJ14	VSS
DJ16	VSS
DJ18	VSS
DJ2	VSS
DJ20	VSS
DJ22	VSS
DJ24	VSS
DJ26	RSVD
DJ28	RSVD
DJ30	VCCD345
DJ32	VCCD345
DJ34	VCCD345
DJ36	VCCD345
DJ38	VCCD345
DJ4	VSS
DJ40	VCCD345
DJ42	VCCD345
DJ44	VCCD345
DJ46	VCCD345
DJ48	VCCD345
DJ50	VCCD345
DJ52	VCCD345
DJ54	VSS

Table 2-2. Lands by Number (Sheet 60 of 94)

Land No.	Land Name
DJ56	VSS
DJ58	DDR4_ECC[3]
DJ6	VSS
DJ60	DDR4_DQS_DN[17]
DJ62	DDR4_ECC[4]
DJ64	DDR4_DQ[26]
DJ66	DDR4_DQS_DN[12]
DJ68	DDR4_DQ[28]
DJ70	DDR4_DQ[18]
DJ72	DDR4_DQS_DN[11]
DJ74	DDR4_DQ[21]
DJ76	DDR4_DQ[10]
DJ78	DDR4_DQS_DN[10]
DJ8	VSS
DJ80	DDR4_DQ[12]
DJ82	DDR4_DQ[3]
DJ84	DDR4_DQS_DP[9]
DK11	DDR4_DQ[49]
DK13	DDR4_DQ[47]
DK15	DDR4_DQS_DP[5]
DK17	DDR4_DQ[40]
DK19	DDR4_DQ[39]
DK21	DDR4_DQS_DP[4]
DK23	DDR4_DQ[33]
DK25	RSVD
DK27	RSVD
DK29	RSVD
DK3	DDR4_DQS_DP[7]
DK31	DDR3_C2
DK33	DDR3_MA[13]
DK35	DDR3_CS_N[0]
DK37	DDR3_MA[0]
DK39	VCCD345
DK41	DDR3_CLK_DN[0]
DK45	DDR3_MA[1]
DK47	DDR3_MA[5]
DK49	DDR3_MA[9]
DK5	DDR4_DQ[56]
DK51	DDR3_BG0

Table 2-2. Lands by Number (Sheet 61 of 94)

Land No.	Land Name
DK53	DDR3_CKE[1]
DK55	RSVD
DK57	VSS
DK59	VSS
DK61	VSS
DK63	VSS
DK65	VSS
DK67	VSS
DK69	VSS
DK7	DDR4_DQ[55]
DK71	VSS
DK73	VSS
DK75	VSS
DK77	VSS
DK79	VSS
DK81	VSS
DK83	VSS
DK85	VSS
DK9	DDR4_DQS_DP[6]
DL10	DDR4_DQ[48]
DL12	VSS
DL14	DDR4_DQ[46]
DL16	DDR4_DQ[41]
DL18	VSS
DL2	DDR4_DQ[62]
DL20	DDR4_DQ[38]
DL22	DDR4_DQ[32]
DL24	VSS
DL26	RSVD
DL28	RSVD
DL30	DDR3_C0_CS_N[2]
DL32	DDR3_MA[17]
DL34	DDR3_CAS_N_MA[15]
DL36	DDR3_BA0
DL38	DDR3_PAR
DL4	DDR4_DQ[57]
DL40	DDR3_CLK_DP[0]
DL42	VCCD345
DL44	VCCD345

Table 2-2. Lands by Number (Sheet 62 of 94)

Land No.	Land Name
DL46	DDR3_MA[3]
DL48	DDR3_MA[8]
DL50	DDR3_BC_N_MA[12]
DL52	DDR3_ACT_N
DL54	RSVD
DL56	VSS
DL58	DDR4_ECC[7]
DL6	VSS
DL60	DDR4_DQS_DP[8]
DL62	DDR4_ECC[0]
DL64	DDR4_DQ[31]
DL66	DDR4_DQS_DP[3]
DL68	DDR4_DQ[25]
DL70	DDR4_DQ[23]
DL72	DDR4_DQS_DP[2]
DL74	DDR4_DQ[20]
DL76	DDR4_DQ[15]
DL78	DDR4_DQS_DP[1]
DL8	DDR4_DQ[54]
DL80	DDR4_DQ[9]
DL82	DDR4_DQ[7]
DL84	DDR4_DQS_DP[0]
DM11	VSS
DM13	VSS
DM15	DDR4_DQS_DN[5]
DM17	VSS
DM19	VSS
DM21	DDR4_DQS_DN[4]
DM23	VSS
DM25	VSS
DM27	RSVD
DM29	VCCD345
DM3	DDR4_DQS_DN[7]
DM31	VCCD345
DM33	VCCD345
DM35	VCCD345
DM37	VCCD345
DM39	VCCD345
DM41	VCCD345

Table 2-2. Lands by Number (Sheet 63 of 94)

Land No.	Land Name
DM45	VCCD345
DM47	VCCD345
DM49	VCCD345
DM5	VSS
DM51	VCCD345
DM53	VCCD345
DM55	RSVD
DM57	VSS
DM59	DDR4_ECC[6]
DM61	DDR4_ECC[1]
DM63	VSS
DM65	DDR4_DQ[30]
DM67	DDR4_DQ[24]
DM69	VSS
DM7	VSS
DM71	DDR4_DQ[22]
DM73	DDR4_DQ[16]
DM75	VSS
DM77	DDR4_DQ[14]
DM79	DDR4_DQ[8]
DM81	VSS
DM83	DDR4_DQ[6]
DM85	DDR4_DQ[0]
DM9	DDR4_DQS_DN[6]
DN10	VSS
DN12	DDR5_DQS_DN[15]
DN14	VSS
DN16	VSS
DN18	DDR5_DQS_DP[14]
DN2	DDR4_DQ[58]
DN20	VSS
DN22	VSS
DN24	DDR5_DQS_DN[13]
DN26	VSS
DN28	RSVD
DN30	DDR4_C0_CS_N[2]
DN32	DDR4_MA[17]
DN34	DDR4_CAS_N_MA[15]
DN36	DDR4_BA0

Table 2-2. Lands by Number (Sheet 64 of 94)

Land No.	Land Name
DN38	DDR4_BA1
DN4	VSS
DN40	DDR4_CLK_DN[2]
DN42	VCCD345
DN44	VCCD345
DN46	DDR4_MA[4]
DN48	DDR4_MA[7]
DN50	DDR4_ALERT_N
DN52	DDR4_CKE[0]
DN54	RSVD
DN56	VSS
DN58	VSS
DN6	DDR5_DQS_DP[16]
DN60	DDR4_DQS_DN[8]
DN62	VSS
DN64	VSS
DN66	DDR4_DQS_DN[3]
DN68	VSS
DN70	VSS
DN72	DDR4_DQS_DN[2]
DN74	VSS
DN76	VSS
DN78	DDR4_DQS_DN[1]
DN8	VSS
DN80	VSS
DN82	VSS
DN84	DDR4_DQS_DN[0]
DP11	DDR5_DQ[50]
DP13	DDR5_DQ[53]
DP15	VSS
DP17	DDR5_DQ[46]
DP19	DDR5_DQ[45]
DP21	VSS
DP23	DDR5_DQ[34]
DP25	DDR5_DQ[37]
DP27	VSS
DP29	RSVD
DP3	VSS
DP31	DDR4_C2

Table 2-2. Lands by Number (Sheet 65 of 94)

Land No.	Land Name
DP33	DDR4_MA[13]
DP35	DDR4_CS_N[0]
DP37	DDR4_MA[0]
DP39	DDR4_CLK_DP[2]
DP41	VCCD345
DP45	DDR4_MA[2]
DP47	DDR4_MA[6]
DP49	DDR4_MA[11]
DP5	DDR5_DQ[63]
DP51	DDR4_BG1
DP53	DDR4_CKE[1]
DP55	VSS
DP57	DDR5_DQS_DP[17]
DP59	VSS
DP61	VSS
DP63	DDR5_DQS_DP[12]
DP65	VSS
DP67	VSS
DP69	DDR5_DQS_DN[11]
DP7	DDR5_DQ[61]
DP71	VSS
DP73	VSS
DP75	DDR5_DQS_DP[10]
DP77	VSS
DP79	VSS
DP81	DDR5_DQS_DN[9]
DP83	VSS
DP85	DDR4_DQ[4]
DP9	VSS
DR10	DDR5_DQ[51]
DR12	DDR5_DQS_DP[15]
DR14	DDR5_DQ[52]
DR16	DDR5_DQ[47]
DR18	DDR5_DQS_DN[14]
DR2	VSS
DR20	DDR5_DQ[44]
DR22	DDR5_DQ[35]
DR24	DDR5_DQS_DP[13]
DR26	DDR5_DQ[36]

Table 2-2. Lands by Number (Sheet 66 of 94)

Land No.	Land Name
DR28	VCCD345
DR30	VCCD345
DR32	VCCD345
DR34	VCCD345
DR36	VCCD345
DR38	VCCD345
DR4	DDR5_DQ[59]
DR40	VCCD345
DR42	VCCD345
DR44	VCCD345
DR46	VCCD345
DR48	VCCD345
DR50	VCCD345
DR52	VCCD345
DR54	VSS
DR56	DDR5_ECC[2]
DR58	DDR5_ECC[5]
DR6	DDR5_DQS_DN[16]
DR60	VSS
DR62	DDR5_DQ[27]
DR64	DDR5_DQ[29]
DR66	VSS
DR68	DDR5_DQ[19]
DR70	DDR5_DQ[17]
DR72	VSS
DR74	DDR5_DQ[11]
DR76	DDR5_DQ[13]
DR78	VSS
DR8	DDR5_DQ[60]
DR80	DDR5_DQ[2]
DR82	DDR5_DQ[1]
DR84	VSS
DT11	VSS
DT13	VSS
DT15	VSS
DT17	VSS
DT19	VSS
DT21	VSS
DT23	VSS

Table 2-2. Lands by Number (Sheet 67 of 94)

Land No.	Land Name
DT25	VSS
DT27	VSS
DT29	RSVD
DT3	VSS
DT31	DDR4_C1_CS_N[3]
DT33	DDR4_CS_N[1]
DT35	DDR4_WE_N_MA[14]
DT37	DDR4_AP_MA[10]
DT39	VCCD345
DT41	DDR4_CLK_DN[0]
DT45	DDR4_MA[1]
DT47	DDR4_MA[5]
DT49	DDR4_MA[9]
DT5	VSS
DT51	DDR4_BG0
DT53	RSVD
DT55	DDR5_ECC[3]
DT57	DDR5_DQS_DN[17]
DT59	DDR5_ECC[4]
DT61	DDR5_DQ[26]
DT63	DDR5_DQS_DN[12]
DT65	DDR5_DQ[28]
DT67	DDR5_DQ[18]
DT69	DDR5_DQS_DP[11]
DT7	VSS
DT71	DDR5_DQ[21]
DT73	DDR5_DQ[10]
DT75	DDR5_DQS_DN[10]
DT77	DDR5_DQ[12]
DT79	DDR5_DQ[3]
DT81	DDR5_DQS_DP[9]
DT83	DDR5_DQ[5]
DT85	VSS
DT9	VSS
DU10	DDR5_DQ[55]
DU12	DDR5_DQS_DP[6]
DU14	DDR5_DQ[49]
DU16	DDR5_DQ[42]
DU18	DDR5_DQS_DN[5]

Table 2-2. Lands by Number (Sheet 68 of 94)

Land No.	Land Name
DU2	RSVD
DU20	DDR5_DQ[40]
DU22	DDR5_DQ[39]
DU24	DDR5_DQS_DN[4]
DU26	DDR5_DQ[33]
DU28	RSVD
DU30	VCCD345
DU32	DDR4_ODT[1]
DU34	DDR4_ODT[0]
DU36	DDR4_RAS_N_MA[16]
DU38	DDR4_PAR
DU4	DDR5_DQ[58]
DU40	DDR4_CLK_DP[0]
DU42	VCCD345
DU44	VCCD345
DU46	DDR4_MA[3]
DU48	DDR4_MA[8]
DU50	DDR4_BC_N_MA[12]
DU52	DDR4_ACT_N
DU54	VSS
DU56	VSS
DU58	VSS
DU6	DDR5_DQS_DP[7]
DU60	VSS
DU62	VSS
DU64	VSS
DU66	VSS
DU68	VSS
DU70	VSS
DU72	VSS
DU74	VSS
DU76	VSS
DU78	VSS
DU8	DDR5_DQ[56]
DU80	VSS
DU82	VSS
DU84	VSS
DV11	DDR5_DQ[54]
DV13	DDR5_DQ[48]

Table 2-2. Lands by Number (Sheet 69 of 94)

Land No.	Land Name
DV15	VSS
DV17	DDR5_DQS_DP[5]
DV19	DDR5_DQ[41]
DV21	VSS
DV23	DDR5_DQ[38]
DV25	DDR5_DQ[32]
DV27	VSS
DV29	VCCD345
DV3	VSS
DV31	VCCD345
DV33	VCCD345
DV35	VCCD345
DV37	VCCD345
DV39	VCCD345
DV41	VCCD345
DV45	VCCD345
DV47	VCCD345
DV49	VCCD345
DV5	DDR5_DQ[62]
DV51	VCCD345
DV53	VCCD345
DV55	DDR5_ECC[7]
DV57	DDR5_DQS_DP[8]
DV59	DDR5_ECC[0]
DV61	DDR5_DQ[31]
DV63	DDR5_DQS_DP[3]
DV65	DDR5_DQ[25]
DV67	DDR5_DQ[23]
DV69	DDR5_DQS_DP[2]
DV7	DDR5_DQ[57]
DV71	DDR5_DQ[20]
DV73	DDR5_DQ[15]
DV75	DDR5_DQS_DP[1]
DV77	DDR5_DQ[9]
DV79	DDR5_DQ[7]
DV81	DDR5_DQS_DP[0]
DV83	DDR5_DQ[4]
DV85	RSVD
DV9	VSS

Table 2-2. Lands by Number (Sheet 70 of 94)

Land No.	Land Name
DW10	VSS
DW12	DDR5_DQS_DN[6]
DW14	VSS
DW16	DDR5_DQ[43]
DW18	RSVD
DW2	RSVD
DW20	RSVD
DW22	RSVD
DW24	DDR5_DQS_DP[4]
DW26	VSS
DW28	RSVD
DW30	DDR5_ODT[1]
DW32	DDR5_ODT[0]
DW34	DDR5_RAS_N_MA[16]
DW36	DDR5_PAR
DW38	DDR5_CLK_DP[2]
DW4	VSS
DW40	DDR5_CLK_DN[0]
DW42	VCCD345
DW44	VCCD345
DW46	DDR5_MA[2]
DW48	DDR5_MA[5]
DW50	DDR5_MA[9]
DW52	DDR5_BG0
DW54	VSS
DW56	DDR5_ECC[6]
DW58	DDR5_ECC[1]
DW6	DDR5_DQS_DN[7]
DW60	VSS
DW62	DDR5_DQ[30]
DW64	DDR5_DQ[24]
DW66	VSS
DW68	DDR5_DQ[22]
DW70	DDR5_DQ[16]
DW72	VSS
DW74	DDR5_DQ[14]
DW76	DDR5_DQ[8]
DW78	VSS
DW8	VSS

Table 2-2. Lands by Number (Sheet 71 of 94)

Land No.	Land Name
DW80	DDR5_DQ[6]
DW82	DDR5_DQ[0]
DW84	VSS
DY11	VSS
DY13	VSS
DY15	VSS
DY17	RSVD
DY19	RSVD
DY21	RSVD
DY23	RSVD
DY25	VSS
DY27	RSVD
DY29	DDR5_C1_CS_N[3]
DY3	VSS
DY31	DDR5_CS_N[1]
DY33	DDR5_WE_N_MA[14]
DY35	DDR5_MA[0]
DY37	DDR5_CLK_DN[2]
DY39	DDR5_CLK_DP[0]
DY41	VCCD345
DY45	DDR5_MA[1]
DY47	DDR5_MA[3]
DY49	DDR5_MA[8]
DY5	VSS
DY51	DDR5_BC_N_MA[12]
DY53	DDR5_ACT_N
DY55	VSS
DY57	DDR5_DQS_DN[8]
DY59	VSS
DY61	VSS
DY63	DDR5_DQS_DN[3]
DY65	RSVD
DY67	RSVD
DY69	DDR5_DQS_DN[2]
DY7	VSS
DY71	VSS
DY73	VSS
DY75	DDR5_DQS_DN[1]
DY77	VSS

Table 2-2. Lands by Number (Sheet 72 of 94)

Land No.	Land Name
DY79	VSS
DY81	DDR5_DQS_DN[0]
DY83	VSS
DY85	RSVD
DY9	VSS
E10	RSVD
E12	VSS
E14	RSVD
E16	RSVD
E18	RSVD
E2	VSS
E20	RSVD
E22	RSVD
E24	VSS
E26	RSVD
E28	DDR2_C1_CS_N[3]
E30	DDR2_MA[17]
E32	DDR2_CAS_N_MA[15]
E34	DDR2_BA0
E36	DDR2_PAR
E38	DDR2_CLK_DN[2]
E4	RSVD
E40	VCCD012
E42	VSS
E46	VSS
E48	DDR2_MA[8]
E50	DDR2_BC_N_MA[12]
E52	DDR2_ACT_N
E54	VSS
E56	RSVD
E58	RSVD
E6	VSS
E60	RSVD
E62	RSVD
E64	RSVD
E66	RSVD
E72	VSS
E74	VSS
E76	VSS

Table 2-2. Lands by Number (Sheet 73 of 94)

Land No.	Land Name
E78	VSS
E8	RSVD
E80	VSS
E82	VSS
E84	RSVD
EA10	RSVD
EA12	VSS
EA14	VSS
EA16	VSS
EA18	RSVD
EA20	RSVD
EA22	RSVD
EA24	RSVD
EA26	RSVD
EA28	VCCD345
EA30	VCCD345
EA32	VCCD345
EA34	VCCD345
EA36	VCCD345
EA38	VCCD345
EA4	EAR_N
EA40	VCCD345
EA42	VSS
EA44	VSS
EA46	VCCD345
EA48	VCCD345
EA50	VCCD345
EA52	VCCD345
EA54	VCCD345
EA56	VSS
EA58	VSS
EA6	VSS
EA60	RSVD
EA62	VSS
EA64	RSVD
EA66	RSVD
EA68	RSVD
EA70	VSS
EA72	VSS

Table 2-2. Lands by Number (Sheet 74 of 94)

Land No.	Land Name
EA74	VSS
EA76	VSS
EA78	RSVD
EA8	VSS
EA80	VSS
EA82	VSS
EA84	VSS
EB11	VSS
EB13	RSVD
EB15	RSVD
EB21	RSVD
EB23	RSVD
EB25	RSVD
EB27	RSVD
EB29	DDR5_C0_CS_N[2]
EB3	RSVD
EB31	DDR5_MA[17]
EB33	DDR5_CAS_N_MA[15]
EB35	DDR5_BA0
EB37	DDR5_BA1
EB39	VCCD345
EB41	VSS
EB45	VSS
EB47	DDR5_MA[4]
EB49	DDR5_MA[7]
EB5	VSS
EB51	DDR5_ALERT_N
EB53	DDR5_CKE[0]
EB55	VSS
EB57	VSS
EB59	RSVD
EB61	RSVD
EB63	VSS
EB65	RSVD
EB67	RSVD
EB69	RSVD
EB7	RSVD
EB71	VSS
EB73	RSVD

Table 2-2. Lands by Number (Sheet 75 of 94)

Land No.	Land Name
EB75	VSS
EB77	RSVD
EB79	RSVD
EB81	VSS
EB83	RSVD
EB85	RSVD
EB9	RSVD
EC10	RSVD
EC12	RSVD
EC14	RSVD
EC16	RSVD
EC22	RSVD
EC24	RSVD
EC26	RSVD
EC28	VCCD345
EC30	DDR5_C2
EC32	DDR5_MA[13]
EC34	DDR5_CS_N[0]
EC36	DDR5_AP_MA[10]
EC38	VCCD345
EC4	RSVD
EC40	VSS
EC42	RSVD
EC44	RSVD
EC46	VSS
EC48	DDR5_MA[6]
EC50	DDR5_MA[11]
EC52	DDR5_BG1
EC54	DDR5_CKE[1]
EC56	RSVD
EC58	RSVD
EC6	RSVD
EC60	RSVD
EC62	RSVD
EC70	RSVD
EC72	RSVD
EC74	RSVD
EC76	RSVD
EC78	RSVD

Table 2-2. Lands by Number (Sheet 76 of 94)

Land No.	Land Name
EC8	RSVD
EC80	VSS
EC82	RSVD
EC84	VSS
ED11	RSVD
ED13	RSVD
ED15	RSVD
ED23	RSVD
ED25	RSVD
ED27	RSVD
ED29	RSVD
ED31	RSVD
ED33	RSVD
ED35	RSVD
ED37	RSVD
ED39	RSVD
ED41	RSVD
ED45	RSVD
ED47	RSVD
ED49	RSVD
ED5	RSVD
ED51	RSVD
ED53	RSVD
ED55	RSVD
ED57	RSVD
ED59	RSVD
ED61	RSVD
ED63	RSVD
ED69	RSVD
ED7	RSVD
ED71	RSVD
ED73	RSVD
ED75	RSVD
ED77	RSVD
ED79	RSVD
ED81	RSVD
ED83	RSVD
ED9	RSVD
EE10	RSVD

Table 2-2. Lands by Number (Sheet 77 of 94)

Land No.	Land Name
EE12	RSVD
EE14	RSVD
EE16	RSVD
EE24	RSVD
EE26	RSVD
EE28	RSVD
EE30	RSVD
EE32	RSVD
EE34	RSVD
EE36	RSVD
EE38	RSVD
EE40	RSVD
EE44	RSVD
EE46	RSVD
EE48	RSVD
EE50	RSVD
EE52	RSVD
EE54	RSVD
EE56	RSVD
EE58	RSVD
EE6	RSVD
EE60	RSVD
EE62	RSVD
EE70	RSVD
EE72	RSVD
EE74	RSVD
EE76	RSVD
EE78	RSVD
EE8	RSVD
EE80	RSVD
EE82	RSVD
EE84	RSVD
EF45	RSVD
EF47	RSVD
EF49	RSVD
EF51	RSVD
EF53	RSVD
EF55	RSVD
EF57	RSVD

Table 2-2. Lands by Number (Sheet 78 of 94)

Land No.	Land Name
EF59	RSVD
EF61	RSVD
EF63	RSVD
EF71	RSVD
EF73	RSVD
EF75	RSVD
EF77	RSVD
EF79	RSVD
EF81	RSVD
EF83	RSVD
F11	VSS
F13	VSS
F15	RSVD
F17	VSS
F19	RSVD
F21	RSVD
F23	RSVD
F25	VSS
F27	VSS
F29	VCCD012
F3	VSS
F31	VCCD012
F33	VCCD012
F35	VCCD012
F37	VCCD012
F39	VCCD012
F41	VCCD012
F43	VSS
F45	VSS
F47	VCCD012
F49	VCCD012
F5	VSS
F51	VCCD012
F53	VCCD012
F55	RSVD
F57	RSVD
F59	RSVD
F61	RSVD
F63	RSVD

Table 2-2. Lands by Number (Sheet 79 of 94)

Land No.	Land Name
F65	RSVD
F67	RSVD
F69	RSVD
F7	VSS
F71	VSS
F73	VSS
F75	VSS
F77	VSS
F79	VSS
F81	VSS
F83	VSS
F9	RSVD
G10	VSS
G12	DDR2_DQS_DN[15]
G14	VSS
G16	VSS
G18	DDR2_DQS_DP[14]
G2	RSVD
G20	RSVD
G22	RSVD
G24	DDR2_DQS_DN[13]
G26	VSS
G28	VCCD012
G30	DDR2_ODT[1]
G32	DDR2_ODT[0]
G34	DDR2_RAS_N_MA[16]
G36	DDR2_BA1
G38	DDR2_CLK_DP[0]
G4	VSS
G40	DDR2_MA[2]
G42	VCCD012
G46	DDR2_MA[4]
G48	DDR2_MA[6]
G50	DDR2_MA[11]
G52	DDR2_BG1
G54	VSS
G56	VSS
G58	RSVD
G6	DDR2_DQS_DP[16]

Table 2-2. Lands by Number (Sheet 80 of 94)

Land No.	Land Name
G60	RSVD
G62	VSS
G64	RSVD
G66	RSVD
G68	RSVD
G70	RSVD
G72	CD_HFI0_RESET_N
G74	VSS
G76	CD_TCLK
G78	CD_HFI0_I2CCLK
G8	VSS
G80	VSS
G82	RSVD
G84	VSS
H1	RSVD
H11	DDR2_DQ[55]
H13	DDR2_DQ[49]
H15	VSS
H17	DDR2_DQ[47]
H19	DDR2_DQ[41]
H21	VSS
H23	DDR2_DQ[39]
H25	DDR2_DQ[33]
H27	VSS
H29	DDR2_C0_CS_N[2]
H3	VSS
H31	DDR2_CS_N[1]
H33	DDR2_WE_N_MA[14]
H35	DDR2_AP_MA[10]
H37	DDR2_CLK_DN[0]
H39	DDR2_MA[1]
H41	DDR2_MA[3]
H43	VCCD012
H45	VCCD012
H47	DDR2_MA[5]
H49	DDR2_MA[7]
H5	DDR2_DQ[62]
H51	DDR2_ALERT_N
H53	DDR2_CKE[0]

Table 2-2. Lands by Number (Sheet 81 of 94)

Land No.	Land Name
H55	VSS
H57	VSS
H59	RSVD
H61	VSS
H63	VSS
H65	RSVD
H67	RSVD
H69	RSVD
H7	DDR2_DQ[57]
H71	RSVD
H73	VSS
H75	VSS
H77	CD_HFI0_I2CDAT
H79	VSS
H81	VSS
H83	VSS
H85	VSS
H9	VSS
J10	DDR2_DQ[54]
J12	DDR2_DQS_DP[15]
J14	DDR2_DQ[48]
J16	DDR2_DQ[46]
J18	DDR2_DQS_DN[14]
J2	VSS
J20	DDR2_DQ[40]
J22	DDR2_DQ[38]
J24	DDR2_DQS_DP[13]
J26	DDR2_DQ[32]
J28	VCCD012
J30	VCCD012
J32	VCCD012
J34	VCCD012
J36	VCCD012
J38	VCCD012
J4	DDR2_DQ[63]
J40	VCCD012
J42	VCCD012
J46	VCCD012
J48	VCCD012

Table 2-2. Lands by Number (Sheet 82 of 94)

Land No.	Land Name
J50	VCCD012
J52	VCCD012
J54	VSS
J56	DDR2_DQS_DN[17]
J58	VSS
J6	DDR2_DQS_DN[16]
J60	VSS
J62	DDR2_DQS_DP[12]
J64	VSS
J66	VSS
J68	DDR2_DQS_DN[11]
J70	VSS
J72	VSS
J74	DDR2_DQS_DP[10]
J76	VSS
J78	VSS
J8	DDR2_DQ[56]
J80	DDR2_DQS_DN[9]
J82	VSS
J84	RSVD
J86	RSVD
K1	RSVD
K11	VSS
K13	VSS
K15	VSS
K17	VSS
K19	VSS
K21	VSS
K23	VSS
K25	VSS
K27	VSS
K29	DDR1_C1_CS_N[3]
K3	VSS
K31	DDR1_CS_N[1]
K33	DDR1_WE_N_MA[14]
K35	DDR1_AP_MA[10]
K37	DDR1_PAR
K39	DDR1_CLK_DN[0]
K41	DDR1_MA[5]

Table 2-2. Lands by Number (Sheet 83 of 94)

Land No.	Land Name
K43	VCCD012
K45	VCCD012
K47	DDR1_MA[9]
K49	DDR1_BG0
K5	VSS
K51	DDR1_CKE[1]
K53	VSS
K55	DDR2_ECC[7]
K57	DDR2_ECC[1]
K59	VSS
K61	DDR2_DQ[31]
K63	DDR2_DQ[25]
K65	VSS
K67	DDR2_DQ[23]
K69	DDR2_DQ[17]
K7	VSS
K71	VSS
K73	DDR2_DQ[15]
K75	DDR2_DQ[9]
K77	VSS
K79	DDR2_DQ[7]
K81	DDR2_DQ[1]
K83	VSS
K85	VSS
K9	VSS
L10	DDR2_DQ[51]
L12	DDR2_DQS_DN[6]
L14	DDR2_DQ[53]
L16	DDR2_DQ[43]
L18	DDR2_DQS_DP[5]
L2	RSVD
L20	DDR2_DQ[44]
L22	DDR2_DQ[35]
L24	DDR2_DQS_DN[4]
L26	DDR2_DQ[36]
L28	RSVD
L30	DDR1_ODT[1]
L32	DDR1_ODT[0]
L34	DDR1_RAS_N_MA[16]

Table 2-2. Lands by Number (Sheet 84 of 94)

Land No.	Land Name
L36	DDR1_MA[0]
L38	DDR1_CLK_DP[0]
L4	DDR2_DQ[58]
L40	DDR1_MA[2]
L42	VCCD012
L46	DDR1_MA[8]
L48	DDR1_BC_N_MA[12]
L50	DDR1_ACT_N
L52	VCCD012
L54	DDR2_ECC[6]
L56	DDR2_DQS_DP[17]
L58	DDR2_ECC[0]
L6	DDR2_DQS_DP[7]
L60	DDR2_DQ[30]
L62	DDR2_DQS_DN[12]
L64	DDR2_DQ[24]
L66	DDR2_DQ[22]
L68	DDR2_DQS_DP[11]
L70	DDR2_DQ[16]
L72	DDR2_DQ[14]
L74	DDR2_DQS_DN[10]
L76	DDR2_DQ[8]
L78	DDR2_DQ[6]
L8	DDR2_DQ[60]
L80	DDR2_DQS_DP[9]
L82	DDR2_DQ[0]
L84	RSVD
L86	RSVD
M1	RSVD
M11	DDR2_DQ[50]
M13	DDR2_DQ[52]
M15	VSS
M17	DDR2_DQ[42]
M19	DDR2_DQ[45]
M21	VSS
M23	DDR2_DQ[34]
M25	DDR2_DQ[37]
M27	VSS
M29	VCCD012

Table 2-2. Lands by Number (Sheet 85 of 94)

Land No.	Land Name
M3	VSS
M31	VCCD012
M33	VCCD012
M35	VCCD012
M37	VCCD012
M39	VCCD012
M41	VCCD012
M43	VCCD012
M45	VCCD012
M47	VCCD012
M49	VCCD012
M5	DDR2_DQ[59]
M51	VCCD012
M53	VSS
M55	VSS
M57	VSS
M59	VSS
M61	VSS
M63	VSS
M65	VSS
M67	VSS
M69	VSS
M7	DDR2_DQ[61]
M71	VSS
M73	VSS
M75	VSS
M77	VSS
M79	VSS
M81	VSS
M83	VSS
M85	RSVD
M9	VSS
N10	VSS
N12	DDR2_DQS_DP[6]
N14	VSS
N16	VSS
N18	DDR2_DQS_DN[5]
N2	VSS
N20	VSS

Table 2-2. Lands by Number (Sheet 86 of 94)

Land No.	Land Name
N22	VSS
N24	DDR2_DQS_DP[4]
N26	VSS
N28	VCCD012
N30	DDR1_C2
N32	DDR1_MA[13]
N34	DDR1_CS_N[0]
N36	DDR1_BA1
N38	DDR1_CLK_DN[2]
N4	VSS
N40	DDR1_MA[3]
N42	VCCD012
N46	DDR1_MA[6]
N48	DDR1_MA[11]
N50	DDR1_BG1
N52	RSVD
N54	DDR2_ECC[3]
N56	DDR2_DQS_DN[8]
N58	DDR2_ECC[5]
N6	DDR2_DQS_DN[7]
N60	DDR2_DQ[27]
N62	DDR2_DQS_DP[3]
N64	DDR2_DQ[28]
N66	DDR2_DQ[19]
N68	DDR2_DQS_DN[2]
N70	DDR2_DQ[21]
N72	DDR2_DQ[11]
N74	DDR2_DQS_DP[1]
N76	DDR2_DQ[12]
N78	DDR2_DQ[3]
N8	VSS
N80	DDR2_DQS_DN[0]
N82	DDR2_DQ[4]
N84	RSVD
N86	RSVD
P1	VSS
P11	VSS
P13	VSS
P15	DDR1_DQS_DP[14]

Table 2-2. Lands by Number (Sheet 87 of 94)

Land No.	Land Name
P17	VSS
P19	VSS
P21	DDR1_DQS_DN[13]
P23	VSS
P25	VSS
P27	RSVD
P29	DDR1_C0_CS_N[2]
P3	DDR1_DQS_DP[16]
P31	DDR1_MA[17]
P33	DDR1_CAS_N_MA[15]
P35	DDR1_BA0
P37	DDR1_CLK_DP[2]
P39	DDR1_MA[1]
P41	DDR1_MA[4]
P43	VCCD012
P45	VCCD012
P47	DDR1_MA[7]
P49	DDR1_ALERT_N
P5	VSS
P51	DDR1_CKE[0]
P53	VSS
P55	DDR2_ECC[2]
P57	DDR2_ECC[4]
P59	VSS
P61	DDR2_DQ[26]
P63	DDR2_DQ[29]
P65	VSS
P67	DDR2_DQ[18]
P69	DDR2_DQ[20]
P7	VSS
P71	VSS
P73	DDR2_DQ[10]
P75	DDR2_DQ[13]
P77	VSS
P79	DDR2_DQ[2]
P81	DDR2_DQ[5]
P83	VSS
P85	RSVD
P9	DDR1_DQS_DN[15]

Table 2-2. Lands by Number (Sheet 88 of 94)

Land No.	Land Name
R10	DDR1_DQ[49]
R12	VSS
R14	DDR1_DQ[47]
R16	DDR1_DQ[41]
R18	VSS
R2	DDR1_DQ[63]
R20	DDR1_DQ[39]
R22	DDR1_DQ[33]
R24	VSS
R26	RSVD
R28	VSS
R30	VCCD012
R32	VCCD012
R34	VCCD012
R36	VCCD012
R38	VCCD012
R4	DDR1_DQ[57]
R40	VCCD012
R42	VCCD012
R46	VCCD012
R48	VCCD012
R50	VCCD012
R52	VCCD012
R54	VSS
R56	DDR2_DQS_DP[8]
R58	VSS
R6	VSS
R60	VSS
R62	DDR2_DQS_DN[3]
R64	VSS
R66	VSS
R68	DDR2_DQS_DP[2]
R70	VSS
R72	VSS
R74	DDR2_DQS_DN[1]
R76	VSS
R78	VSS
R8	DDR1_DQ[55]
R80	DDR2_DQS_DP[0]

Table 2-2. Lands by Number (Sheet 89 of 94)

Land No.	Land Name
R82	VSS
R84	VSS
R86	RSVD
T1	DDR1_DQ[62]
T11	DDR1_DQ[48]
T13	DDR1_DQ[46]
T15	DDR1_DQS_DN[14]
T17	DDR1_DQ[40]
T19	DDR1_DQ[38]
T21	DDR1_DQS_DP[13]
T23	DDR1_DQ[32]
T25	VSS
T27	RSVD
T29	DDR0_C1_CS_N[3]
T3	DDR1_DQS_DN[16]
T31	DDR0_CS_N[1]
T33	DDR0_WE_N_MA[14]
T35	DDR0_AP_MA[10]
T37	DDR0_PAR
T39	DDR0_CLK_DN[0]
T41	DDR0_MA[5]
T43	VCCD012
T45	VCCD012
T47	DDR0_MA[9]
T49	DDR0_BG0
T5	DDR1_DQ[56]
T51	DDR0_CKE[1]
T53	CD_HFI1_MODPRST_N
T55	VSS
T57	VSS
T59	DDR1_DQS_DN[17]
T61	VSS
T63	VSS
T65	DDR1_DQS_DP[12]
T67	VSS
T69	VSS
T7	DDR1_DQ[54]
T71	DDR1_DQS_DN[11]
T73	VSS

Table 2-2. Lands by Number (Sheet 90 of 94)

Land No.	Land Name
T75	VSS
T77	DDR1_DQS_DP[10]
T79	VSS
T81	VSS
T83	DDR1_DQS_DN[9]
T85	VSS
T9	DDR1_DQS_DP[15]
U10	VSS
U12	VSS
U14	VSS
U16	VSS
U18	VSS
U2	VSS
U20	VSS
U22	VSS
U24	VSS
U26	RSVD
U28	VSS
U30	DDR0_ODT[1]
U32	DDR0_ODT[0]
U34	DDR0_RAS_N_MA[16]
U36	DDR0_MA[0]
U38	DDR0_CLK_DP[0]
U4	VSS
U40	DDR0_MA[2]
U42	VCCD012
U46	DDR0_MA[8]
U48	DDR0_BC_N_MA[12]
U50	DDR0_ACT_N
U52	DDR012_RESET_N
U54	CD_HFI1_INT_N
U56	VSS
U58	DDR1_ECC[7]
U6	VSS
U60	DDR1_ECC[1]
U62	VSS
U64	DDR1_DQ[31]
U66	DDR1_DQ[25]
U68	VSS

Table 2-2. Lands by Number (Sheet 91 of 94)

Land No.	Land Name
U70	DDR1_DQ[23]
U72	DDR1_DQ[17]
U74	VSS
U76	DDR1_DQ[15]
U78	DDR1_DQ[9]
U8	VSS
U80	VSS
U82	DDR1_DQ[7]
U84	DDR1_DQ[1]
U86	VSS
V1	DDR1_DQ[59]
V11	DDR1_DQ[53]
V13	DDR1_DQ[43]
V15	DDR1_DQS_DP[5]
V17	DDR1_DQ[44]
V19	DDR1_DQ[35]
V21	DDR1_DQS_DN[4]
V23	DDR1_DQ[36]
V25	VSS
V27	RSVD
V29	VCCD012
V3	DDR1_DQS_DP[7]
V31	VCCD012
V33	VCCD012
V35	VCCD012
V37	VCCD012
V39	VCCD012
V41	VCCD012
V43	VCCD012
V45	VCCD012
V47	VCCD012
V49	VCCD012
V5	DDR1_DQ[60]
V51	VCCD012
V53	VCCD012
V55	CD_HFI1_I2CDAT
V57	DDR1_ECC[6]
V59	DDR1_DQS_DP[17]
V61	DDR1_ECC[0]

Table 2-2. Lands by Number (Sheet 92 of 94)

Land No.	Land Name
V63	DDR1_DQ[30]
V65	DDR1_DQS_DN[12]
V67	DDR1_DQ[24]
V69	DDR1_DQ[22]
V7	DDR1_DQ[51]
V71	DDR1_DQS_DP[11]
V73	DDR1_DQ[16]
V75	DDR1_DQ[14]
V77	DDR1_DQS_DN[10]
V79	DDR1_DQ[8]
V81	DDR1_DQ[6]
V83	DDR1_DQS_DP[9]
V85	DDR1_DQ[0]
V9	DDR1_DQS_DN[6]
W10	DDR1_DQ[52]
W12	VSS
W14	DDR1_DQ[42]
W16	DDR1_DQ[45]
W18	VSS
W2	DDR1_DQ[58]
W20	DDR1_DQ[34]
W22	DDR1_DQ[37]
W24	VSS
W26	VSS
W28	VSS
W30	DDR0_C2
W32	DDR0_MA[13]
W34	DDR0_CS_N[0]
W36	DDR0_BA1
W38	DDR0_CLK_DN[2]
W4	DDR1_DQ[61]
W40	DDR0_MA[3]
W42	VCCD012
W46	DDR0_MA[6]
W48	DDR0_MA[11]
W50	DDR0_BG1
W52	DDR012_MEMHOT_N
W54	CD_HFI1_LED_N
W56	VSS

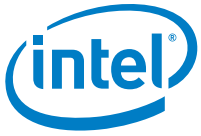


Table 2-2. Lands by Number (Sheet 93 of 94)

Land No.	Land Name
W58	VSS
W6	VSS
W60	VSS
W62	VSS
W64	VSS
W66	VSS
W68	VSS
W70	VSS
W72	VSS
W74	VSS
W76	VSS
W78	VSS
W8	DDR1_DQ[50]
W80	VSS
W82	VSS
W84	VSS
W86	VSS
Y1	VSS
Y11	VSS
Y13	VSS
Y15	DDR1_DQS_DN[5]
Y17	VSS
Y19	VSS
Y21	DDR1_DQS_DP[4]
Y23	VSS
Y25	VSS
Y27	VSS
Y29	DDR0_C0_CS_N[2]
Y3	DDR1_DQS_DN[7]
Y31	DDR0_MA[17]
Y33	DDR0_CAS_N_MA[15]
Y35	DDR0_BA0
Y37	DDR0_CLK_DP[2]
Y39	DDR0_MA[1]
Y41	DDR0_MA[4]
Y43	VCCD012
Y45	VCCD012
Y47	DDR0_MA[7]
Y49	DDR0_ALERT_N

Table 2-2. Lands by Number (Sheet 94 of 94)

Land No.	Land Name
Y5	VSS
Y51	DDR0_CKE[0]
Y53	DDR012_VREFCA
Y55	CD_HFI1_I2CCLK
Y57	DDR1_ECC[3]
Y59	DDR1_DQS_DN[8]
Y61	DDR1_ECC[5]
Y63	DDR1_DQ[27]
Y65	DDR1_DQS_DP[3]
Y67	DDR1_DQ[28]
Y69	DDR1_DQ[19]
Y7	VSS
Y71	DDR1_DQS_DP[2]
Y73	DDR1_DQ[21]
Y75	DDR1_DQ[11]
Y77	DDR1_DQS_DP[1]
Y79	DDR1_DQ[12]
Y81	DDR1_DQ[3]
Y83	DDR1_DQS_DN[0]
Y85	DDR1_DQ[4]
Y9	DDR1_DQS_DP[6]

§

3.0 Processor Signal Descriptions

This chapter describes the processor signals, which are arranged in functional groups according to their associated interface or category. Signal groups include DDR4, PCI Express*, DMI2, fabric, Platform Environmental Control Interface (PECI), system reference clock, SMBus, JTAG and Test Access Port (TAP), SVID interface, processor asynchronous sideband, miscellaneous, and power/other signals.

3.1 Processor Signal Buffer Types

The processor utilizes various signaling technologies. Signal electrical characteristics and buffer types are listed in Table 3-1. The buffer type indicates which signaling technology and specifications apply to the signals.

Note: In the tables that follow, the direction (input and/or output) of a signal is given with respect to the CPU.

Table 3-1. Signal Buffer Types

Signal	Description
Analog	Analog reference or output. May be used as a threshold voltage or for buffer compensation.
Asynchronous[1]	Signal has no timing relationship with any system reference clock.
CMOS_10	CMOS buffers: 1.0V level
CMOS_12	CMOS buffers: 1.2V level
CMOS_18	CMOS buffers: 1.8V level
CMOS_25	CMOS buffers: 2.5V level
OD_10	Open Drain buffers: 1.0V level
OD_25	Open Drain buffers: 2.5V level
OS_10	Open Source buffers: 1.0V level
HCSL	High-Speed Current Steering Logic
DMI2	Direct Media Interface Gen 2 signals. These signals are compatible with PCI Express* 2.0 and 1.0 Signaling Environment AC Specifications and are AC coupled.
PCIE3	PCI Express Gen 3 interface signals. These signals are compatible with PCI Express 3.0 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3V tolerant.
PCIE3CLK	100 MHz PCIe* 3.0 specification compliant differential reference clock
SSTL_12	Stub Series Terminated Logic: 1.2V level
POD_12	Pseudo Open Drain: 1.2V level

Notes:
1. Qualifier for a buffer type

3.2 Internal Pull Ups/Pull Downs

Table 3-2 lists the signals with on-die pull ups/pull downs.

Table 3-2. Signals with Weak Pull Up/pull Down on Silicon

Signal Name	Pull Up/Pull Down	Rail	Value	Unit	Notes
DEBUG_EN_N	PU	VCCU	5k-15k	Ω	
EAR_N	PU	VCCU	5k-15k	Ω	
CATERR_N	PU	VCCU	5k-15k	Ω	
PRDY_N	PU	VCCU	5k-15k	Ω	
PREQ_N	PU	VCCU	5k-15k	Ω	
TCK	PD	GND	5k-15k	Ω	
TDI	PU	VCCU	5k-15k	Ω	
TRST_N	PU	VCCU	5k-15k	Ω	
TMS	PU	VCCU	5k-15k	Ω	
TEST[27]	PD	GND	5k-15k	Ω	
TEST[29]	PD	GND	5k-15k	Ω	
TEST[30]	PU	VCCU	5k-15k	Ω	
TEST[31]	PD	GND	5k-15k	Ω	
TEST[32]	PD	GND	5k-15k	Ω	
CD_TCLK	PD	GND	25k-50k	Ω	
CD_TDI	PU	VCCH_1P8	25k-50k	Ω	
CD_TMS	PU	VCCH_1P8	25k-50k	Ω	
CD_TRST_N	PD	GND	25k-50k	Ω	

3.3 System Memory Interface

The system memory interface utilizes DDR4 technology, which consists of numerous signal groups. These include: command signals, control signals, and data signals. Each group consists of numerous signals, which may utilize various signaling technologies. See Table 3-3. Throughout this document the system memory interface may be referred to as DDR4.

Board and platform designers can find further DDR4 signal naming, description, and board routing recommendations provided in the DDR4 SDRAM Specification, the DDR4 RDIMM Design Specification and Raw Card Annexes, and the DDR4 LRDIMM Design Specification and Raw Card Annexes available on the JEDEC website.

Table 3-3. DDR4 Memory Channels 0-5 Signals (Sheet 1 of 2)

Signal Name	Direction (Buffer)	Description
DDR4 memory bus signal names are preceded by the prefix: DDR{0/1/2/3/4/5}_, e.g., DDR0_ACT_N.		
DQ[63:0]	Input/Output (POD_12)	Memory data bus, six separate channels
ALERT_N	Input (POD_12)	Indicates a parity error has been detected.
ACT_N	Output (SSTL_12)	Activation Command Input. Used when a row activate command is sent to the DRAM.
AP_MA[10]		Multi-function pin. Memory address 10 and auto pre-charge.
BC_N_MA[12]		Multi-function pin. Memory address 12 and burst chop.
ECC[7:0]		Error Correction Code data for each byte
MA[17, 13, 11, 9:0]		Memory Address. Selects the row address for activate commands and the column address for reads and writes. Also used to set values for DRAM configuration registers.
WE_N_MA[14]		Multi-function pin. Write enable and memory address 14.
BA[1:0]		Bank Address. Defines the bank which is the destination for the current active, read, write, or precharge command. Also used to determine the mode register to be accessed during an MRS cycle.
BG[1:0]		Bank Group. Defines which bank group is the destination for an active, read, write or precharge command. Also used to determine the mode register to be accessed during an MRS cycle.
C0_CS_N[2] C1_CS_N[3] C2	Output (SSTL_12)	Chip ID. Used only for 3DS memory (2, 4 or 8 high stacked die) to select each specific die in a stacked component.
CAS_N_MA[15]		Multi-function pin. Column address strobe and memory address 15.
CKE[1:0]		Clock Enable
CS_N[1:0]		Chip Select. Each signal selects one rank as the target of the command and address.
ODT[1:0]		On Die Termination. Enables DRAM on die termination during read or write transactions.
PAR		Address and command parity for data written to memory
RAS_N_MA[16]		Multi-function pin. Row address strobe and memory address 16.
CLK_D{N/P}[0, 2]	Output (SSTL_12)	Differential clocks. All address and control signals are valid on the crossing of the rising edge of CLK_DP and the falling edge of CLK_DN.
DQS_D{N/P}[17:0]	Input / Output (POD_12)	Differential pair data strobes. Strobes latch data into each DRAM. Driven with edges in center of data.

Table 3-3. DDR4 Memory Channels 0-5 Signals (Sheet 2 of 2)

Signal Name	Direction (Buffer)	Description
DDR4 Sideband Signal Names		
DDR012_DRAM_PWR_OK DDR345_DRAM_PWR_OK	Input (CMOS_10)	Power Good input to the processor indicates that the VCCD power supply is stable for channels 0, 1 and 2 and channels 3, 4 and 5.
DDR012_MEMHOT_N DDR345_MEMHOT_N	Input (CMOS_10) / Output (OD_10)	Is an input to the processor from the host platform and indicates a DDR4 memory voltage regulator has exceeded its maximum temperature. When activated, the processor will limit the memory activity in order to reduce memory power dissipation. MEMHOT is generated by the BMC, or other logic, on the host platform.
DDR012_RCOMP[2:0] DDR345_RCOMP[2:0]	Input (Analog)	Compensation resistors for DDR4 voltage settings
DDR012_RESET_N DDR345_RESET_N	Output (CMOS_12)	Memory Reset. Reset signal from processor to DRAMs. DDR012_RESET is use for channels 0, 1 and 2. DDR345 is used for channels 3, 4 and 5.
DDR012_VREFCA DDR345_VREFCA	Output (Analog)	Voltage reference for memory command and address
DDR4 Memory Module SMBus Signal Names		
SPDSCL0	Input (CMOS_10) / Output (OD_10)	Memory module SMBus clock
SPDSDA0		Memory module SMBus data

3.4 PCI Express Based Interface Signals

The PCI Express Signal Group consists of PCI Express ports P1, P2, P3 and PCI Express miscellaneous signals as listed in Table 3-4.

PCI Express Ports 1, 2 and 3 signals are receive and transmit differential pairs.

Table 3-4. PCI Express Port Signals (Sheet 1 of 2)

Signal Name	Direction (Buffer)	Description
PCI Express* bus signal names are preceded by the prefix: PE{1, 2, 3}{A, B, C, D}_, and are aggregated in groups of four differential pairs, e.g., PE1A_RX_N[3:0].		
PCIe* Port 1 includes 8 lanes at the processor pin level, but only the first 4 lanes (PE1A_) are exposed at the platform level. Port PE1A remains available for expansion cards when a processor with fabric is installed. *Port PE1B is not implemented in current generation processors, only 36 lanes are available.*		
PE1A_RX_{N/P}[3:0] PE1B_RX_{N/P}[7:4]	Input (PCIE3)	Differential PCI Express Receive Data Input
PE1A_TX_{N/P}[3:0] PE1B_TX_{N/P}[7:4]	Output (PCIE3)	Differential PCI Express Transmit Data Output
PCIe Ports 2 and 3 are each 16 lanes wide. These ports are exposed to the platform for processors that do not include integrated fabric. Processors with fabric do not expose these pins at the platform level.		

Table 3-4. PCI Express Port Signals (Sheet 2 of 2)

Signal Name	Direction (Buffer)	Description
PE{2/3}A_RX_{N/P}[3:0] PE{2/3}B_RX_{N/P}[7:4] PE{2/3}C_RX_{N/P}[11:8] PE{2/3}D_RX_{N/P}[15:12]	Input (PCIE3)	Differential PCI Express Receive Data Input
PE{2/3}A_TX_{N/P}[3:0] PE{2/3}B_TX_{N/P}[7:4] PE{2/3}C_TX_{N/P}[11:8] PE{2/3}D_TX_{N/P}[15:12]	Output (PCIE3)	Differential PCI Express Transmit Data Output
PE_REFCLK_D{N/P}	Input (PCIE3CLK)	Differential 100 MHz PCIe clock

3.5 DMI2 Signals

The Direct Media Interface Gen 2 (DMI2) sends and receives packets and commands to the PCH. The DMI2 is an extension of the standard PCI Express specification. The DMI2 port consist of DMI2 receive and transmit input/output signals. Refer to Table 3-5.

DMI signals are receive and transmit differential pairs.

Table 3-5. DMI2 Signals

Signal Name	Direction (Buffer)	Description
DMI_RX_D{N/P}[3:0]	Input (DMI2)	Differential DMI Gen2 Receive Data Input, receives data from the PCH
DMI_TX_D{N/P}[3:0]	Output (DMI2)	Differential DMI Gen2 Transmit Data Output, sends data to the PCH

3.6 Fabric Component Signals

Table 3-6 lists the fabric controller die's sideband signals, which are brought down to the baseboard through lands on the processor with fabric's package.

Note: The fabric controller die is also known as the Companion Die (CD).

Table 3-6. Fabric Component Signals (Sheet 1 of 2) (Sheet 1 of 2)

Signal Name	Direction (Buffer)	Description
CD_HFI_REFCLK_D{N/P}	Input (HCSL)	156.25 MHz differential oscillator inputs. The differential clock pair provides the fundamental clock source for the integrated fabric component.
CD_PE_REFCLK_D{N/P}	Input (PCIE3CLK)	100MHz fabric PCIe* reference clock. A differential pair.
CD_HFI{0/1}_I2CCLK	Input (CMOS_25) / Output (OD_25)	Port {0/1} I^2C clock
CD_HFI{0/1}_I2CDAT	Input (CMOS_25) / Output (OD_25)	Port {0/1} I^2C data
CD_HFI{0/1}_INT_N	Input (CMOS_25)	Port {0/1} interrupt
CD_HFI{0/1}_LED_N	Output (OD_25)	Port {0/1} indicator LED
CD_HFI{0/1}_MODPRST_N	Input (CMOS_25)	Port {0/1} Module (or cable) Present Indicator

Table 3-6. Fabric Component Signals (Sheet 2 of 2) (Sheet 2 of 2)

Signal Name	Direction (Buffer)	Description
CD_HFI{0/1}_RESET_N	Output (OD_25)	Port {0/1} Reset
CD_PERST_N	Input (CMOS_25)	Reset signal to the fabric component.
CD_PRESENT_N	Output (N/A)	Indicates that the fabric component is present in the processor package (i.e., indicates that a processor with fabric is present), by being pulled to ground.
CD_TCLK	Input (CMOS_18)	JTAG test clock[1]
CD_TDI	Input (CMOS_18)	JTAG test data in[1]
CD_TDO	Output (CMOS_18)	JTAG test data out[1]
CD_TMS	Input (CMOS_18)	JTAG test mode select[1]
CD_TRST_N	Input (CMOS_18)	JTAG reset[1]

Notes:
1. These JTAG signals are for the fabric controller die on a processor with fabric multi-chip package. They compose a different interface than those for the processor die, described later in Section 3.9.

3.7 PECI Signal

The Platform Environment Control Interface (PECI) is an Intel proprietary interface that provides a communication channel between the processor (CPU) and the Platform Controller Hub (PCH) or the Baseboard Management Controller (BMC) using single-wire mode. PECI provides an interface for external devices to read processor temperature, perform processor manageability functions, and manage processor interface tuning and diagnostics. The PECI signal is further described in Table 3-7.

Table 3-7. PECI Signals

Signal Name	Direction (Buffer)	Description
PECI	Input (CMOS_10) / Output (OS_10)	Platform Environment Control Interface (PECI) is the serial sideband interface to the processor and is used primarily for thermal, power and error management.

Examples of PECI implementation and usage include access by external system management logic and thermal monitoring devices. The Intel® Xeon Phi™ Processor x200 Product Family processor contains Digital Thermal Sensors (DTS) that report relative die temperature as an offset from Thermal Control Circuit (TCC) activation temperature. Temperature sensors are located throughout the package and are implemented as analog-to-digital converters calibrated at the factory. PECI allows a way to monitor these sensors.

3.8 System Reference Clock Signals

The processor core, processor uncore, OPIO interface, and DDR4 interface operating frequencies are generated from BCLK_DP and BCLK_DN signals, as described in Table 3-8.

Clock multiplying within the processor is provided by the internal phase locked loop (PLL), which requires a constant frequency BCLK_DP, BCLK_DN input, with exceptions for spread spectrum clocking. DC specifications for the BCLK_DP, BCLK_DN inputs are provided in Section 5.1.7. These specifications must be met while also meeting the associated signal quality specifications outlined in Section 5.2.

Table 3-8. System Reference Clock (BCLK0) Signals

Signal Name	Direction (Buffer)	Description
BCLK0_D{N/P}	Input (PCIE3CLK)	Reference Clock Differential input. These pins provide the PLL reference clock differential input into the processor. This is a 100 MHz clock.

3.9 JTAG and TAP Signals

Table 3-9 lists the processor die's JTAG and TAP signals. Due to the voltage levels supported by other components in the JTAG and Test Access Port (TAP) logic, Intel recommends the processor be first in the TAP chain, followed by any other components within the system. A voltage translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Two copies of each signal may be required with each driving a different voltage level.

Table 3-9. JTAG and TAP Signals (Sheet 1 of 2)

Signal Name	Direction (Buffer)	Description
BPM_N[7:0]	Input (CMOS_10) / Output (OD_10)	Breakpoint Monitor Signals: I/O signals from the processor that indicates the status of breakpoints and programmable counters used for monitoring processor performance. These are 100 MHz signals.
DEBUG_EN_N	Input (CMOS_10)	This pin is used to enable certain features used by ITP (e.g., probe mode). This pin should be connected to the ITP XDP_PRESENT_N signal (see the PDG for details) as a security measure to validate user physical access to the target platform. 0 = Enable features 1 = Disable features
EAR_N	Input (CMOS_10)	External Alignment of Reset, used to bring the processor up into a deterministic state. This signal is pulled up on the die. 0 = Reset flow will be halted 1 = Normal mode (no alignment) 0->1: Aligns reset to global alignment point
OBS[15:0]	Input (CMOS_10) / Output (CMOS_10)	Data signals between the processor and debug tool
OBSSTB_{N/P}[1:0]	Output (CMOS_10)	Differential XDP Data signal strobes
PRDY_N	Output (OD_10)	Probe Mode Ready is a processor output used by debug tools to determine processor debug readiness.
PREQ_N	Input (CMOS_10)	Probe Mode Request is used by debug tools to request debug operation of the processor.
TCK	Input (CMOS_10)	Test Clock provides the clock input for the processor test bus (also known as the test access port).

Table 3-9. JTAG and TAP Signals (Sheet 2 of 2)

Signal Name	Direction (Buffer)	Description
TDI	Input (CMOS_10)	Test Data In transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output (OD_10)	Test Data Out transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TMS	Input (CMOS_10)	Test Mode Select is a JTAG specification support signal used by debug tools.
TRST_N	Input (CMOS_10)	Test Reset resets the Test Access Port (TAP) logic. TRST_N must be driven low during power-on Reset.

3.10 Serial VID Interface (SVID) Signals

Table 3-10 lists the signals that the processor uses to communicate with its key voltage regulators on the baseboard.

Table 3-10. SVID Signals

Signal Name	Direction (Buffer)	Description
SVIDALERT_N	Input (CMOS_10)	Serial VID alert
SVIDCLK	Output (OD_10)	Serial VID clock
SVIDDATA	Input (CMOS_10) / Output (OD_10)	Serial VID data

3.11 Processor Asynchronous Sideband and Miscellaneous Signals

The processor includes asynchronous sideband signals that provide asynchronous input, output, or I/O signals between the processor and the platform or platform controller hub. See Table 3-11 and the applicable platform design guide for details.

Refer to Section 5.1.10 for the DC specifications, and Section 5.2 for applicable signal integrity specifications.

Table 3-11. Processor Asynchronous Sideband and Miscellaneous Signals (Sheet 1 of 2)

Signal Name	Direction (Buffer)	Description
BIST_ENABLE[1]	Input (CMOS_10)	Input which allows the platform to enable or disable Built-In Self Test (BIST) on the processor. This strap is latched during all reset modes. 0 = CPU will NOT execute LLC and MLC BIST. 1 = CPU will execute LLC and MLC BIST.
CATERR_N	Output (OD_10)	Indicates that the system has experienced a fatal or catastrophic error and cannot continue to operate. The processor will assert CATERR_N for non-recoverable machine check errors and other internal unrecoverable errors. Since this pin is bi-directional, external agents are allowed to assert this signal which will cause the processor to take a machine check exception. CATERR_N is used for signaling the following types of errors: • Legacy MCERRs, CATERR_N is asserted for 16 BCLKs, and samples it for 28 BCLKs to determine if it is driven by an external agent indicating a fatal or uncorrected error. • Legacy IERRs, CATERR_N remains asserted until warm or cold reset.
CPUPWRGD	Input (CMOS_10)	Power Good input signal. Active high. The processor requires this signal to be a clean indication that all processor clocks and power supplies are stable and within their specifications. "Clean" implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. CPUPWRGD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of CPUPWRGD. The signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
ERROR_N[2:0]	Output (OD_10)	Error status signals for integrated I/O (IIO) unit: 0: Hardware correctable error (no operating system or firmware action necessary) 1: Nonfatal error (operating system or firmware action required to contain and recover) 2: Fatal error (system reset likely required to recover)
PMSYNC	Input (CMOS_10)	Power Management Sync. A sideband signal to communicate power management status from the Platform Controller Hub (PCH) to the processor.
PROCHOT_N	Input (CMOS_10) / Output (OD_10)	PROCessor HOT. This signal can also be driven to the processor to activate the Thermal Control Circuit. Upon assertion of PROCHOT_N the processor will lower its operating frequency to reduce power dissipation and consequently, temperature. If PROCHOT_N is asserted at the deassertion of RESET_N, the processor will tristate its outputs.
RESET_N	Input (CMOS_10)	Asserting the RESET_N signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents.
RSVD	-	RESERVED. All signals that are RSVD must be left unconnected on the board.

Table 3-11. Processor Asynchronous Sideband and Miscellaneous Signals (Sheet 2 of 2)

Signal Name	Direction (Buffer)	Description
SKTOCC_N	Output (N/A)	SKTOCC_N (Socket occupied) will be pulled to ground in the processor package to indicate that the processor is present. There is no connection to the processor silicon for this signal.
TEST[0] TEST[11:4] TEST[22:13] TEST[32:26]	-	Test signals must be individually connected to an appropriate power source or ground through a resistor for proper processor operation. See Table 3-12.
THERMTRIP_N	Output (OD_10)	Assertion of THERMTRIP_N (Thermal Trip) indicates one of two possible critical over-temperature conditions: One, the processor junction temperature has reached a level beyond which permanent silicon damage may occur; or Two, one or more of the on-package MCDRAMs has indicated to the processor die that they have exceeded the temperature beyond which permanent damage may occur. Measurement of the processor junction temperature is accomplished through multiple internal thermal sensors that are monitored by the Digital Thermal Sensor (DTS). Once activated, the processor will stop all execution and shut down all PLLs. To further protect the processor, all core and memory voltages must be removed following the assertion of THERMTRIP_N. Once activated, THERMTRIP_N remains latched until RESET_N is asserted. While the assertion of the RESET_N signal may de-assert THERMTRIP_N, if the processor's junction temperature remains at or above the trip level, THERMTRIP_N will again be asserted after RESET_N is deasserted. This signal can also be asserted if the system memory interface has exceeded a critical temperature limit set by BIOS.

Notes:
1. Platform should set the default by either pulling this pin high to VCCU through a 249 Ω 1% resistor, or by pulling this pin low to GND through a 249 Ω 1% resistor.

Table 3-12. Required Pull Ups/Pull Downs on the Baseboard (Sheet 1 of 2)

Signal Name[1]	Pull Up/Pull Down	Rail	Value (all 1%)	Unit	Notes
TEST[0]	PD	GND	402	Ω	2, 3, 4, 5, 6
TEST[4]	PD	GND	49.9	Ω	
TEST[5]	PD	GND	49.9	Ω	
TEST[6]	PD	GND	49.9	Ω	
TEST[7]	PD	GND	49.9	Ω	
TEST[8]	PD	GND	49.9	Ω	
TEST[9]	PD	GND	49.9	Ω	
TEST[10]	PD	GND	49.9	Ω	
TEST[11]	PD	GND	49.9	Ω	
TEST[13]	PD	GND	402	Ω	2, 3, 4, 5, 6
TEST[14]	PD	GND	49.9	Ω	
TEST[15]	PD	GND	49.9	Ω	
TEST[16]	PD	GND	49.9	Ω	
TEST[17]	PD	GND	49.9	Ω	
TEST[18]	PD	GND	49.9	Ω	

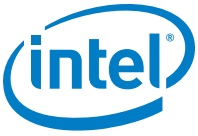


Table 3-12. Required Pull Ups/Pull Downs on the Baseboard (Sheet 2 of 2)

Signal Name[1]	Pull Up/Pull Down	Rail	Value (all 1%)	Unit	Notes
TEST[19]	PD	GND	49.9	Ω	
TEST[20]	PD	GND	49.9	Ω	
TEST[21]	PD	GND	49.9	Ω	
TEST[22]	PD	GND	49.9	Ω	
TEST[26]	PD	GND	0	Ω	

Notes:
1. These signals are used during CPU testing only and must be tied through either a Pull-Up (PU) or Pull-Down (PD) resistor on the platform except where noted.
2. Maximum coupling of -40 dB to VDD/VSS
3. Maximum coupling of -50 dB to other I/O signals
4. Microstrip routing with 5.9 mil trace width and 1 inch maximum length
5. 2h minimum spacing to each other, where "h" is the dielectric height between the signal trace and the closest reference ground plane.
6. 6h minimum spacing with other interfaces

3.12 Processor Power and Ground Supplies

Table 3-13 lists the power and ground supplies required by the processor. The processor power supply specifications are given in Section 4.0.

Table 3-13. Power and Ground Signals (Sheet 1 of 2)

Signal Name	Type	Description
VCCCLR	Processor Power Rails	Powers non-core areas of the processor silicon, e.g., mesh, etc.
VCCIIO		Power supply for processor PCIe* interface
VCCLVR		Processor analog power
VCCP		Processor core voltage
VCCPIO		Processor PCIe power
VCC_CDCORE	Fabric Power Rails	Variable power supply for the processor cores. It is provided by a VRM12 compliant regulator.
VCCE_1P0		Power supply for the fabric component analog I/O
VCCH_1P8		Power supply for fabric component digital I/O
VCCH_2P5		Power supply for fabric component digital I/O
VCCP_1P0		Fabric component PCIe power
VCCD012 VCCD345	DDR4 Power Rails	DDR4 memory channels I/O analog voltage
VCCDDRIO012 VCCDDRIO345		DDR4 memory channels I/O digital voltage
VCCU		Processor DDR4 interface and miscellaneous I/O power

Table 3-13. Power and Ground Signals (Sheet 2 of 2)

Signal Name	Type	Description
VCCMF	MCDRAM Power Rails	Proprietary MCDRAM voltage
VCCMH01, VCCMH23, VCCMH45, VCCMH67		On package MCDRAM power
VCCMIO0123 VCCMIO4567		On package MCDRAM I/O power
VCCMIOQ0123 VCCMIOQ4567		On package MCDRAM I/O power
VCCMLB0123 VCCMLB4567		MCDRAM digital power
VCCMP0123 VCCMP4567		MCDRAM memory power
VCCMPLL01, VCCMPLL23, VCCMPLL45, VCCMPLL67		MCDRAM memory PLL voltage
VCCOPIO01, VCCOPIO23, VCCOPIO45, VCCOPIO67		Powers the interface on the processor to the MCDRAM
VSS	Ground	Ground
VCC_CDCORE_SENSE VSS_VCC_CDCORE_SENSE	Single or Direct Sense	Differential sense line pair for VCC_CDCORE (only on processors with fabric)
VCCCLR_SENSE VSS_VCCCLR_SENSE		Differential sense line pair for VCCCLR
VCCMLB0123_SENSE VCCMLB4567_SENSE VSS_VCCMLB0123_SENSE VSS_VCCMLB4567_SENSE		Differential sense line pair for the MCDRAM voltage
VCCMP0123_SENSE VCCMP4567_SENSE VSS_VCCMP0123_SENSE VSS_VCCMP4567_SENSE		Differential sense line pair for MCDRAM memory power
VCCP_SENSE VSS_VCCP_SENSE		Differential sense line pair for processor core voltage
VCCPIO_SENSE VSS_VCCPIO_SENSE		Differential sense line pair for processor PCIe voltage
VCCU_SENSE VSS_VCCU_SENSE	Dual Sense with Equal Weighting	Differential sense line pair for DDR4 I/O voltage. *This sense pair actually senses VCCDDRIO{012/345}, not VCCU/VCCUQ.*

3.13 Reserved or Unused Pins

All processor reserved (RSVD) pins must be left unconnected. Connection of these signals to power, ground or to any other signal (including each other) can result in component malfunction or incompatibility with future processors.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (VSS). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within ±20% of the impedance of the baseboard trace, unless otherwise noted in the appropriate platform design guidelines.

§

4.0 Processor Power Supply Specifications

This chapter begins with a brief discussion of the Serial Voltage Identification (SVID) interface, and explicit commands and features supported by the processor. The chapter continues with a detailed description of the processor voltage, current and power targets, followed by the power sequence diagrams and absolute voltage ratings.

4.1 Serial Voltage Identification (SVID)

The SVID code interface is a serial interface used by the processor to interact with voltage regulator (VR) controllers. The VR controllers for the VCCP, VCCCLR, VCCU, VCCMLB and VCC_CDCORE processor voltage rails must fully comply with the VR12.0 specification, by implementation either with "pure" VR12.0 controllers or with VR12.5 controllers put in the VR12.0 mode. The VR controllers for the VCCD012 and VCCD345 processor memory voltage rails must fully comply with the VR12.5 Specification.

The reference voltage or the VID setting is set via the SVID communication bus between the processor and the voltage regulator controller chip. The VID settings are the nominal voltages to be delivered to the processor's power lands when current draw equals zero. Table 4-2 specifies the reference voltage level corresponding to the VID value transmitted over serial VID. The voltage will change due to temperature and/or current load changes in order to minimize the power and to maximize the performance of the part. The specifications are set so that a voltage regulator can operate with all supported frequencies.

The processor uses voltage identification signals to support automatic selection of processor power supply voltages. If either the processor socket is empty (SKTOCC_N high) or a "not supported" response is received from the SVID bus, then the voltage regulator must disable itself or not power on. Vout MAX register (30h) is programmed by the processor to set the maximum supported VID code and if the programmed VID code is higher than the VID supported by the VR, then VR will respond with a "not supported" acknowledgment.

4.1.1 SVID Commands

The processor supports the following VR commands:

- 0x1: SetVID-Fast (20 mV/µs), ramps a VR up at the fastest slew rate
- 0x2: SetVID-Slow (5 mV/µs), ramps a VR down at a slower slew rate
- 0x3: SetVID-Decay, ramps a VR down proportional to current (no controlled slew rate)
- 0x4: SetPS, places a VR in a desired power state
- 0x5: SetReg-Addr, sets the register address for the SetReg_Data command
- 0x6: SetReg-Data, writes data to the address specified by SetReg_Addr
- 0x7: GetReg, reads VR registers

Table 4-2 includes SVID step sizes. Minimum and maximum voltages must be maintained as shown in Table 4-4.

4.1.1.1 SetVID-Fast

The SetVID-Fast command contains the target VID in the payload byte. The range of voltage is defined in the VID table. The VR should ramp to the new VID setting with a fast slew rate as defined in the slew rate data register. Typically 20 mV/µS for server platforms.

The SetVID-Fast command is preemptive, the VR interrupts its current processes and moves to the new VID. The SetVID-Fast command operates on 1 VR address at a time. This command is used in the processor for package C6 fast exit.

4.1.1.2 SetVID-Slow

The SetVID-Slow command contains the target VID in the payload byte. The range of voltage is defined in the VID table. The VR should ramp to the new VID setting with a "slow" slew rate as defined in the slow slew rate data register. Typically the SetVID-Slow is 4x slower than the SetVID-Fast slew rate.

The SetVID-Slow command is preemptive, the VR interrupts its current processes and moves to the new VID. This is the instruction used for normal P-State voltage change.

4.1.1.3 SetVID-Decay

The SetVID-Decay command is the slowest of the DVID transitions. It is normally used for VID down transitions. The VR does not control the slew rate, the output voltage declines with the output load current only.

The SetVID-Decay command is preemptive, the VR interrupts its current processes and moves to the new VID. This command is used in the processor for package C6 entry, allowing capacitor discharge by the leakage, thus saving energy. This command is normally used in VID down direction in the processor package C6 entry.

4.1.1.4 SetPS: SVID Power State Functions

The processor has three power state functions and these will be set via the SVID bus using the SetPS command. Based on the power state command, the SetPS command sends information to the VR controller to configure the VR to improve efficiency, especially at light loads. For example, typical power states are:

- PS(00h): Represents full power or active mode
- PS(01h): Represents a light load 5 to 20A
- PS(02h): Represents a very light load <5A

PS(03h) is not supported by the processor. The VR may change its configuration to meet the processor's power needs with greater efficiency. For example, it may reduce the number of active phases, transition from Continuous Conduction Mode (CCM) to Discontinuous Conduction Mode (DCM) mode, reduce the switching frequency or pulse skip, or change to asynchronous regulation. For example, typical power states are 00h = run in normal mode; a command of 01h= shed phases mode, and an 02h=pulse skip.

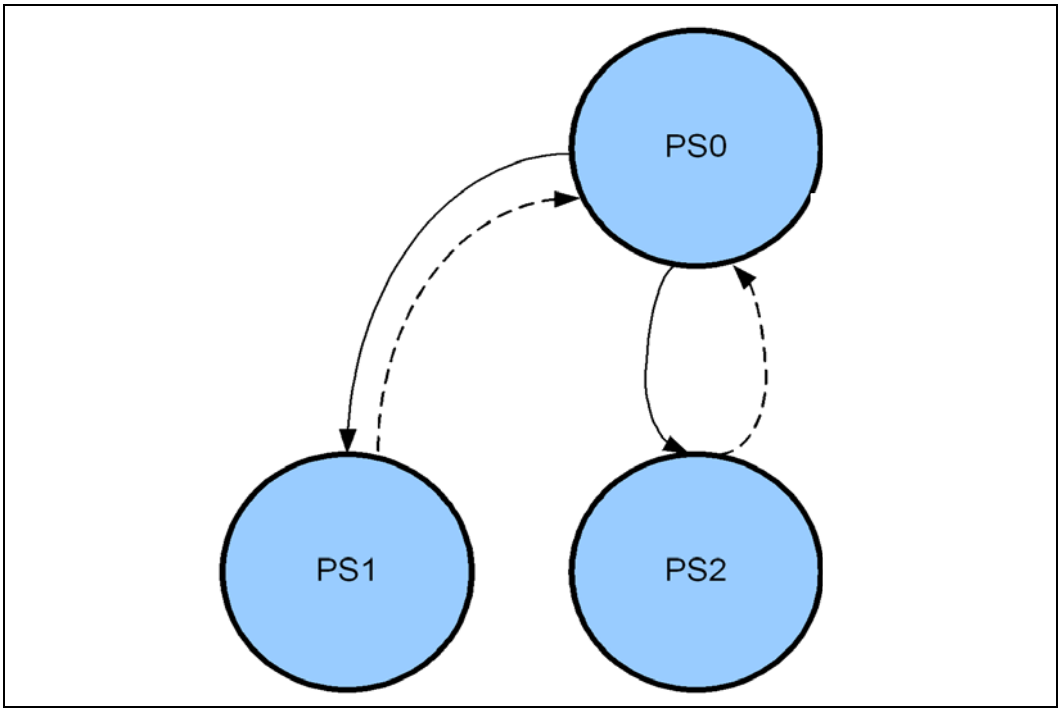
The VR may reduce the number of active phases from PS(00h) to or from PS(01h) or PS(00h) to or from PS(02h) for example. There are multiple VR design schemes that can be used to maintain a greater efficiency in these different power states, please work with your VR controller suppliers for optimizations.

The SetPS command sends a byte that is encoded with the desired power state of the VR.

If a power state is not supported by the controller, the slave should acknowledge with command rejected (11b)

If the VR is in a low power state and receives a SetVID command moving the VID up, then the VR exits the low power state and moves to normal mode (PS0) in order to move the voltage up as fast as possible. The processor must reissue a low power state (PS1 or PS2) command if it is in a low current condition at the new higher voltage. See Figure 4-1 for VR power state transitions.

Figure 4-1. VR Power-State Transitions



4.1.2 SVID Voltage Rail Addressing

The processor addresses nine voltage rail control segments. Table 4-1 shows the address assignment for each rail. The SVID data packet contains a 4-bit addressing code:

Table 4-1. SVID Address Usage

PWM Address (HEX)	Processor Voltage Rail[1, 2, 3]
00	VCCP
01	VCCU
02	VCCD012
03	+1 not used
04	VCCD345
05	+1 not used
06	VCCCLR
07	VCCMLB
08	VCC_CDCORE[4]

Notes:
1. Check with VR vendors to determine the physical address assignment method for their controllers.
2. VR addressing is assigned on a per-voltage-rail basis. Dual VR controllers will have two addresses with the lowest order address, always being the higher phase count.
3. For future platform flexibility, the VR controller should include an address offset, as shown with +1 not used.
4. The VCC_CDCORE VR controller's ALERT# signal must not be connected to the processor. (All other VR controllers' ALERT# signals must be connected to the processor, as is normal.)

Table 4-2. VR12.0/12.5 Reference Code Voltage Identification (VID) Table

Hex	V	Hex	V	Hex	V	Hex	V	Hex	V	Hex	V	Hex	V	Hex	V	Hex	V
VCCP, VCCU, VCCCLR, VCCMLB, VCC_CDCORE (VR12.0 Mode)																	
00	0.000	42	0.575	50	0.645	5E	0.715	6C	0.785	7A	0.855	88	0.925	96	0.995	A4	1.065
		43	0.580	51	0.650	5F	0.720	6D	0.790	7B	0.860	89	0.930	97	1.000	A5	1.070
		44	0.585	52	0.655	60	0.725	6E	0.795	7C	0.865	8A	0.935	98	1.005	A6	1.075
		45	0.590	53	0.660	61	0.730	6F	0.800	7D	0.870	8B	0.940	99	1.010	A7	1.080
		46	0.595	54	0.665	62	0.735	70	0.805	7E	0.875	8C	0.945	9A	1.015	A8	1.085
		47	0.600	55	0.670	63	0.740	71	0.810	7F	0.880	8D	0.950	9B	1.020	A9	1.090
		48	0.605	56	0.675	64	0.745	72	0.815	80	0.885	8E	0.955	9C	1.025	AA	1.095
		49	0.610	57	0.680	65	0.750	73	0.820	81	0.890	8F	0.960	9D	1.030	AB	1.100
		4A	0.615	58	0.685	66	0.755	74	0.825	82	0.895	90	0.965	9E	1.035	AC	1.105
3D	0.550	4B	0.620	59	0.690	67	0.760	75	0.830	83	0.900	91	0.970	9F	1.040	AD	1.110
3E	0.555	4C	0.625	5A	0.695	68	0.765	76	0.835	84	0.905	92	0.975	A0	1.045	AE	1.115
3F	0.560	4D	0.630	5B	0.700	69	0.770	77	0.840	85	0.910	93	0.980	A1	1.050	AF	1.120
40	0.565	4E	0.635	5C	0.705	6A	0.775	78	0.845	86	0.915	94	0.985	A2	1.055	B0	1.125
41	0.570	4F	0.640	5D	0.710	6B	0.780	79	0.850	87	0.920	95	0.990	A3	1.060		
VCCD012 and VCCD345 (VR12.5 Mode)																	
				43	1.160	46	1.190	49	1.220	4C	1.250	4F	1.280				
				44	1.170	47	1.200	4A	1.230	4D	1.260	50	1.290				
				45	1.180	48	1.210	4B	1.240	4E	1.270	51	1.300				

Notes:
1. 00h = Off State
2. VID range beyond those in the table are not used by the processor.

4.2 Power Limit Specifications

The maximum power limits for associated states are listed in Table 4-3.

Table 4-3. Package C-State Power Specifications

C0 (P_{TDP})	C2	C3	C6
215W	95W	43W	31W
245W	95W	43W	31W

Notes:
1. SKUs are subject to change. Contact the local Intel field representative to obtain the latest SKU information.
2. C0 is the performance state of the processor, and includes all P-states, including Intel Turbo Boost Technology.

4.3 Power Supply Specifications

4.3.1 Voltage Specifications

Table 4-4 lists the voltage requirements for the processor's voltage rails at the processor's sense pins (or, if none, at its LGA lands).

Table 4-4. Voltage Pin Level Specification (Sheet 1 of 2)

Symbol	Parameter	Number of Lands	Min.	Typ.	Max.	Unit	Notes[4, 7]
VCCCLR	Processor mesh - VID range	106	0.550	N/A	1.100	V	1, 2, 5, 8, 10
	Processor mesh - operational limits		See Section 4.3.3 and Section 4.3.4				3, 9
VCCP	Processor core - VID range (215W SKU)	303	0.550	N/A	1.125	V	1, 2, 5, 8, 10
	Processor core - VID range (245W SKU)		0.550	N/A	1.150		1, 2, 5, 8, 10
	Processor core - operational limits		See Section 4.3.3 and Section 4.3.4				3, 9
VCC_CDCORE	Fabric core	13	0.810	0.900	1.000	V	1, 2, 3, 5
VCCU	DDR4 digital and processor misc. I/O	14	V_{Typ} - 5%	1.060	V_{Typ} + 5%	V	1, 2, 3, 5
VCCIIO	Processor PCIe digital	7					
VCCDDRIO012 VCCDDRIO345	DDR4 digital	13 17					
VCCMLB0123 VCCMLB4567	MCDRAM digital	24 24	V_{Typ} - 5%	1.000	V_{Typ} + 5%	V	1, 2, 3, 5
VCCMIO0123 VCCMIO4567	MCDRAM on-package I/O	10 10					
VCCMIOQ0123 VCCMIOQ4567	MCDRAM on-package analog	6 6					
VCCOPIO01 VCCOPIO23 VCCOPIO45 VCCOPIO67	MCDRAM to processor on-package I/O	8 8 8 8					
VCCD012 VCCD345	DDR4 analog	90 92	1.150	1.210	1.280	V	2, 5, 6
VCCPIO	Processor PCIe*	13	0.950	1.000	1.050	V	3
VCCP_1P0	Fabric PCIe	6	0.960	1.010	1.050	V	6
VCCE_1P0	Fabric analog I/O	7	0.960	1.000	1.050	V	6
VCCMP0123 VCCMP4567	MCDRAM memory cell	24 24	1.140	1.200	1.260	V	3
VCCMPLL01 VCCMPLL23 VCCMPLL45 VCCMPLL67	MCDRAM PLL	2 2 2 2	1.210	1.250	1.275	V	6
VCCMF	MCDRAM proprietary	8	1.540	1.600	1.680	V	6

Table 4-4. Voltage Pin Level Specification (Sheet 2 of 2)

Symbol	Parameter	Number of Lands	Min.	Typ.	Max.	Unit	Notes[4, 7]
VCCLVR	Processor analog	4	1.650	1.750	1.800	V	6
VCCH_1P8	Fabric digital I/O	2	1.620	1.800	1.980	V	6
VCCMH01 VCCMH23 VCCMH45 VCCMH67	MCDRAM core power	2 2 2 2	2.420	2.562	2.750	V	6
VCCH_2P5	Fabric sideband I/O	2	2.250	2.500	2.750	V	6

Notes:

1. Individual processor VID values may be calibrated during manufacturing such that two devices at the same speed may have different settings.
2. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required.
3. The voltage specification requirements are measured across the remote sense pin pairs when provided. Voltage measurement should be taken with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using a 1.5 pF maximum probe capacitance, and 1 mΩ minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
4. The processor should not be subjected to any static voltage level that exceeds the maximum value associated with any particular current. Failure to adhere to this specification can shorten processor lifetime.
5. This specification represents the voltage reduction or increase due to each VID transition, see Section 4.1.
6. All static voltage specification requirements are measured across sense vias on the platform. Choose vias close to the socket and measure with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using 1.5 pF maximum probe capacitance, and 1 mΩ minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
7. Specified voltage ranges are inclusive of DC + AC + ripple.
8. This row specifies the range of VIDs that the processor can issue to the board voltage regulator.
9. The actual voltage seen at the sense pins is based on its loadline with allowable overshoot, as discussed in Section 4.3.3 and Section 4.3.4.
10. This voltage can change dynamically during runtime when different P-states or package C-states are entered.

4.3.2 Current Specifications

Table 4-5 lists the current required for each of the processor's voltage rails at the processor pins.

Table 4-5. Current Pin Level Specification

Symbol	Power Rail Descriptor	ICC MAX[2]	ICC TDC[1]	Unit
I_{VCCCLR}	Processor Mesh	80.00	65.00	A
I_{VCCIIO}	Processor PCIe* digital	2.9	2.2	A
I_{VCCLVR}	Processor analog	1.81	1.41	A
I_{VCCP}	Processor core (215W SKU)	250.0	198.8	A
I_{VCCP}	Processor core (245W SKU)	250.0	220.0	A
I_{VCCPIO}	Process PCIe	6.9	5.3	A
I_{VCC_CDCORE}	Fabric core	9.9	8.9	A
I_{VCCE_1P0}	Fabric on-package I/O	2.96	2.16	A

Table 4-5. Current Pin Level Specification

Symbol	Power Rail Descriptor	ICC MAX[2]	ICC TDC[1]	Unit
I_{VCCH_1P8}	Fabric I/O	80	60	mA
I_{VCCH_2P5}	Fabric Sideband	15.0	10.0	mA
I_{VCCP_1P0}	Fabric PCIe	4.0	3.4	A
$I_{VCCD012}$ $I_{VCCD345}$	DDR4 analog	2.87	2.53	A
$I_{VCCDDRIO012}$ $I_{VCCDDRIO345}$	DDR4 digital	4.0	3.6	A
I_{VCCU}	Processor DDR4 digital	3.5	2.7	A
I_{VCCMF}	MCDRAM JTAG	59	59	mA
$I_{VCCMH01}$ $I_{VCCMH23}$ $I_{VCCMH45}$ $I_{VCCMH67}$	MCDRAM Vpp Charge Pump (4 on-package MCDRAM)	0.122	0.122	A
$I_{VCCMIO0123}$ $I_{VCCMIO4567}$	MCDRAM on-package I/O (4 on-package MCDRAM)	1.4	1.4	A
$I_{VCCMIOQ0123}$ $I_{VCCMIOQ4567}$	MCDRAM on-package I/O Quiet (4 on-package MCDRAM)	2.2	2.2	A
$I_{VCCMLB0123}$ $I_{VCCMLB4567}$	MCDRAM digital (4 on-package MCDRAM)	14.24	14.24	A
$I_{VCCMP0123}$ $I_{VCCMP4567}$	MCDRAM memory cell (4 on-package MCDRAM)	8.75	8.75	A
$I_{VCCMPLL01}$ $I_{VCCMPLL23}$ $I_{VCCMPLL45}$ $I_{VCCMPLL67}$	MCDRAM memory PLL	0.19	0.19	A
$I_{VCCOPIO01}$ $I_{VCCOPIO23}$ $I_{VCCOPIO45}$ $I_{VCCOPIO67}$	Processor I/O to on-package memory	5.1	3.98	A

Notes:

1. I_{CC_TDC} (Thermal Design Current) is the sustained (DC equivalent) current that the processor is capable of drawing indefinitely and should be used for the voltage regulator thermal assessment. The voltage regulator is responsible for monitoring its temperature and asserting the necessary signal to inform the processor of a thermal excursion.
2. Electrically, the voltage regulators must be designed to supply currents up to I_{CC_MAX} without going into overcurrent protection. For VCCP, I_{CC_MAX} is specified at the relative V_{CC_MAX} point on the load line, and the processor is capable of drawing I_{CC_MAX} for up to 25 ms.
3. 215W SKU/245W SKU, respectively

4.3.3 Static and Transient Loadlines

Table 4-6 and Table 4-7 with Figure 4-2 and Figure 4-3 specify the static and transient behavior for VCCP and VCCCLR, respectively.

Table 4-6. V_{CCP} Static and Transient Tolerance Table

ICC (A)	VCC_MAX (V)	VCC_TYP (V)	VCC_MIN (V)	Notes
0.0	VID + 0.015	VID + 0.000	VID - 0.015	1-5
13.2	VID + 0.004	VID - 0.011	VID - 0.026	1-5
26.3	VID - 0.006	VID - 0.021	VID - 0.036	1-5
39.5	VID - 0.017	VID - 0.032	VID - 0.047	1-5
52.6	VID - 0.027	VID - 0.042	VID - 0.057	1-5
65.8	VID - 0.038	VID - 0.053	VID - 0.068	1-5
78.9	VID - 0.048	VID - 0.063	VID - 0.078	1-5
92.1	VID - 0.059	VID - 0.074	VID - 0.089	1-5
105.3	VID - 0.069	VID - 0.084	VID - 0.099	1-5
118.4	VID - 0.080	VID - 0.095	VID - 0.110	1-5
131.6	VID - 0.090	VID - 0.105	VID - 0.120	1-5
144.7	VID - 0.101	VID - 0.116	VID - 0.131	1-5
157.9	VID - 0.111	VID - 0.126	VID - 0.141	1-5
171.1	VID - 0.122	VID - 0.137	VID - 0.152	1-5
184.2	VID - 0.132	VID - 0.147	VID - 0.162	1-5
197.4	VID - 0.143	VID - 0.158	VID - 0.173	1-5
210.5	VID - 0.153	VID - 0.168	VID - 0.183	1-5
223.7	VID - 0.164	VID - 0.179	VID - 0.194	1-5
236.8	VID - 0.174	VID - 0.189	VID - 0.204	1-5
250.0	VID - 0.185	VID - 0.200	VID - 0.215	1-5

Notes:
1. The loadline specification includes both static and transient limits.
2. This table is intended to aid in reading discrete points on graph in Figure 4-2.
3. The loadlines specify voltage limits at the die measured at the VCCP_SENSE and VSS_VCCP_SENSE lands.
4. The Vcc_min and Vcc_max loadlines represent static and transient limits. See Section 4.3.4 for Vcc overshoot specifications.
5. The adaptive loadline positioning slope is 0.8 mΩ, and the tolerance (TOB) is ±15 mV.

Figure 4-2. V_{CCP} Static and Transient Tolerance Loadlines

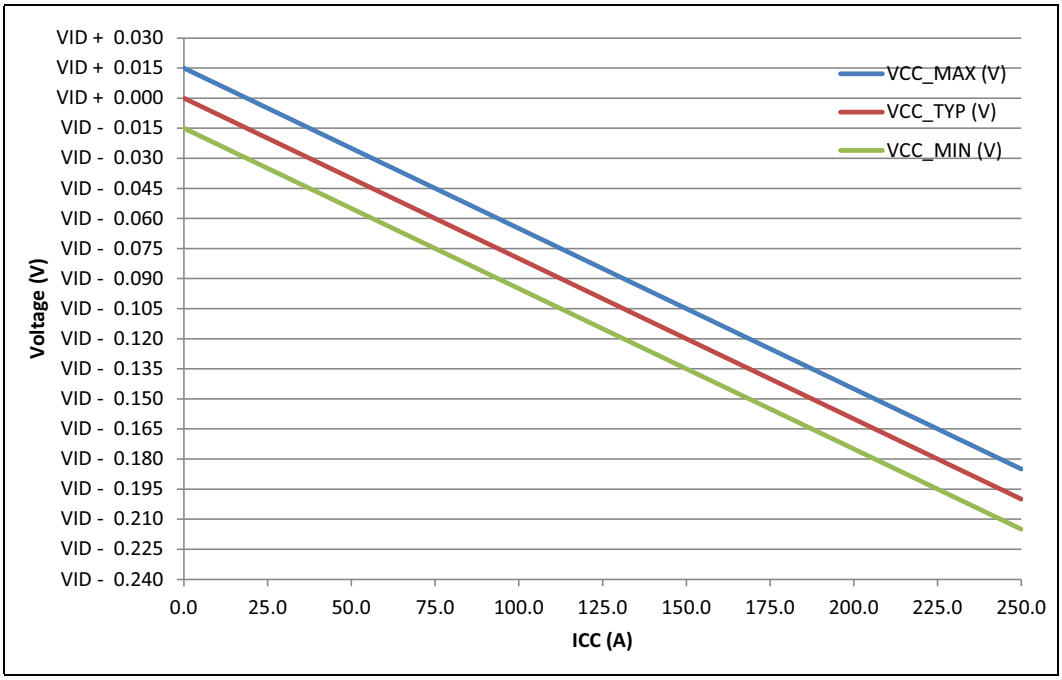


Table 4-7. V_{CCCLR} Static and Transient Tolerance Table (Sheet 1 of 2)

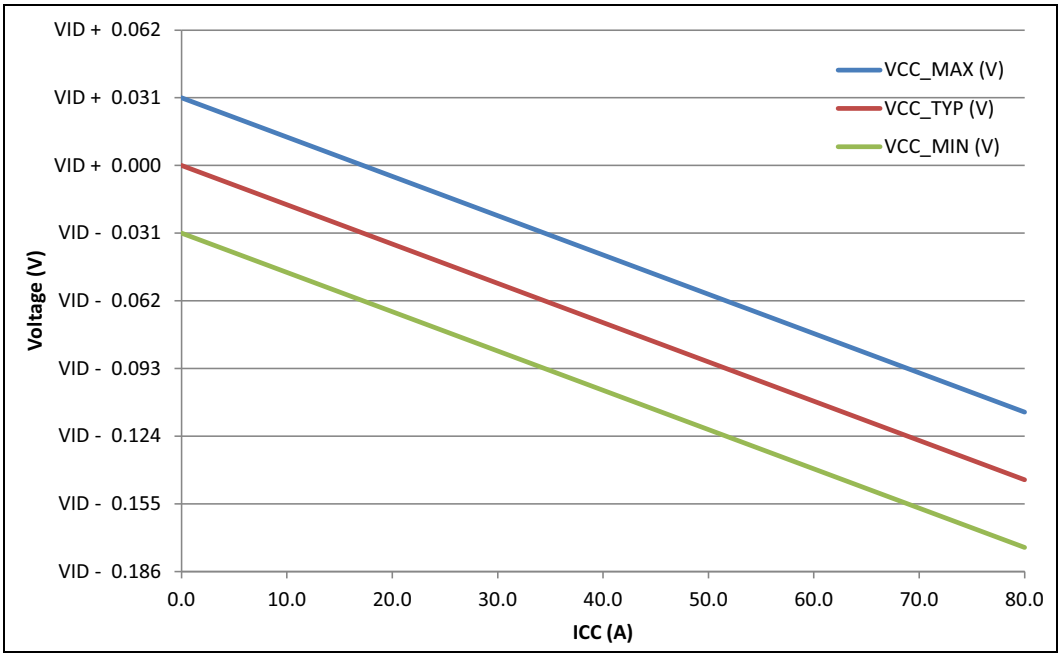
ICC (A)	VCC_MAX (V)	VCC_TYP (V)	VCC_MIN (V)	Notes
0.0	VID + 0.031	VID + 0.000	VID - 0.031	1-5
4.2	VID + 0.023	VID - 0.008	VID - 0.039	1-5
8.4	VID + 0.016	VID - 0.015	VID - 0.046	1-5
12.6	VID + 0.008	VID - 0.023	VID - 0.054	1-5
16.8	VID + 0.001	VID - 0.030	VID - 0.061	1-5
21.1	VID - 0.007	VID - 0.038	VID - 0.069	1-5
25.3	VID - 0.014	VID - 0.045	VID - 0.076	1-5
29.5	VID - 0.022	VID - 0.053	VID - 0.084	1-5
33.7	VID - 0.030	VID - 0.061	VID - 0.092	1-5
37.9	VID - 0.037	VID - 0.068	VID - 0.099	1-5
42.1	VID - 0.045	VID - 0.076	VID - 0.107	1-5
46.3	VID - 0.052	VID - 0.083	VID - 0.114	1-5
50.5	VID - 0.060	VID - 0.091	VID - 0.122	1-5
54.7	VID - 0.068	VID - 0.099	VID - 0.130	1-5
58.9	VID - 0.075	VID - 0.106	VID - 0.137	1-5
63.2	VID - 0.083	VID - 0.114	VID - 0.145	1-5
67.4	VID - 0.090	VID - 0.121	VID - 0.152	1-5
71.6	VID - 0.098	VID - 0.129	VID - 0.160	1-5
75.8	VID - 0.105	VID - 0.136	VID - 0.167	1-5

Table 4-7. V_{CCCLR} Static and Transient Tolerance Table (Sheet 2 of 2)

ICC (A)	VCC_MAX (V)	VCC_TYP (V)	VCC_MIN (V)	Notes
80.0	VID - 0.113	VID - 0.144	VID - 0.175	1-5

Notes:
1. The loadline specification includes both static and transient limits.
2. This table is intended to aid in reading discrete points on graph in Figure 4-3.
3. The loadlines specify voltage limits at the die measured at the VCCCLR_SENSE and VSS_VCCCLR_SENSE lands.
4. The Vcc_min and Vcc_max loadlines represent static and transient limits. see Section 4.3.4 for Vcc overshoot specifications.
5. The adaptive loadline positioning slope is 1.8 mΩ, and the tolerance (TOB) is ±31 mV.

Figure 4-3. V_{CCCLR} Static and Transient Tolerance Loadlines



4.3.4 VCC Overshoot Specifications

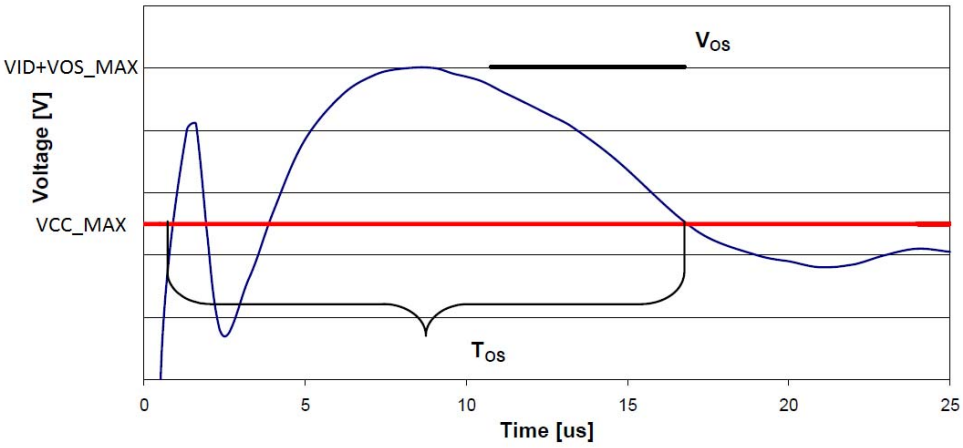
For both the VCCP and VCCCLR voltage rails, the processor can tolerate short transient overshoot events where VCC exceeds VCC_MAX (the maximum voltage at any place along the loadline) when transitioning from a high- to low-current load. This overshoot cannot exceed the absolute value VID + VOS_MAX (VOS_MAX is the maximum allowable overshoot above VID), and it must be less than TOS_MAX in duration (inclusive of all excursions due to ringing). These specifications apply to the processor die voltage as measured across the VCC_SENSE and VSS_VCC_SENSE lands. The processor can tolerate overshoot to phase added bumps as well. See Table 4-8.

Table 4-8. VCC Overshoot Specifications

Symbol	Definition	Min.	Max.	Unit	Figure	Notes
VOS_MAX	Maximum allowable VCC overshoot above VID		65	mV	Figure 4-4	1
TOS_MAX	Maximum allowable time duration of VCC overshoot above VCC_MAX at the new lighter load		25	µs	Figure 4-4	1, 2

Notes:
1. These specifications apply to the processor die voltage as measured across the remote sense points and should be taken with the oscilloscope bandwidth limit setting of DC to 20 MHz (or DC to 100 MHz), depending on your particular scope's bandwidth setting capability (with DC to 20 MHz preference).
2. VCC_MAX = VID - $R_{loadline}$ * ICC + TOB

Figure 4-4. VCC Overshoot Example Waveform



T_{OS}: Overshoot time above VCC_MAX
V_{OS}: Overshoot voltage above VCC_MAX

4.4 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Large electrolytic bulk capacitors (C_{BULK}), help maintain the output voltage during current transients, for example coming out of an idle condition. Care must be taken in the baseboard design to ensure that the voltages provided to the processor remain within the specifications listed in Table 4-4. Failure to do so can result in timing violations or reduced lifetime of the processor.

4.5 Processor Power Sequencing

Figure 4-5 and Figure 4-6 show the processor's power sequencing requirements for power-up and power-down respectively.

Figure 4-5. Processor Voltage Sequence Timing Requirements - Power Up

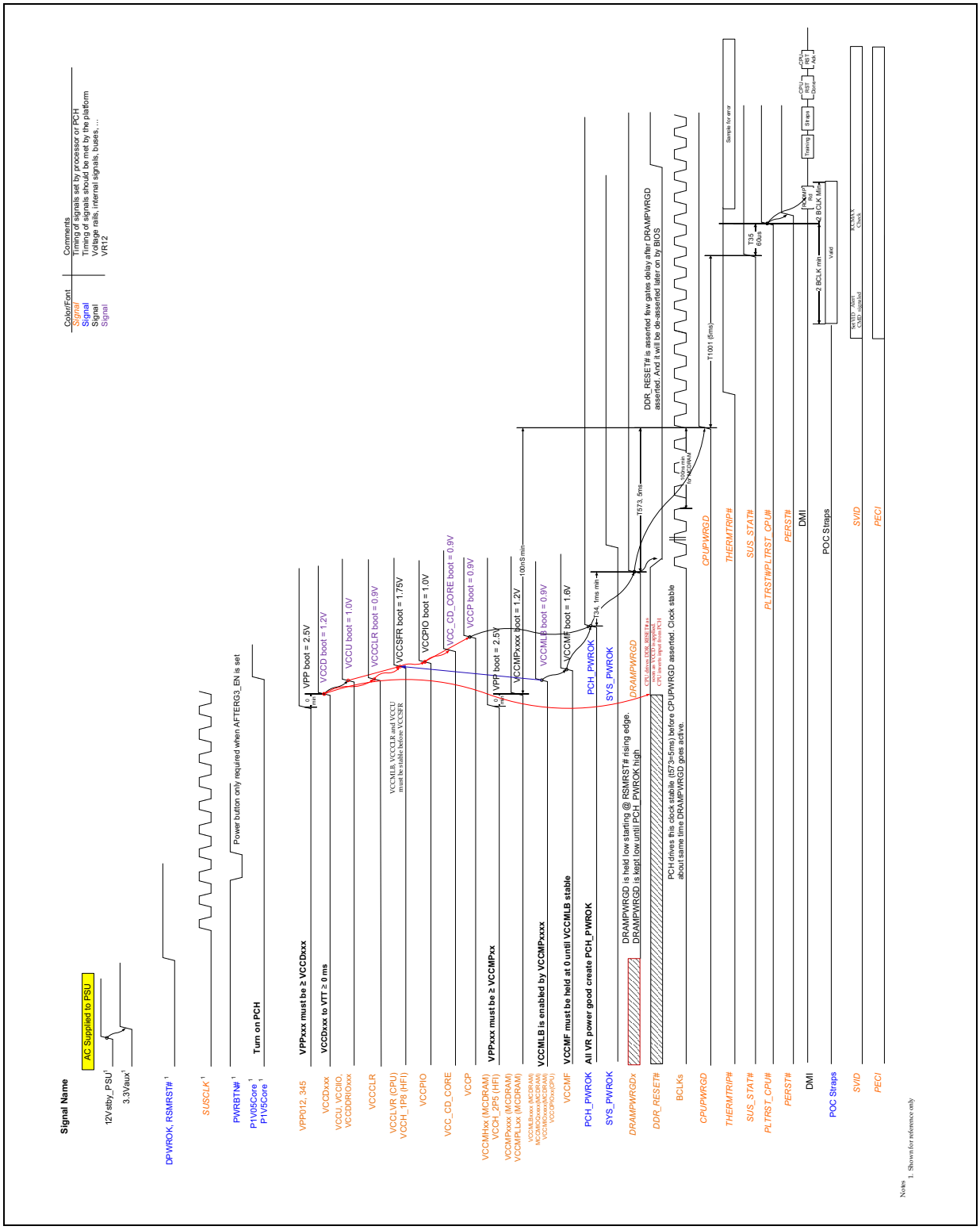
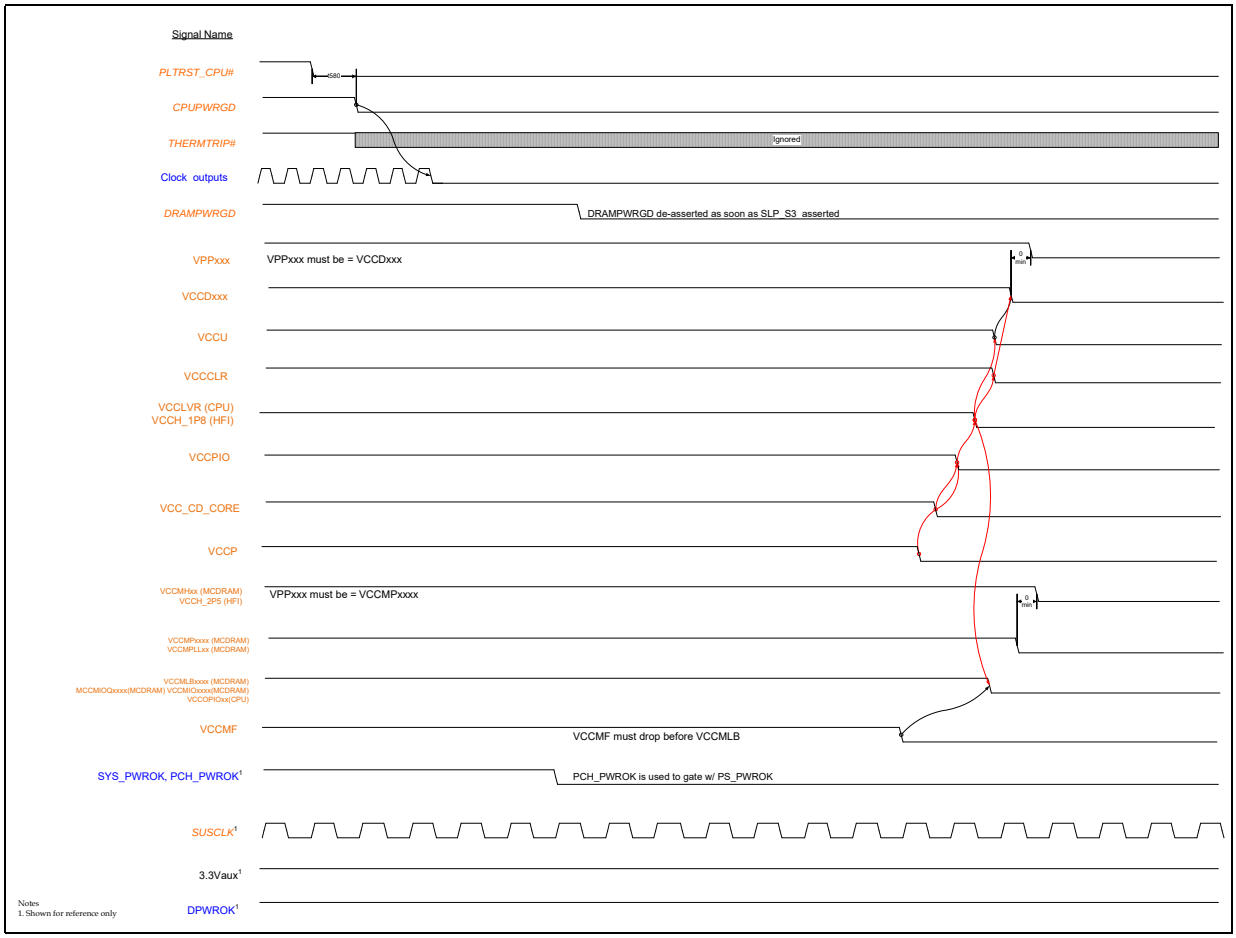


Figure 4-6. Processor Voltage Sequence Timing Requirements - Power Down



4.6 Absolute Maximum and Minimum Ratings

Table 4-9 specifies the absolute maximum and minimum ratings for the processor power pins. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding the absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time, it will either not function or its reliability will be severely degraded when returned to conditions within the functional operating condition limits.

Although the processor contains protective circuitry to resist damage from Electro-Static Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

Table 4-9. Processor Absolute Minimum and Maximum Ratings: Power Lands

Symbol	Parameter	Absolute Min.	Absolute Max.	Unit
VCC_CDCORE	Power supply voltage with respect to V_{SS}	-0.3	1.25	V
VCCCLR	Power supply voltage with respect to V_{SS}	-0.3	1.3	V
VCCD012 VCCD345	Power supply voltage with respect to V_{SS}	-0.3	1.8	V
VCCDDRIO012 VCCDDRIO345	Power supply voltage with respect to V_{SS}	-0.3	1.3	V
VCCE_1P0	Power supply voltage with respect to V_{SS}	-0.3	1.3	V
VCCH_1P8	Power supply voltage with respect to V_{SS}	-0.3	1.85	V
VCCH_2P5	Power supply voltage with respect to V_{SS}	-0.3	2.8	V
VCCIIO	Power supply voltage with respect to V_{SS}	-0.3	1.3	V
VCCLVR	Power supply voltage with respect to V_{SS}	-0.3	1.8	V
VCCMF	Power supply voltage with respect to V_{SS}	-0.3	1.8	V
VCCMH01, VCCMH23, VCCMH45, VCCMH67	Power supply voltage with respect to V_{SS}	-0.3	2.8	V
VCCMIO0123 VCCMIO4567	Power supply voltage with respect to V_{SS}	-0.3	1.1	V
VCCMIOQ0123 VCCMIOQ4567	Power supply voltage with respect to V_{SS}	-0.3	1.1	V
VCCMLB0123 VCCMLB4567	Power supply voltage with respect to V_{SS}	-0.3	1.1	V
VCCMP0123 VCCMP4567	Power supply voltage with respect to V_{SS}	-0.3	1.4	V
VCCMPLL01, VCCMPLL23, VCCMPLL45, VCCMPLL67	Power supply voltage with respect to V_{SS}	-0.3	1.4	V
VCCOPIO01, VCCOPIO23, VCCOPIO45, VCCOPIO67	Power supply voltage with respect to V_{SS}	-0.3	1.3	V
VCCP	Power supply voltage with respect to V_{SS}	-0.3	1.3	V
VCCP_1P0	Power supply voltage with respect to V_{SS}	-0.3	1.3	V
VCCPIO	Power supply voltage with respect to V_{SS}	-0.3	1.3	V
VCCU	Power supply voltage with respect to V_{SS}	-0.3	1.3	V

Notes:
1. For functional operation, all processor electrical, signal quality, mechanical, and thermal specifications must be satisfied.
2. Overshoot and undershoot voltage guidelines for I/O signals are outlined in Section 5.2.2. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.

§

5.0 Processor Signal Specifications

5.1 DC Specifications

DC specifications are defined at the processor pins, unless otherwise noted. DC specifications are only valid while meeting specifications for case temperature (T_{CASE} specified in *Intel® Xeon Phi™ Processor x200 Product Family Thermal/Mechanical Specification and Design Guide*), clock frequency, and input voltages. Care should be taken to read all notes associated with each specification.

5.1.1 DDR4 Signal DC Specifications

The DC specifications for the processor's DDR4 interface are given in Table 5-1.

Table 5-1. DDR4 Signal DC Specifications (Sheet 1 of 2)

Symbol	Definition	Min.	Typ.	Max.	Unit	Notes[1]
I_{IL}	Input Leakage Current	-1.4		+1.4	mA	9
Data Signals						
R_{ON}	DDR4 Data Buffer "On" Resistance	27		33	Ω	6
Data ODT	On-Die Termination for Data Signals	45		55	Ω	8
Reference Clock and Command Signals						
V_{OL}	Output Low Voltage		$(V_{CCD} / 2) * (R_{ON} / (R_{ON} + R_{VTT\_TERM}))$		V	2, 7
V_{OH}	Output High Voltage		$V_{CCD} - [(V_{CCD} / 2) * (R_{ON} / (R_{ON} + R_{VTT\_TERM}))]$		V	2, 5, 7
Data Signals						
V_{OL}	Output Low Voltage		Varies		V	10
V_{OH}	Output High Voltage		V_{CCD}		V	
Reference Clock Signal						
R_{ON}	DDR4 CLK Buffer "On" Resistance	27		33	Ω	6
Command Signals						
R_{ON}	DDR4 CMD Buffer "On" Resistance	16		20	Ω	6
R_{ON}	DDR4 RST Buffer "On" Resistance		78		Ω	6
V_{OL}	Output Low Voltage: DDR{012/345}_RESET_N			$0.2 * V_{CCD}$	V	2
V_{OH}	Output High Voltage: DDR{012/345}_RESET_N	$0.9 * V_{CCD}$			V	2
Control Signals						
R_{ON}	DDR4 CTRL Buffer "On" Resistance	27		33	Ω	6

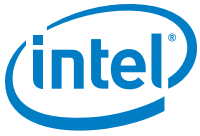


Table 5-1. DDR4 Signal DC Specifications (Sheet 2 of 2)

Symbol	Definition	Min.	Typ.	Max.	Unit	Notes[1]
DDR4 Miscellaneous Signals						
ALERT_N	On-Die Termination for Parity Error Signals	81	90	99	Ω	
V_{IL}	Input Low Voltage: DDR{012/345}_DRAM_PWR_OK			304	mV	2, 3
V_{IH}	Input High Voltage: DDR{012/345}_DRAM_PWR_OK	800			mV	2, 4, 5
V_{IL}	Input Low Voltage: DDR{012/345}_MEMHOT_N			0.3 * VCCU	V	
V_{IH}	Input High Voltage: DDR{012/345}_MEMHOT_N	0.7 * VCCU			V	
$V_{Hysteresis}$	Hysteresis	0.1 * VCCU			V	
I_{IL}	Input Leakage Current	50		200	µA	
V_{OL}	Output Low Voltage: DDR{012/345}_MEMHOT_N			0.2 * VCCU	V	
$R_{ON\_Pulldown}$	Buffer On Resistance: DDR{012/345}_MEMHOT_N	4		14	Ω	
ER_O	Output Edge Rate: DDR{012/345}_MEMHOT_N	0.05		0.6	V/ns	11

Notes:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The voltage rail V_{CCD} is set to 1.210V nominal per JEDEC specification.
3. V_{IL} is the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
4. V_{IH} is the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
5. V_{IH} and V_{OH} may experience excursions above V_{CCD}. However, input signal drivers must comply with the signal quality specifications. Refer to Section 5.2.
6. This is the pull down driver resistance. Refer to processor signal integrity models for I/V characteristics. Reset drive does not have a termination.
7. RVTT_TERM is the termination on the DIMM and not controlled by the processor. Refer to the applicable DIMM datasheet.
8. The minimum and maximum values for these signals are programmable by BIOS to one of the pairs.
9. Input leakage current is specified for all DDR4 signals.
10. $V_{OL} = R_{ON} * [V_{CCD} / (R_{ON} + R_{TT}\_Eff)]$, where R_{TT}_Eff is the effective pull-up resistance of all DIMMs in the system, including ODTs and series resistors on the DIMMs.
11. Value is given for a 50Ω pull up to VCCU, measuring between 0.2 * VCCU and 0.8 * VCCU.

5.1.2 SMBus DC Specifications

The DC specifications for the processor's SMBus interface to the DDR4 DIMMs are given in Table 5-2.

Table 5-2. SMBus DC Specifications

Symbol	Definition	Min.	Max.	Unit	Notes
V_{IL}	Input Low Voltage		0.3 * VCCU	V	
V_{IH}	Input High Voltage	0.7 * VCCU		V	
$V_{Hysteresis}$	Hysteresis	0.1 * VCCU		V	
I_{IL}	Input Leakage Current	50	200	µA	
V_{OL}	Output Low Voltage		0.2 * VCCU	V	
R_{ON}	Buffer On Resistance	4	14	Ω	
ER_O	Output Edge Rate	0.05	0.6	V/ns	1

Note:
1. Value is given for a 50 Ω pull up to VCCU, measuring between 0.2 * VCCU and 0.8 * VCCU.

5.1.3 PCI Express DC Specifications

The processor DC specifications for the PCI Express interface are available in the *PCI Express Base Specification Revision 3.0*.

5.1.4 DMI2 DC Specifications

The processor DC specifications for the DMI2 are available in the *PCI Express Base Specification 2.0 and 1.0*.

5.1.5 Fabric Component Signals DC Specifications

The DC specifications for the processor with fabric's fabric sideband signals are given in Table 5-3.

Table 5-3. Fabric Component Signals DC Specifications (Sheet 1 of 2)

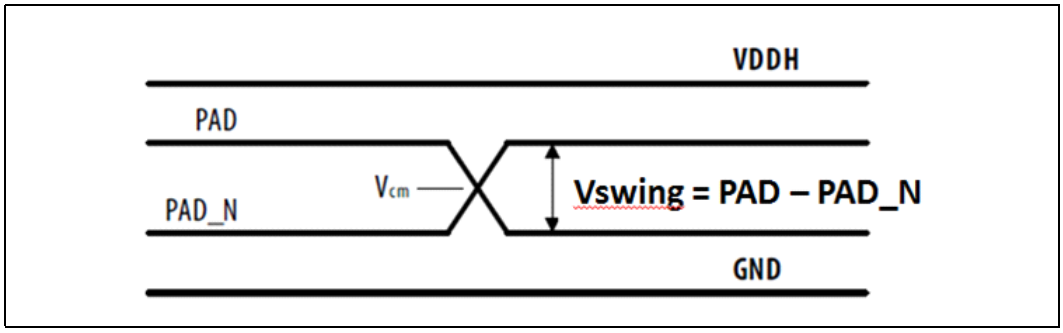
Symbol	Definition	Min.	Typ.	Max.	Unit	Notes
HCSL Signals: CD_HFI_REFCLK_D{N/P}[1]						
V_{Swing}	Single-ended voltage swing from CD_HFI_REFCLK_DP to CD_HFI_REFCLK_DN	0.3	0.7	1.2	V	2
V_{CM}	Median crosspoint voltage	0.15	0.35	0.6	V	2
$V_{Hysteresis}$	Pad Hysteresis	0.02	0.025	0.04	V	
R_{Term}	Termination resistance		50		Ω	
ER_I	Input rising/falling edge rate	0.6		4.0	V/ns	3
PCIE3CLK Signals: CD_PE_REFCLK_D{N/P}						
The DC specifications for this clock are available in the *PCI Express Base Specification Revision 3.0*.						

Table 5-3. Fabric Component Signals DC Specifications (Sheet 2 of 2)

Symbol	Definition	Min.	Typ.	Max.	Unit	Notes
CMOS / Open Drain 2.5V Signals: Sideband						
V_{IL}	Input Low Voltage	-0.3		0.7	V	
V_{IH}	Input High Voltage	1.7		VCCH_2P5 + 1.2	V	
$V_{Hysteresis}$	Hysteresis	0.14		0.30	V	
V_{OL}	Output Low Voltage			0.4	V	
PU	External Pullup to VCCH_2P5	1k		10k	Ω	
CMOS 1.8V Signals: JTAG						
V_{IL}	Input Low Voltage	-0.3		0.35 * VCCH_1P8	V	
V_{IH}	Input High Voltage	0.65 * VCCH_1P8		VCCH_1P8 + 1.2	V	
$V_{Hysteresis}$	Hysteresis	0.192		0.477	V	
V_{OL}	Output Low Voltage			0.25 * VCCH_1P8	V	
V_{OH}	Output High Voltage	0.75 * VCCH_1P8			V	

Notes:
1. Contact Intel for a list of approved crystal vendors for this reference clock. The vendor parts have been carefully evaluated by Intel to ensure they meet the Fabric requirements. It is important that the customer use one of the parts on this list and follow all design guidelines.
2. See Figure 5-1.
3. Measurement taken from differential waveform; measured from -150 mV to +150 mV on the differential waveform.

Figure 5-1. CD_HFI_REFCLK Single-Ended Measurement Points for Median Crosspoint and Swing



5.1.6 PECI DC Specifications

The PECI interface operates in the VCCU voltage domain (i.e., V_{TT} = VCCU), with the set of DC electrical specifications shown in Table 5-4.

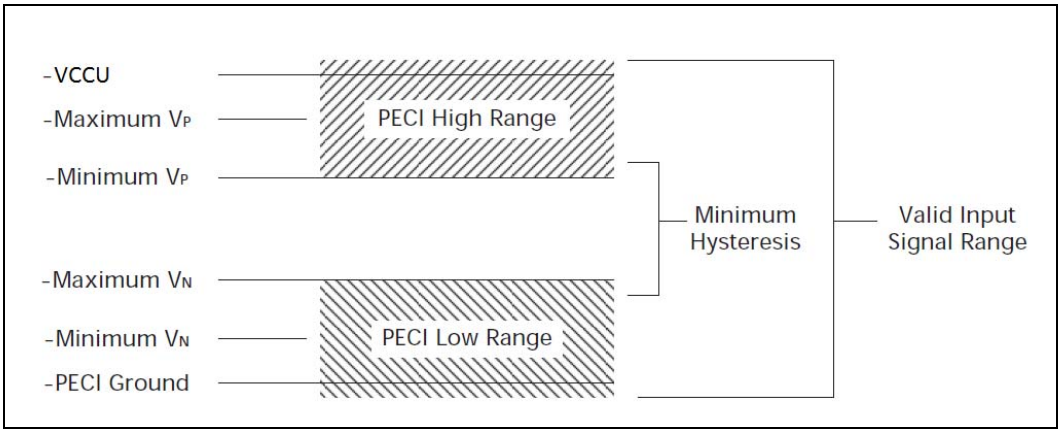
The PECI client and host input buffers must use a Schmitt-triggered input design for improved noise immunity.

Table 5-4. PECI DC Specifications

Symbol	Definition	Min.	Max.	Unit	Figure	Notes
V_{In}	Input Voltage Range	-0.15	VCCU + 0.15	V		
V_N	Negative-edge threshold voltage	0.275 * VCCU	0.500 * VCCU	V	Figure 5-2	1
V_P	Positive-edge threshold voltage	0.550 * VCCU	0.725 * VCCU	V	Figure 5-2	1
$V_{Hysteresis}$	Hysteresis	0.1 * VCCU		V		
R_{ON_Pullup}	Buffer On Resistance (V_{OH} = 0.75 * VCCU)	20	36	Ω		
I_{Leak+}	High impedance state leakage to VCCU (V_{leak} = V_{OL})		50	µA		2
I_{Leak-}	High impedance leakage to GND (V_{leak} = V_{OH})		10	µA		2
C_{Bus}	Bus capacitance per node		10	pF		3, 4
V_{Noise}	Signal noise immunity above 300 MHz	0.1 * VCCU		V_{p-p}		
I_{Source}	High level output source (V_{OH} = 0.75 * VCCU)	-6.0		mA		
I_{Sink}	Low level output sink (V_{OL} = 0.25 * VCCU)	0.5	1.0	mA		
ER_O	Output Edge Rate	1.5	4.0	V/ns		5

Notes:
1. It is expected that the PECI driver will take into account the variance in the receiver input thresholds and consequently, be able to drive its output within safe limits.
2. The leakage specification applies to powered devices on the PECI bus.
3. One node is counted for each client and one node for the system host. Extended trace lengths might appear as additional nodes.
4. Excessive capacitive loading on the PECI line may slow down the signal rise/fall times and consequently limit the maximum bit rate at which the interface can operate.
5. Value is given for a 50 Ω pull down to GND, measuring between 0.2 * VCCU and 0.8 * VCCU.

Figure 5-2. PECI Input Device Hysteresis



5.1.7 System Reference Clock (BCLK) DC Specifications

The DC specifications for the system reference clock (BCLK) required by the processor are given in Table 5-5.

Table 5-5. System Reference Clock (BCLK) DC Specifications

Symbol	Definition	Signal	Min.	Max.	Unit	Figure	Notes[1]
$V_{BCLK\_diff\_ih}$	Differential Input High Voltage	Differential	0.150		V	Figure 5-3	2
$V_{BCLK\_diff\_il}$	Differential Input Low Voltage	Differential		-0.150	V	Figure 5-3	2
V_{cross} (abs)	Absolute Crossing Point	Single-ended	0.250	0.550	V	Figure 5-4, Figure 5-5	3, 5, 7
V_{cross} (rel)	Relative Crossing Point	Single-ended	0.250 + 0.5 * (VH_{avg} - 0.700)	0.550 + 0.5 * (VH_{avg} - 0.700)	V	Figure 5-4	3, 4, 5
ΔV_{cross}	Range of Crossing Points	Single-ended		0.140	V	Figure 5-6	6
V_{TH}	Threshold Voltage	Single-ended	Vcross - 0.1	Vcross + 0.1	V		
I_{IL}	Input Leakage Current	N/A		1.5	µA		8
C_{pad}	Pad Capacitance	N/A	0.9	1.1	pF		

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The differential waveform is derived from BCLK_DP minus BCLK_DN.
3. Crossing voltage is defined as the instantaneous voltage value when the rising edge of BCLK_DP is equal to the falling edge of BCLK_DN.
4. V_{Havg} is the statistical average of the V_H measured by the oscilloscope.
5. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
6. ΔV_{CROSS} is defined as the total variation of all crossing voltages as defined in Note 3.
7. The rising edge of BCLK_DP is equal to the falling edge of BCLK_DN.
8. For Vin between 0 and Vih

Figure 5-3. BCLK Differential Measurement Point for Ringback

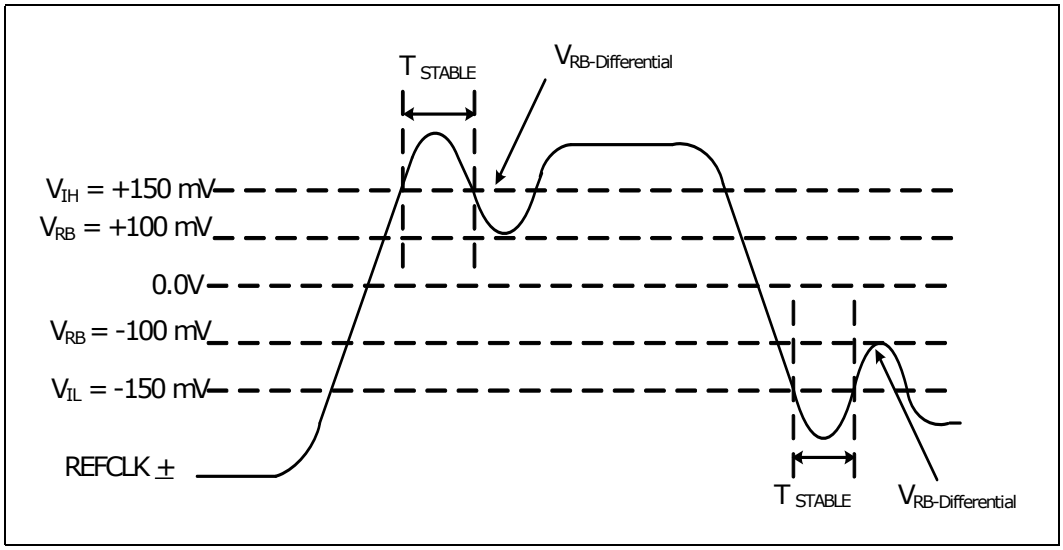


Figure 5-4. BCLK Single-Ended Crosspoint Specification

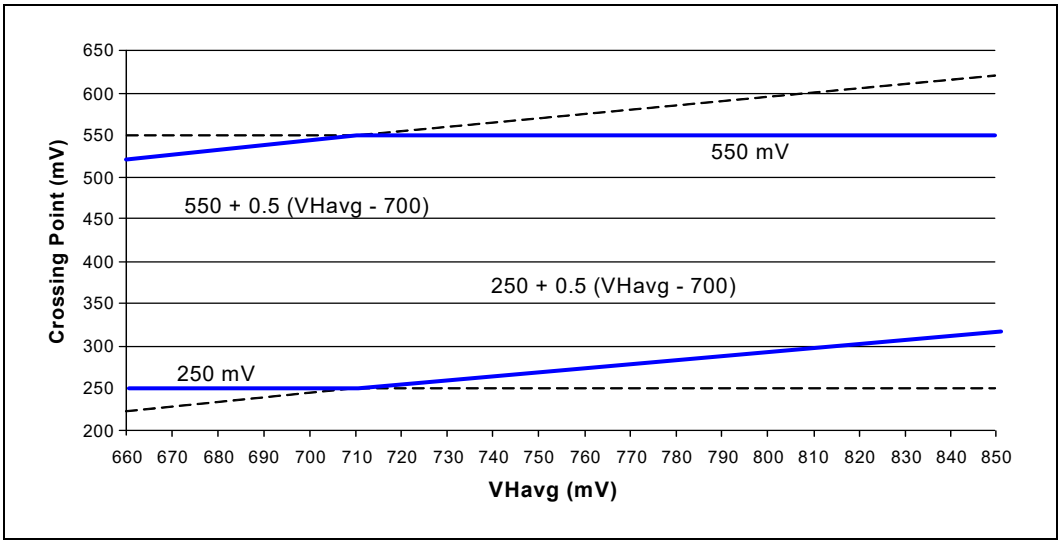


Figure 5-5. BCLK Single-Ended Measurement Points for Absolute Crosspoint and Swing

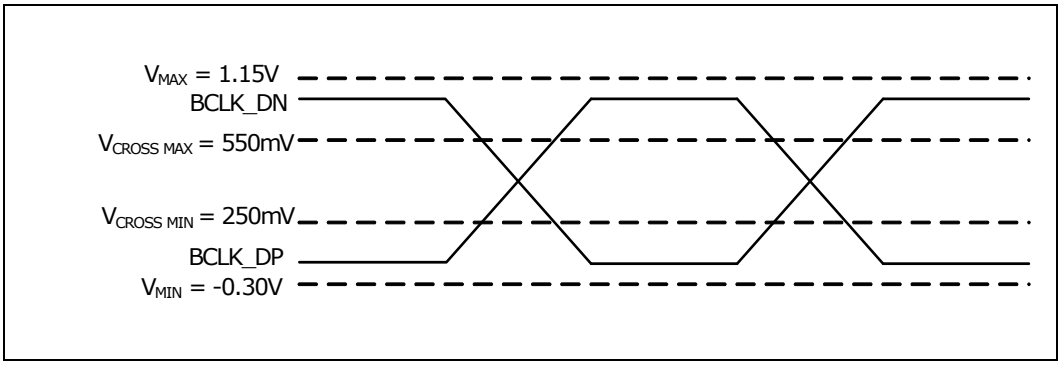
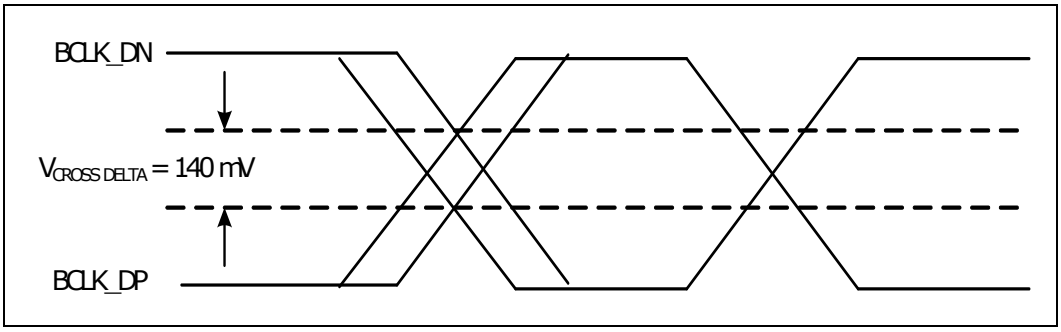


Figure 5-6. BCLK Single-Ended Measurement Points for Delta Crosspoint



5.1.8 JTAG and TAP Signals DC Specifications

The DC specifications for the processor's JTAG and TAP signals are given in Table 5-6.

Table 5-6. JTAG and TAP Signals DC Specifications

Symbol	Definition	Min.	Typ.	Max.	Unit	Notes
V_{IL}	Input Low Voltage: BPM_N[7:0], PREQ_N, TMS, TDI			0.5 * VCCU	V	
V_{IH}	Input High Voltage: BPM_N[7:0], PREQ_N, TMS, TDI	0.8 * VCCU			V	
V_{IL}	Input Low Voltage: OBS[15:0], DEBUG_EN_N, EAR_N			0.4 * VCCU	V	
V_{IH}	Input High Voltage: OBS[15:0], DEBUG_EN_N, EAR_N	0.6 * VCCU			V	
V_{IL}	Input Low Voltage: TCK, TRST_N			0.3 * VCCU	V	
V_{IH}	Input High Voltage: TCK, TRST_N	0.7 * VCCU			V	
$V_{Hysteresis}$	Hysteresis	0.1 * VCCU			V	
I_{IL}	Input Leakage Current	50		200	µA	
V_{OL}	Output Low Voltage			0.2 * VCCU	V	
$R_{ON\_Pulldown}$	Buffer On Resistance: BPM_N[7:0], PRDY_N, TDO	4		14	Ω	
$R_{ON\_Pulldown}$	Buffer On Resistance: OBS[15:0], OBSSTB_{N/P}[1:0]		30		Ω	
R_{ON_Pullup}	Buffer On Resistance: OBS[15:0], OBSSTB_{N/P}[1:0]		50		Ω	
ER_O	Output Edge Rate: BPM_N[7:0], PRDY_N, TDO	0.2		1.5	V/ns	1
ER_O	Output Edge Rate: OBS[15:0], OBSSTB_{N/P}[1:0]	1		3.5	V/ns	1

Note:
1. Value is given for a 50Ω pull up to VCCU, measuring between 0.2 * VCCU and 0.8 * VCCU.

5.1.9 Serial VID Interface (SVID) DC Specifications

The DC specifications for the processor's SVID interface to the VRs are given in Table 5-7.

Table 5-7. Serial VID Interface (SVID) DC Specifications

Symbol	Definition	Min.	Typ.	Max.	Unit	Notes
V_{IL}	Input Low Voltage: SVIDDATA, SVIDALERT_N			0.4 * VCCU	V	
V_{IH}	Input High Voltage: SVIDDATA, SVIDALERT_N	0.6 * VCCU			V	
$V_{Hysteresis}$	Hysteresis	0.1 * VCCU			V	
I_{IL}	Input Leakage Current	50		200	µA	
V_{OL}	Output Low Voltage			0.2 * VCCU	V	
$R_{ON\_Pulldown}$	Buffer On Resistance: SVIDCLK, SVIDDATA	4		14	Ω	
ER_O	Output Edge Rate: SVIDCLK, SVIDDATA	1		3.5	V/ns	1

Note:
1. Value is given for a 50Ω pull up to VCCU, measuring between 0.2 * VCCU and 0.8 * VCCU.

5.1.10 Processor Asynchronous Sideband DC Specifications

The DC specifications for the processor's asynchronous sideband signals are given in Table 5-8 and Table 5-9.

Table 5-8. Processor Asynchronous Sideband DC Specifications

Symbol	Definition	Min.	Max.	Unit	Notes[1, 2]
V_{IL}	Input Low Voltage: RESET_N, CPUPWRGD, PMSYNC		0.3 * VCCU	V	
V_{IH}	Input High Voltage: RESET_N, CPUPWRGD, PMSYNC	0.7 * VCCU		V	
V_{IL}	Input Low Voltage: PROCHOT_N, BIST_ENABLE		0.4 * VCCU	V	
V_{IH}	Input High Voltage: PROCHOT_N, BIST_ENABLE	0.6 * VCCU		V	
$V_{Hysteresis}$	Hysteresis	0.1 * VCCU		V	
I_{IL}	Input Leakage Current	50	200	µA	
V_{OL}	Output Low Voltage		0.2 * VCCU	V	
$R_{ON\_Pulldown}$	Buffer On Resistance	4	14	Ω	
ER_O	Output Edge Rate	1	3.5	V/ns	3

Notes:
1. This table applies to the processor sideband and miscellaneous signals specified in Section 3.11.
2. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
3. Value is given for a 50 Ω pull up to VCCU, measuring between 0.2 * VCCU and 0.8 * VCCU.

Table 5-9. Miscellaneous Signals DC Specifications

Symbol	Definition	Min.	Typ.	Max.	Unit
SKTOCC_N, CD_PRESENT_N					
$V_{O\_ABS\_MAX}$	Output Absolute Max. Voltage		3.30	3.50	V
I_{OMAX}	Output Max Current			1	mA

5.2 Signal Quality

Data transfer requires the clean reception of data signals and clock signals. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swings will adversely affect system timings. Ringback and signal non-monotonicity cannot be tolerated since these phenomena may inadvertently advance receiver state machines. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity and can cause device failure if absolute voltage limits are exceeded. Overshoot and undershoot can also cause timing degradation due to the build up of Intersymbol Interference (ISI) effects.

For these reasons, it is crucial that the designer work towards a solution that provides acceptable signal quality across all systematic variations encountered in volume manufacturing.

This section documents signal quality metrics used to derive topology and routing guidelines through simulation. All specifications are specified at the processor die (pad measurements).

Specifications for signal quality are for measurements at the processor core only and are only observable through simulation. Therefore, proper simulation is the only way to verify proper timing and signal quality.

5.2.1 PCIe and DMI Signal Quality Specifications

Signal quality specifications for PCIe and DMI signals are included as part of the PCIe DC specifications and AC specifications.

5.2.2 Overshoot/Undershoot Tolerance

Overshoot (or undershoot) is the absolute value of the maximum voltage above or below VSS, see Figure 5-7. The overshoot/undershoot specifications limit transitions beyond specified maximum voltages or VSS due to the fast signal edge rates. The processor can be damaged by single and/or repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (i.e., if the over/undershoot is great enough). Baseboard designs which meet signal integrity and timing requirements and which do not exceed the maximum overshoot or undershoot limits listed in Table 5-10 will ensure reliable I/O performance for the lifetime of the processor.

5.2.2.1 Overshoot/Undershoot Magnitude

Magnitude describes the maximum potential difference between a signal and its voltage reference level. For the processor, both are referenced to VSS. It is important to note that the overshoot and undershoot conditions are separate and their impact must be determined independently.

The pulse magnitude and duration must be used to determine if the overshoot/undershoot pulse is within specifications.

5.2.2.2 Overshoot/Undershoot Pulse Duration

Pulse duration describes the total amount of time that an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage. The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

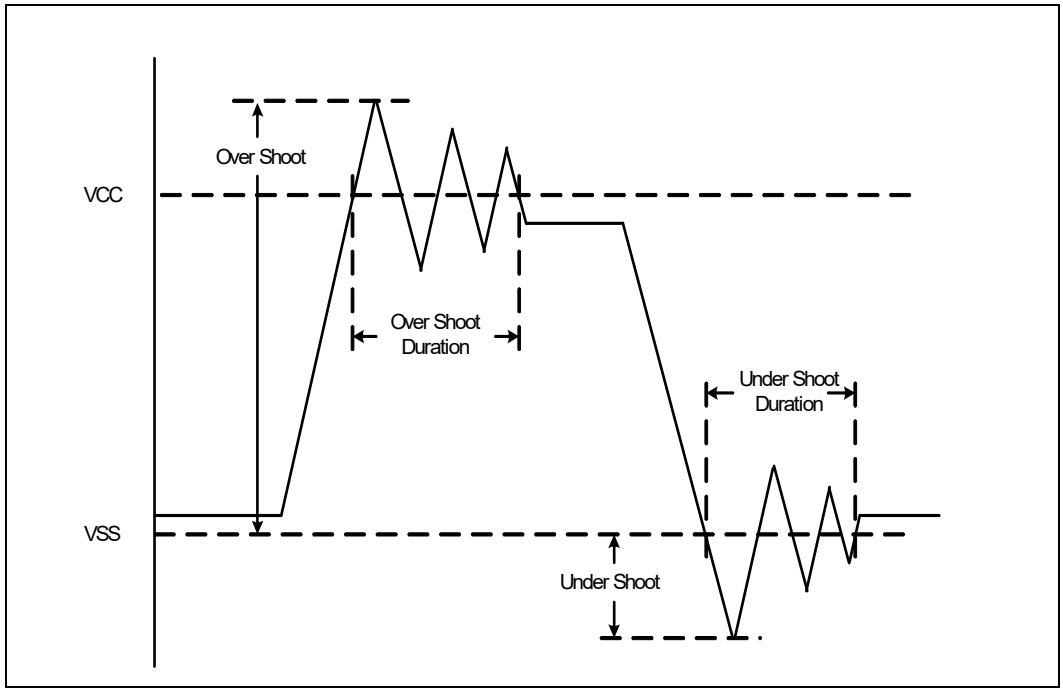
Note: Oscillations below the reference voltage cannot be subtracted from the total overshoot/undershoot pulse duration.

Table 5-10. Processor I/O Overshoot/Undershoot Specifications

Signal Group	Maximum Undershoot	Maximum Overshoot	Overshoot Duration	Undershoot Duration	Notes[1, 2]
DDR4 Command, Data, Clocks	-0.22 * VCCD	1.22 * VCCD	0.25 * T_{CH}	0.1 * T_{CH}	3
DDR4 Miscellaneous, SMBus, PECI, JTAG and TAP, SVID, and Processor Asynchronous Sideband Signals (reference voltage is VCCU)	-0.25V	1.25V	1.25ns	0.5ns	
System Reference Clock (BCLK)	-0.3V	1.15V	N/A	N/A	
CD Reference Clock (CD_HFI_REFCLK)	-0.5V	1.98V	N/A	N/A	
CD Sideband Signals	-0.5V	VCCH_2P5 + 1.4V	N/A	N/A	
CD JTAG	-0.5V	VCCH_1P8 + 1.4V	N/A	N/A	

Notes:
1. These specifications are measured at the processor pad.
2. Refer to Figure 5-7 for description of allowable overshoot/undershoot magnitude and duration.
3. T_{CH} is the minimum high pulse width duration.

Figure 5-7. Maximum Acceptable Overshoot/Undershoot Waveform



§