Intel® Celeron® Processor 550
Datasheet Addendum

Addendum for Intel Celeron Processor 500 Series Datasheet

For Platforms Based on Mobile Intel® 965 Express Chipset Family

January 2008

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Revision History

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1 Introduction

This document is an addendum to the *datasheet* for the Intel® Celeron® processor 500 series for platforms based on Mobile Intel® 965 Express Chipset family. It is based on the new Intel® Core™ microarchitecture.

In this document, the Celeron processor 500 series will be referred to as the Celeron processor, or simply the processor.

This document adds the 479-pin uFCBGA packaging diagrams that are supported for Intel embedded customers.

The following list provides some of the key features of this processor:

- Single core
- On-die, primary 32-kB instruction cache and 32-kB write-back data cache
- On-die, 1-MB second level shared cache with advanced transfer cache architecture
- 533-MHz source-synchronous front side bus (FSB)
- Supports Intel® architecture with dynamic execution
- Data prefetch logic
- Micro-FCPGA and Micro-FCBGA packaging technology
- MMX™ technology, Streaming SIMD Extensions (SSE), Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3), and Supplemental Streaming SIMD Extensions 3 (SSSE 3)
- Digital Thermal Sensor (DTS)
- Execute Disable Bit support for enhanced security
- Intel® 64 architecture (formerly Intel® EM64T)
- Architectural and performance enhancements of the Core microarchitecture.

Note: Unless specified otherwise, all references to the Celeron processor in this document are references to the Celeron processor 500 series with a 533-MHz FSB on Mobile Intel 965 Express Chipset family-based systems.

1.1 Terminology

Term	Definition
#	A "#" symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as address or data), the "#" symbol implies that the signal is inverted. For example, D[3:0] = "HLHL" refers to a hex 'A', and D[3:0]# = "LHLH" also refers to a hex "A" (H= High logic level, L= Low logic level). XXXX means that the specification or value is yet to be determined.
Front Side Bus (FSB)	Refers to the interface between the processor and system core logic (also known as the chipset components).
AGTL+	Advanced Gunning Transceiver Logic. Used to refer to Assisted GTL+ signaling technology on some Intel processors.
Storage Conditions	Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor lands should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
Processor Core	Processor core die with integrated L1 and L2 cache. All AC timing and signal integrity specifications are at the pads of the processor core.
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture.
V_{CC}	The processor core power supply
V_{SS}	The processor ground

1.2 References

Material and concepts in the following documents may be beneficial when reading this document.The reference materials without order numbers have not been released at the time of publication.

Document	Location
Intel® Celeron® Processor 500 Series Datasheet	http://www.intel.com/design/mobile/datashts/317666.htm

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2 Package Mechanical Specifications and Pin Information

2.1 Package Mechanical Specifications

The Celeron processor 550 series will have two variants, both may be available in a 478-pin Micro-FCPGA (not shown in this addendum, see *Intel Celeron Processor 500 Series Datasheet* for reference) or 479-pin Micro-FCBGA package (illustrated in this addendum). Package mechanical dimensions are shown in Figure 1 for the 1 MB configured variant and Figure 3 for the 1 MB variant.

2.1.1 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Decoupling capacitors are typically mounted in the keep-out areas. The location and quantity of the capacitors may change but will remain within the component keep-in. See Figure 2 and Figure 4 for keep-out zones.

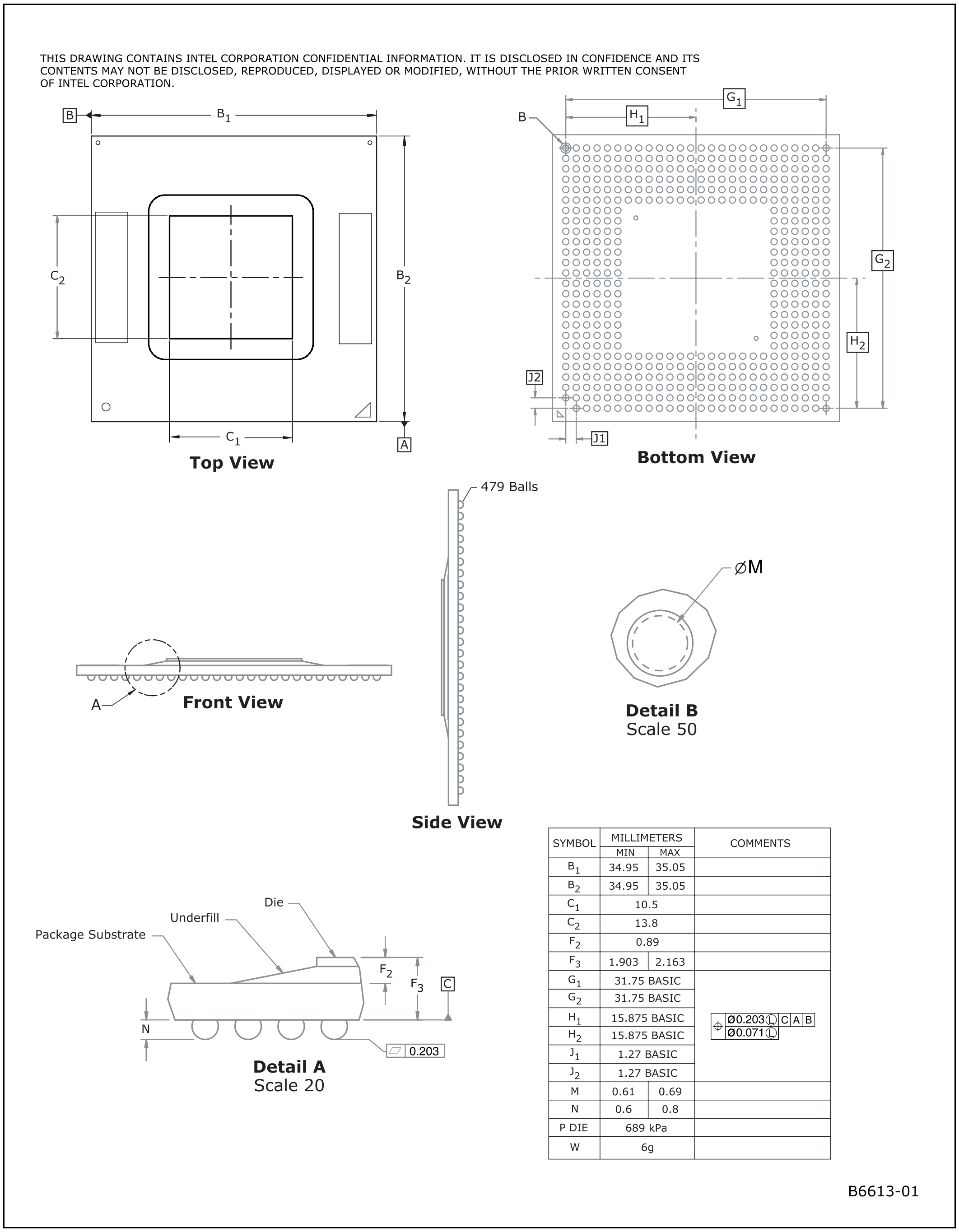
2.1.2 Package Loading Specifications

Maximum mechanical package loading specifications are given in Figure 1 and Figure 3 for the 1 MB configured variant and 1 MB variant respectively. These specifications are static compressive loading in the direction normal to the processor. This maximum load limit should not be exceeded during shipping conditions, standard use condition, or by the thermal solution. In addition, there are additional load limitations against transient bend, shock, and tensile loading. These limitations are more platform specific and should be obtained by contacting your field support. Moreover, the processor package substrate should not be used as a mechanical reference or load-bearing surface for the thermal or mechanical solution.

2.1.3 Processor Mass Specifications

The typical mass of the 1 MB configured variant and 1 MB variant is shown in Figure 1 and Figure 3. This mass includes all the components that are included in the package.

Figure 1. 1 MB Configured Micro-FCBGA Processor Package Drawing (1 of 2)



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SYMBOL	MILLIMETERS		COMMENTS
	MIN	MAX	
B_1	34.95	35.05	
B_2	34.95	35.05	
C_1	10.5		
C_2	13.8		
F_2	0.89		
F_3	1.903	2.163	
G_1	31.75 BASIC		⌖ Ø0.203 Ⓛ | C | A | B Ø0.071 Ⓛ
G_2	31.75 BASIC		
H_1	15.875 BASIC		
H_2	15.875 BASIC		
J_1	1.27 BASIC		
J_2	1.27 BASIC		
M	0.61	0.69	
N	0.6	0.8	
P DIE	689 kPa		
W	6g		

Figure 2. 1 MB Configured Micro-FCBGA Processor Package Drawing (2 of 2)

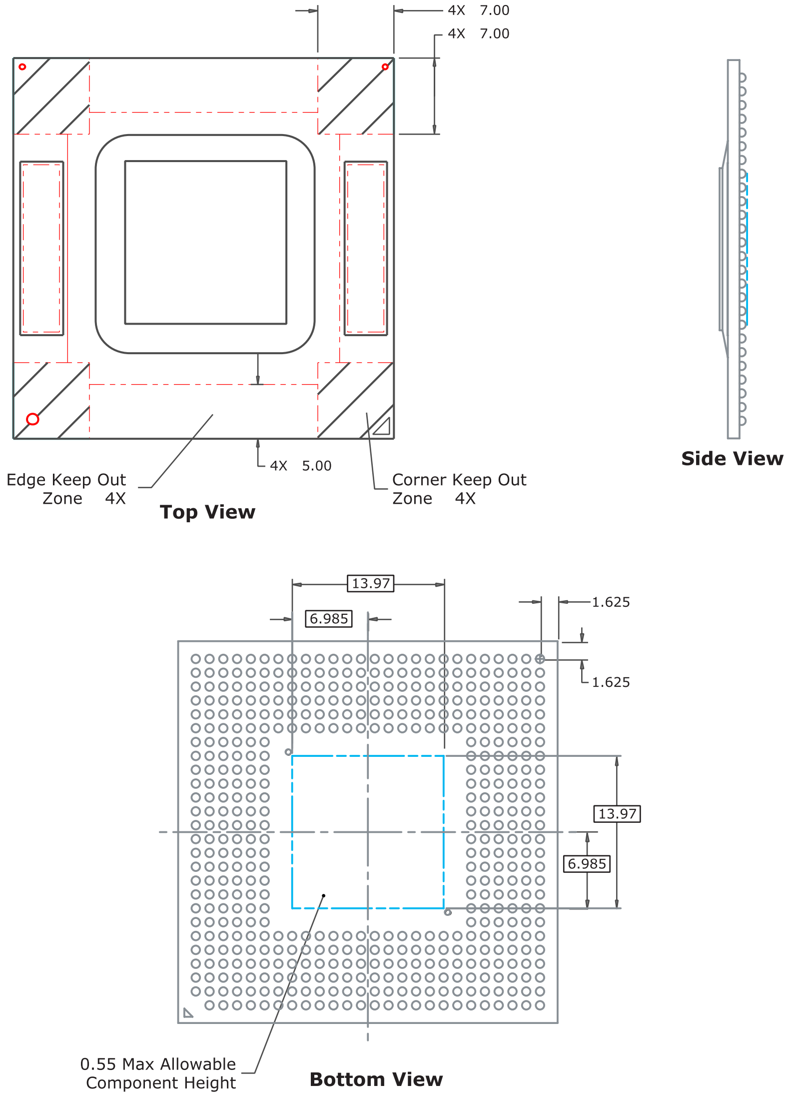
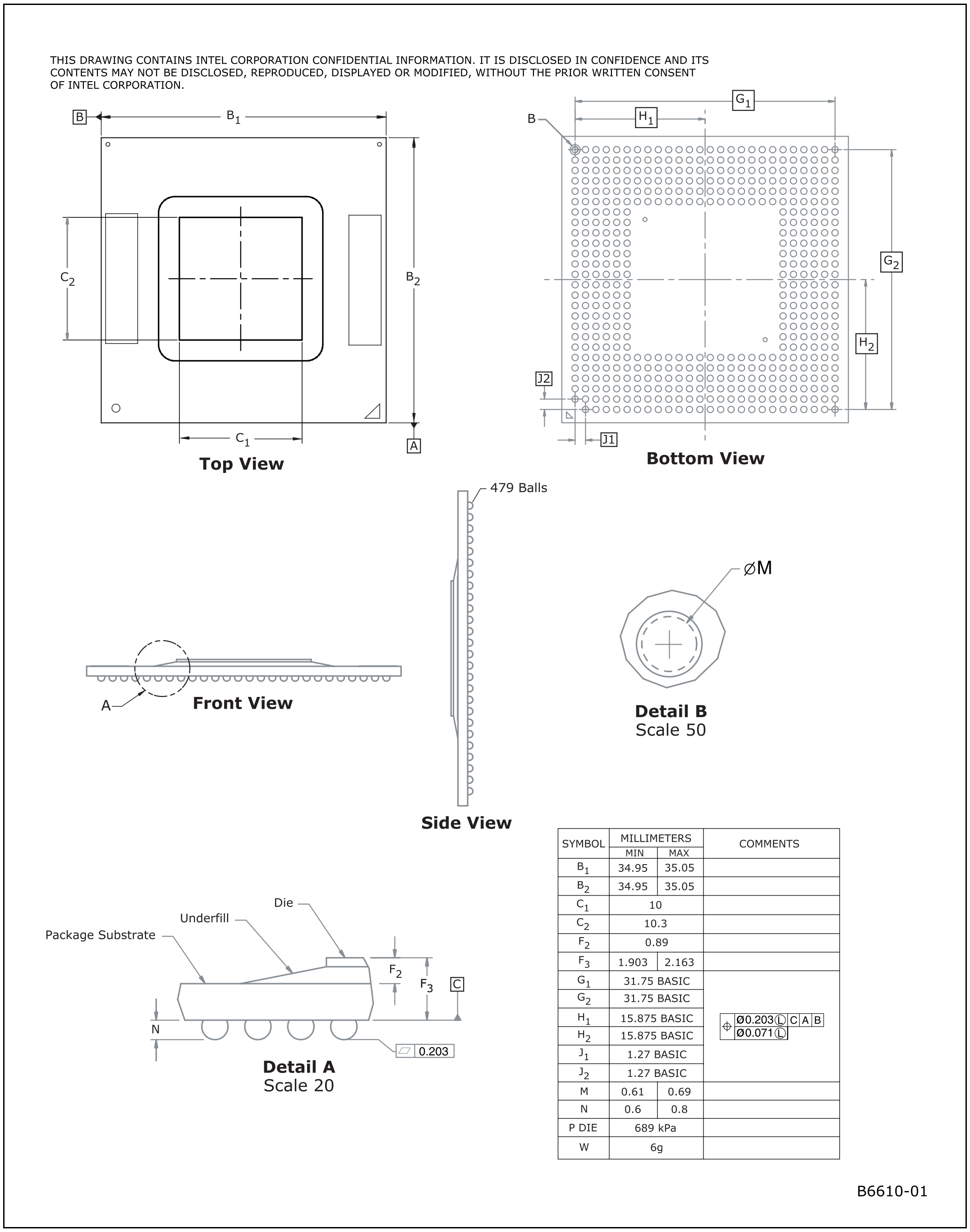


Figure 3. 1 MB Micro-FCBGA Processor Package Drawing (1 of 2)



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SYMBOL	MILLIMETERS MIN	MILLIMETERS MAX	COMMENTS
B_1	34.95	35.05	
B_2	34.95	35.05	
C_1	10		
C_2	10.3		
F_2	0.89		
F_3	1.903	2.163	
G_1	31.75 BASIC		
G_2	31.75 BASIC		
H_1	15.875 BASIC		⌖ Ø0.203Ⓛ C A B Ø0.071Ⓛ
H_2	15.875 BASIC		
J_1	1.27 BASIC		
J_2	1.27 BASIC		
M	0.61	0.69	
N	0.6	0.8	
P DIE	689 kPa		
W	6g		

Figure 4. 1 MB Micro-FCBGA Processor Package Drawing (2 of 2)