# Intel Atom ${ }^{\circledR}$ Processor E3900 and A3900 Series <br> Datasheet Addendum 

July 2019

Revision 004

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## Revision History

| Date | Revision | Description |
| :---: | :---: | :---: |
| July 2019 | 004 | - Updated Table 1, with Z-height value corrected from 2.426 mm to 2.422 mm <br> - Updated Table 14, GPIO Multiplexing for Fn1-Fn4 signal |
| May 2019 | $003$ | - Updated Table 1 for Graphics and Imaging Interface. <br> - Added Table 3. Intel Atom ${ }^{\circledR}$ E3900 Processor Series (F-1 stepping) SKU List. <br> - Added Table 5. Intel Atom ${ }^{\circledR}$ A3900 Processor Series (F-1 Stepping) SKU List. <br> - Replaced Figure 1. Processor Block Diagram. <br> - Added notes no. 2 under Table 10. <br> - Updated VCC-3P3C-A in Table 20. <br> - Added Pin Number 'P57' in Table 24. |
| October 2018 | $002$ | - Updated Table 1 with Still and Video column changed to Still Capture and Video Capture in Imaging (CSI D-PHY 1.1) and (CSI D-PHY 1.1). <br> - Updated Table 2 by adding LPDDR4 frequency. <br> - Updated Table 3 by adding A3920 SKU info and LPDDR4 frequency. <br> - Updated Table 9 for GPIO_112 until GPIO_117 by adding (Fn2). <br> - Added notes no. 5 under Table 9. <br> - Updated Table 13 by adding Vil. <br> - Changed Table 15 for Data Rate from 104 MB to 100 MB. <br> - Updated Table 16 for SDR104. <br> - Updated Table 19 for Storage - SDIO. <br> - Changed section 3.7 from Time Coordinated Computing (TCC) to Spread Spectrum Clocking for EMI mitigation. <br> - Updated Table 22 by adding A3920 SKU. <br> - Added section 5.1 Package Mechanical Drawing. |
| July 2017 | 001 | - Initial release. |

Introduction

### 1.0 Introduction

This Datasheet Addendum is a supplement to the Intel ${ }^{\ominus}$ Pentium ${ }^{\circledR}$ and Celeron ${ }^{\ominus}$
Processor N- and J- Series Datasheet Volume 1 of 3 (Document Number: 334817). This addendum contains additional information pertinent to the implementation and operation of the Intel Atom ${ }^{\circledR}$ processor E3900 and A3900 series.

The processor is the Intel ${ }^{\ominus}$ architecture processor that integrates the next-generation Intel processor core, graphics, memory controller, and I/O interfaces into a single system-on-chip solution.

Register information for the Intel Atom ${ }^{\circledR}$ processor E3900 and A3900 series is the same as that of the N - and J - Series Processors. Refer to Intel ${ }^{\oplus}$ Pentium ${ }^{\oplus}$ and Celeron ${ }^{\ominus}$ Processor N - and J- Series Datasheet Volume 2 of 3 (Document Number: 334818) and Intel ${ }^{\oplus}$ Pentium ${ }^{\ominus}$ and Celeron ${ }^{\oplus}$ Processor N - and J- Series Datasheet Volume 3 of 3 (Document Number: 334819).

Table 1. Intel Atom ${ }^{\ominus}$ Processor E3900 and A3900 Series Features

| Interface | de Category | Intel Atom ${ }^{\oplus}$ Processor E3900 and A3900 Series |
| :---: | :---: | :---: |
|  | Number of Cores | Refer to Table 2 and Table 4 for details |
|  | Burst Speed | Refer to Table 2 and Table 4 for details |
|  | LFM/HFM | Refer to Table 2 and Table 4 for details |
|  | Junction Temperature Tj | $-40^{\circ} \mathrm{C}$ to $110^{\circ} \mathrm{C}$ |
|  | Temperature Tcase (E3930) | $-40^{\circ} \mathrm{C}$ to $103^{\circ} \mathrm{C}$ |
|  | Temperature Tcase (E3940) | $-40^{\circ} \mathrm{C} \text { to } 100^{\circ} \mathrm{C}$ |
|  | Temperature Tcase (E3950) | $-40^{\circ} \mathrm{C} \text { to } 98^{\circ} \mathrm{C}$ |
|  | Temperature Tcase <br> (A3930) | $-40^{\circ} \mathrm{C}$ to $103^{\circ} \mathrm{C}$ |
|  | Temperature Tcase (A3940) | $-40^{\circ} \mathrm{C}$ to $101^{\circ} \mathrm{C}$ |
|  | Temperature Tcase (A3950) | $-40^{\circ} \mathrm{C} \text { to } 100^{\circ} \mathrm{C}$ |
|  | Temperature Tcase (A3960) | $-40^{\circ} \mathrm{C} \text { to } 98^{\circ} \mathrm{C}$ |



## Introduction



| Interface | e Category | Intel Atom ${ }^{\oplus}$ Processor E3900 and A3900 Series |
| :---: | :---: | :---: |
| Storage | SD* Card | Same as the N - and J- Series Processors |
|  | Maximum SD Card Speed | Same as the N - and J- Series Processors |
|  | eMMC* | Same as the N - and J- Series Processors |
|  | Maximum eMMC Speed | Same as the N - and J- Series Processors |
|  | Secure Digital I/O (SDIO) | 1 port |
|  | Maximum SDIO Speed | UHS-I at SDR 104/50/25/12 and DDR50 |
| Low-Power Subsystem (LPSS) | $1^{2} \mathrm{C}^{*}$ Ports | Same as the N- and J- Series Processors |
|  | Maximum $I^{2} \mathrm{C}$ Speed | Same as the N - and J- Series Processors |
|  | High-Speed UART (HSUART) (Maximum) | 4 <br> [1x Discrete GNSS (UART1), $1 \times$ Host OS Debug <br> (UART2) and $2 x$ Generic (UARTO and 3)] |
|  | Maximum HSUART Speed | Same as the N - and J- Series Processors |
|  | Serial Peripheral Interface (SPI) (Maximum) | Controller: 3 <br> Devices supported: 7 |
|  | Maximum SPI Speed | Same as the N- and J- Series Processors |
| Integrated <br> Sensor Hub (ISH) | $1^{2} \mathrm{C}$ | Same as the N - and J- Series Processors |
|  | Maximum $I^{2} \mathrm{C}$ Speed | Same as the N- and J- Series Processors |
|  | GPIO | Same as the N - and J- Series Processors |
| Intel Legacy Block (iLB) | Fast SPI | Same as the N - and J-Series Processors |
|  | Maximum Fast SPI Frequency | Same as the N - and J-Series Processors |
| Power Management Controller (PMC) | $1^{2} \mathrm{C}$ (PMIC) | Same as the N - and J-Series Processors |
|  | Maximum $I^{2} \mathrm{C}$ Speed | Same as the N- and J-Series Processors |
| Low Pin Count (LPC) | Number of Ports | Same as the N - and J-Series Processors |
|  | Maximum Speed | Same as the N - and J- Series Processors |
| System Management Bus (SMBus) | Number of Ports | Same as the N- and J- Series Processors |
|  | Maximum Speed | Same as the N - and J-Series Processors |

NOTE: Depending on Stock Keeping Unit (SKU).

## Introduction

### 1.1 SKU List

Table 2. Intel Atom ${ }^{\ominus}$ E3900 Processor Series (D-O stepping) SKU List


Table 3. Intel Atom ${ }^{\circledR}$ E3900 Processor Series (F-1 stepping) SKU List

| Un | $\begin{aligned} & \text { Intel Atom } \\ & \text { x5 E3930 } \end{aligned}$ | Intel Atom <br> x5 E3940 | Intel Atom ${ }^{\ominus}$ x7 E3950 |
| :---: | :---: | :---: | :---: |
| SSPEC/QDF | REKA | REK6 | REK9 |
| MM\# | 983202 | 983195 | 983200 |
| Stepping | F-1 | F-1 | F-1 |
| No. of Cores | 2 | 4 | 4 |
| Processor Frequency LFM/HFM/ Burst | $\begin{gathered} 800 \mathrm{MHz} / \\ 1.3 \mathrm{GHz} \text { / } \\ 1.8 \mathrm{GHz} \end{gathered}$ | $\begin{gathered} 800 \mathrm{MHz} \text { / } \\ 1.6 \mathrm{GHz} \text { / } \\ 1.8 \mathrm{GHz} \end{gathered}$ | $\begin{gathered} 800 \mathrm{MHz} \text { / } \\ 1.6 \mathrm{GHz} / \\ 2.0 \mathrm{GHz} \end{gathered}$ |


| $\operatorname{tin}$ | $\begin{aligned} & \text { Intel Atom }{ }^{\circ} \\ & \text { x5 E3930 } \end{aligned}$ | $\begin{aligned} & \text { Intel Atom } \\ & \times 5 \text { E3940 } \end{aligned}$ | $\begin{aligned} & \text { Intel Atom® } \\ & \text { x7 E3950 } \end{aligned}$ |
| :---: | :---: | :---: | :---: |
| Graphics Frequency LFM/HFM/ Burst | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 400 \mathrm{MHz} / 550 \\ & \mathrm{MHz} \end{aligned}$ | 100 MHz / <br> 400 MHz / <br> 600 MHz | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 500 \mathrm{MHz} \text { / } \\ & 650 \mathrm{MHz} \end{aligned}$ |
| ISP Frequency Low/High/Burst | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} / 675 \\ & \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} / \\ & 675 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} / \\ & 700 \mathrm{MHz} \end{aligned}$ |
| GFX Industrial Reliability Frequency | 400 MHz | 400 MHz | 400 MHz |
| GFX EU | 12 | 12 | 18 |
| TDP (W) at TjMax | 6.5 | 9.5 | 12 |
| Soi3 Power (mW) at $30^{\circ} \mathrm{C}$ | 15 | 15 | 18 |
| S3 Power (mW) at $30^{\circ} \mathrm{C}$ | 13 | 13 | 16 |
| S5 Power (mW) at $30^{\circ} \mathrm{C}$ | 13 | 13 | 16 |
| DDR3L ECC Option | Yes | Yes | Yes |
| LPDDR4 Frequency | $\begin{gathered} \text { up to } 2133 \\ \mathrm{MT} / \mathrm{s} \end{gathered}$ | $\begin{gathered} \text { up to } 2133 \\ \mathrm{MT} / \mathrm{s} \end{gathered}$ | $\begin{gathered} \text { up to } 2400 \\ \mathrm{MT} / \mathrm{s} \end{gathered}$ |

Table 4. Intel Atom ${ }^{\ominus}$ A3900 Processor Series (D-0 stepping) SKU List

| $e^{i k}$ | Intel Atom ${ }^{\oplus}$ x7 A3920 | $\begin{aligned} & \text { Intel } \\ & \text { Atom } \times 5 \\ & \text { A3930 } \end{aligned}$ | Intel Atom ${ }^{\oplus}$ x5 A3940 | Intel Atom ${ }^{\oplus}$ x7 A3950 | Intel <br> Atom ${ }^{6} \times 7$ <br> A3960 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SSPEC | REJZ | R33R | R33L | R33N | R33U |
| MM\# | 953085 | 953087 | 953082 | 953084 | 953096 |
| Stepping | D-0 | D-0 | D-0 | D-0 | D-0 |
| No. of Cores | 4 | 2 | 4 | 4 | 4 |
| Processor Frequency <br> LFM/HFM/ Burst | $\begin{gathered} 800 \mathrm{MHz} \text { / } \\ 1.6 \mathrm{GHz} / \\ 2.08 \mathrm{GHz} \end{gathered}$ | $\begin{gathered} 800 \mathrm{MHz} / \\ 1.3 \mathrm{GHz} / \\ 1.8 \mathrm{GHz} \end{gathered}$ | $\begin{gathered} 800 \mathrm{MHz} \text { / } \\ 1.6 \mathrm{GHz} \text { / } \\ 1.8 \mathrm{GHz} \end{gathered}$ | $\begin{gathered} 800 \mathrm{MHz} / \\ 1.6 \mathrm{GHz} / \\ 2.0 \mathrm{GHz} \end{gathered}$ | $\begin{gathered} 800 \mathrm{MHz} \text { / } \\ 1.9 \mathrm{GHz} / \\ 2.4 \mathrm{GHz} \end{gathered}$ |
| Graphics Frequency LFM/HFM/ Burst | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 500 \mathrm{MHz} / \\ & 650 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 400 \mathrm{MHz} / \\ & 550 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 400 \mathrm{MHz} / \\ & 600 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 500 \mathrm{MHz} / \\ & 650 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 600 \mathrm{MHz} / \\ & 750 \mathrm{MHz} \end{aligned}$ |
| ISP Frequency Low/High/Burst | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} / \\ & 700 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} \text { / } \\ & 675 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} \text { / } \\ & 675 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} \text { / } \\ & 700 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} / \\ & 700 \mathrm{MHz} \end{aligned}$ |
| GFX Industrial Reliability Frequency | $\begin{aligned} & 400 \\ & \mathrm{MHz} \end{aligned}$ | NA | NA | NA | NA |
| GFX EU | 18 | 12 | 12 | 18 | 18 |
| TDP (W) at TjMax | 12 | 6 | 8 | 9.5 | 12.5 |
| S0i3 Power (mW) at $30^{\circ} \mathrm{C}$ | 18 | 8 15 | 15 | 18 | 18 |

Introduction

|  | Intel <br> Atom ${ }^{\circledR}$ x7 <br> A3920 | Intel Atom ${ }^{\circledR}$ x5 A3930 | Intel <br> Atom ${ }^{\oplus}$ x 5 <br> A3940 | Intel Atom ${ }^{\bullet}$ x7 <br> A3950 | Intel Atom ${ }^{\oplus}$ x7 <br> A3960 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| S3 Power ( mW ) at $30^{\circ} \mathrm{C}$ | 16 | 13 | 13 | 16 | 12 |
| S5 Power (mW) at $30^{\circ} \mathrm{C}$ | 16 | 13 | 13 | 16 | 12 |
| DDR3L ECC Option | No | No | No | No | No |
| AEC-Q100 Qualification | No | Yes | Yes | Yes | Yes |
| LPDDR4 Frequency | up to 2400 MT/s | $\begin{gathered} \text { up to } 2133 \\ \mathrm{MT} / \mathrm{s} \end{gathered}$ | $\begin{gathered} \text { up to } 2133 \\ \mathrm{MT} / \mathrm{s} \end{gathered}$ | $\begin{gathered} \text { up to } 2400 \\ \mathrm{MT} / \mathrm{s} \end{gathered}$ | $\begin{gathered} \text { up to } 2400 \\ \mathrm{MT} / \mathrm{s} \end{gathered}$ |

## NOTES:

1. Intel Atom ${ }^{\ominus}$ processor A3900 series are for automotive customers only. No support for nonautomotive customers.
2. Intel Atom ${ }^{\circledR}$ A3900 Processor Series (D-O stepping) SKU List for Tray Pack.

|  | Intel <br> Atom ${ }^{\ominus}$ x 5 <br> A3930 | $\begin{aligned} & \text { Intel } \\ & \text { Atom } \times 5 \\ & \text { A3940 } \end{aligned}$ | $\begin{aligned} & \text { Intel } \\ & \text { Atom }{ }^{\ominus} \times 7 \\ & \text { A3950 } \end{aligned}$ | Intel <br> Atom ${ }^{\text {© }}$ x7 <br> A3960 |
| :---: | :---: | :---: | :---: | :---: |
| SSPEC | R3VK | R3VH | R3VJ | R3VL |
| MM\# +e | 962843 | $\begin{gathered} 96284 \\ 1 \end{gathered}$ | 962842 | $\begin{gathered} 96284 \\ 4 \end{gathered}$ |
| Tray / T\&R | T\&R | T\&R | T\&R | T\&R |
| Stepping | D-0 | D-0 | D-0 | D-0 |
| No. of Cores | 2 | 4 | 4 | 4 |
| Processor Frequency LFM/HFM/ Burst | $\begin{gathered} 800 \mathrm{MHz} / \\ 1.3 \mathrm{GHz} / \\ 1.8 \mathrm{GHz} \end{gathered}$ | $\begin{gathered} 800 \mathrm{MHz} \text { / } \\ 1.6 \mathrm{GHz} / \\ 1.8 \mathrm{GHz} \end{gathered}$ | $\begin{gathered} 800 \mathrm{MHz} \text { / } \\ 1.6 \mathrm{GHz} / \\ 2.0 \mathrm{GHz} \end{gathered}$ | $\begin{gathered} 800 \mathrm{MHz} / \\ 1.9 \mathrm{GHz} / \\ 2.4 \mathrm{GHz} \end{gathered}$ |
| Graphics Frequency LFM/HFM/ Burst | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 400 \mathrm{MHz} / \\ & 550 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 400 \mathrm{MHz} / \\ & 600 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 500 \mathrm{MHz} / \\ & 650 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 600 \mathrm{MHz} / \\ & 750 \mathrm{MHz} \end{aligned}$ |
| ISP Frequency Low/High/Burst | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} / \\ & 675 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} \text { / } \\ & 675 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} / \\ & 700 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} / \\ & 700 \mathrm{MHz} \end{aligned}$ |
| GFX Industrial Reliability Frequency | NA | NA | NA | NA |
| GFX EU | 12 | 12 | 18 | 18 |
| TDP (W) at TjMax | 6 | 8 | 9.5 | 12.5 |
| S0i3 Power (mW) at $30^{\circ} \mathrm{C}$ | 15 | 15 | 18 | 18 |
| S3 Power (mW) at $30^{\circ} \mathrm{C}$ | 13 | 13 | 16 | 12 |
| S5 Power (mW) at $30^{\circ} \mathrm{C}$ | 13 | 13 | 16 | 12 |
| DDR3L ECC Option | No | No | No | No |


|  | Intel <br> Atom ${ }^{\oplus}$ x5 <br> A3930 | Intel <br> Atom ${ }^{\circledR}$ x5 <br> A3940 | Intel Atom ${ }^{\ominus}$ x7 A3950 | Intel <br> Atom ${ }^{\bullet}$ x7 <br> A3960 |
| :---: | :---: | :---: | :---: | :---: |
| AEC-Q100 Qualification | Yes | Yes | Yes | Yes |
| LPDDR4 Frequency | $\begin{gathered} \text { up to } 2133 \\ \text { MT/s } \end{gathered}$ | $\begin{gathered} \text { up to } 2133 \\ \text { MT/s } \end{gathered}$ | $\begin{gathered} \text { up to } 2400 \\ \mathrm{MT} / \mathrm{s} \end{gathered}$ | $\begin{gathered} \text { up to } 2400 \\ \mathrm{MT} / \mathrm{s} \end{gathered}$ |

NOTE: Intel Atom ${ }^{\ominus}$ Processor A3900 series (D-0 stepping) SKU List for Tape \& Reel Pack.

Table 5. Intel Atom ${ }^{\oplus}$ A3900 Processor Series (F-1 stepping) SKU List

|  | $\begin{aligned} & \text { Intel Atom }{ }^{\ominus} \\ & \text { x5 A3930 } \end{aligned}$ | Intel <br> Atom ${ }^{\oplus}$ x5 <br> A3940 | $\begin{aligned} & \text { Intel } \\ & \text { Atom }{ }^{\oplus} \text { x7 } \\ & \text { A3950 } \end{aligned}$ | Intel Atom ${ }^{\oplus}$ x7 <br> A3960 |
| :---: | :---: | :---: | :---: | :---: |
| SSPEC | REKC | REK4 | REK7 | REKE |
| MM\# | 983207 | 983193 | 983198 | 983210 |
| Stepping | F-1 | F-1 | F-1 | F-1 |
| No. of Cores | 2 | 4 | 4 | 4 |
| Processor Frequency LFM/HFM/ Burst | $\begin{gathered} 800 \mathrm{MHz} \text { / } \\ 1.3 \mathrm{GHz} \text { / } \\ 1.8 \mathrm{GHz} \end{gathered}$ | $\begin{gathered} 800 \mathrm{MHz} \text { / } \\ 1.6 \mathrm{GHz} \text { / } \\ 1.8 \mathrm{GHz} \end{gathered}$ | $\begin{gathered} 800 \mathrm{MHz} \text { / } \\ 1.6 \mathrm{GHz} \text { / } \\ 2.0 \mathrm{GHz} \end{gathered}$ | $\begin{gathered} 800 \mathrm{MHz} / \\ \text { 1.9 GHz / } \\ 2.4 \mathrm{GHz} \end{gathered}$ |
| Graphics Frequency LFM/HFM/ Burst | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 400 \mathrm{MHz} \text { / } \\ & 550 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 400 \mathrm{MHz} / \\ & 600 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 500 \mathrm{MHz} \text { / } \\ & 650 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 600 \mathrm{MHz} / \\ & 750 \mathrm{MHz} \end{aligned}$ |
| ISP Frequency Low/High/Burst | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} \text { / } \\ & 675 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} / \\ & 675 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} \text { / } \\ & 700 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} / \\ & 700 \mathrm{MHz} \end{aligned}$ |
| GFX EU | 812 | 12 | 18 | 18 |
| TDP (W) at TjMax | 6 | 8 | 9.5 | 12.5 |
| S0i3 Power (mW) at $30^{\circ} \mathrm{C}$ | 15 | 15 | 18 | 18 |
| S3 Power (mW) at $30^{\circ} \mathrm{C}$ | 13 | 13 | 16 | 12 |
| S5 Power ( mW ) at $30^{\circ} \mathrm{C}$ | 13 | 13 | 16 | 12 |
| DDR3L ECC Option | No | No | No | No |
| AEC-Q100 Qualification | Yes | Yes | Yes | Yes |
| LPDDR4 Frequency | up to 2133 MT/s | up to 2133 MT/s | up to 2400 MT/s | up to 2400 MT/s |

NOTE: Intel Atom ${ }^{\oplus}$ A3900 Processor Series (F-1 stepping) SKU List for Tray Pack.

Introduction

| $e^{e^{8}}$ | $\begin{aligned} & \text { Intel } \\ & \text { Atom }{ }^{\ominus} \times 5 \\ & \text { A3930 } \end{aligned}$ | Intel <br> Atom ${ }^{\circledR}$ x5 <br> A3940 | Intel Atom ${ }^{\oplus}$ x7 A3950 | $\begin{aligned} & \text { Intel } \\ & \text { Atom } \times 7 \\ & \text { A3960 } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: |
| SSPEC | REKD | REK5 | REK8 | REKF |
| MM\# | 983208 | $\begin{gathered} 98319 \\ 4 \end{gathered}$ | 983199 | $\begin{gathered} 98321 \\ 1 \\ \hline \end{gathered}$ |
| Tray / T\&R | T\&R | T\&R | T\&R | T\&R |
| Stepping | F-1 | F-1 | F-1 | F-1 |
| No. of Cores | 2 | 4 | 4 | 4 |
| Processor Frequency LFM/HFM/ Burst | $\begin{gathered} 800 \mathrm{MHz} / \\ 1.3 \mathrm{GHz} / \\ 1.8 \mathrm{GHz} \end{gathered}$ | $\begin{gathered} 800 \mathrm{MHz} / \\ 1.6 \mathrm{GHz} / \\ 1.8 \mathrm{GHz} \end{gathered}$ | $\begin{gathered} 800 \mathrm{MHz} / \\ 1.6 \mathrm{GHz} / \\ 2.0 \mathrm{GHz} \end{gathered}$ | $\begin{gathered} 800 \mathrm{MHz} / \\ 1.9 \mathrm{GHz} / \\ 2.4 \mathrm{GHz} \end{gathered}$ |
| Graphics Frequency LFM/HFM/ Burst | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 400 \mathrm{MHz} / \\ & 550 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 400 \mathrm{MHz} \text { / } \\ & 600 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 500 \mathrm{MHz} / \\ & 650 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 100 \mathrm{MHz} / \\ & 600 \mathrm{MHz} / \\ & 750 \mathrm{MHz} \end{aligned}$ |
| ISP Frequency Low/High/ Burst | $200 \mathrm{MHz} /$ <br> $550 \mathrm{MHz} /$ <br> 675 MHz | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} / \\ & 675 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} / \\ & 700 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 200 \mathrm{MHz} / \\ & 550 \mathrm{MHz} / \\ & 700 \mathrm{MHz} \end{aligned}$ |
| GFXEU | 12 | 12 | 18 | 18 |
| TDP (W) at TjMax | 6 | 8 | 9.5 | 12.5 |
| SOi3 Power (mW) at $30^{\circ} \mathrm{C}$ | 15 | 15 | 18 | 18 |
| S3 Power (mW) at $30^{\circ} \mathrm{C}$ | 13 | 13 | 16 | 12 |
| S5 Power (mW) at $30^{\circ} \mathrm{C}$ | 13 | 13 | 16 | 12 |
| DDR3L ECC Option | No | No | No | No |
| AEC-Q100 Qualification | Yes | Yes | Yes | Yes |
| LPDDR4 Frequency | up to 2133 <br> MT/s | $\begin{gathered} \text { up to } 2133 \\ \mathrm{MT} / \mathrm{s} \\ \hline \end{gathered}$ | up to 2400 <br> MT/s | $\begin{gathered} \text { up to } 2400 \\ \mathrm{MT} / \mathrm{s} \end{gathered}$ |

NOTE: Intel Atom ${ }^{\oplus}$ Processor A3900 series (F-1 stepping) SKU List for Tape \& Reel Pack

### 1.2 Processor Block Diagram

Figure 1. Processor Block Diagram


### 1.3 Terminology

Table 6. Terminology


### 1.4 Reference Documents

Table 7. Reference Documents

| Document | Document No./Location |
| :---: | :---: |
| Intel ${ }^{\oplus}$ Pentium ${ }^{\ominus}$ and Celeron ${ }^{\oplus}$ Processor N - and J-Series Datasheet Volume 1 of 3 | 334817 |
| Intel ${ }^{\oplus}$ Pentium ${ }^{\circledR}$ and Celeron ${ }^{\oplus}$ Processor N - and J-Series Datasheet Volume 2 of 3 | 334818 |
| Intel ${ }^{\oplus}$ Pentium ${ }^{\circledR}$ and Celeron ${ }^{\oplus}$ Processor $N$ - and J-Series Datasheet Volume 3 of 3 | 334819 |
| Intel ${ }^{\ominus}$ Pentium ${ }^{\circledR}$ and Celeron ${ }^{\circledR}$ Processor N - and J-Series Specification Update | 334820 |
| Intel ${ }^{\oplus} 64$ and IA-32 Architectures Software Developer's Manuals <br> Volume 1: Basic Architecture <br> Volume 2A: Instruction Set Reference, A-M <br> Volume 2B: Instruction Set Reference, $N-Z$ <br> Volume 3A: System Programming Guide <br> Volume 3B: System Programming Guide | https://softw are. intel.com/enus/articles/in tel- sdm |

### 2.0 Physical Interfaces

Many interfaces contain physical pins. These groups of pins make up the physical interfaces. Because of the large number of interfaces and the small size of the package, some interfaces share their pins with GPIOs, while others use dedicated physical pins. This chapter summarizes the physical interfaces, including the diversity in GPIO multiplexing options.

### 2.1 PCI Device ID

Table 8. PCI Configuration Matrix

| Device ID | Device Description | Device | Function |
| :--- | :--- | :--- | :--- |
| $0 \times 5 A B C$ | UART 0 | 24 | 0 |
| $0 \times 5 A E E$ | UART 3 | 24 | 3 |
| $0 \times 5 A C 4$ | SPI 1 | 25 | 1 |
| $0 \times 5 A C 6$ | SPI 2 | 25 | 2 |
| 0x5AD0 | SDIO | 30 | 0 |

NOTE: Other PCI Device IDs are the same as those of N - and J-Series Processors. Refer to Intel ${ }^{\circledR}$ Pentium ${ }^{\circledR}$ and Celeron ${ }^{\circledR}$ Processor N - and J- Series Datasheet Volume 1 of 3 (Document Number: 334817).

### 2.2 Memory Interface Signals

Table 9. DDR3L ECC System Memory Signals

| Signal Name | Dir. | I/O <br> Voltage | Type | Description |
| :--- | :--- | :---: | :---: | :--- |
| MEM_CHO_ECC_DQ[7:O] <br> MEM_CH1_ECC_DQ[7:0] | //O | VDDQ | DDR3L <br> PHY | ECC Data Buses: Data <br> signals interface to the <br> Synchronous Dynamic <br> Random Access <br> Memory (SDRAM) data <br> buses. |
| MEM_CHO_ECC_DQSP[8] <br> MEM_CHO_ECC_DQSN[8] <br> MEM_CH1_ECC_DQSP[8] <br> MEM_CH1_ECC_DQSN[8] | I/O | VDDQ | DDR3L | ECC Data Strobes <br> (DQS): Differential <br> data strobe pair. The <br> data is captured at the <br> crossing point of DQS <br> during read and write <br> transactions. |

NOTE: Signal names shown in this table are additional ECC signal names. The rest of the DDR3L signals are the same as those of N - and J - Series Processors.

### 2.3 SDIO Interface Signals

Table 10. SDIO Interface Signals

| Signal Name | GPIO | Dir. | I/O Voltage | Type | Description |
| :--- | :---: | :---: | :---: | :---: | :--- |
| SDIO_CLK | GPIO_166 | I/O | V1P8 | GPIO | SDIO Clock: Port Clock. |
| SDIO_CMD | GPIO_171 | I/O | V1P8 | GPIO | SDIO Command: This signal <br> is used for device <br> initialization and transfer of <br> commands. |
| SDIO_DO <br> SDIO_D1 <br> SDIO_D2 | GPIO_167 <br> GPIO_168 <br> GPIO_169 <br> GPIO_170 | I/O | V1P8 | GPIO | SDIO Data Bits 0 to 3: <br> Bidirectional ports used to <br> transfer data to and from <br> the SDIO device. By default, <br> after power-up or reset, only <br> D D[0] is used for data <br> transfer. A wider data bus <br> can be configured for data <br> transfer, using D [0]-D[3]. |
| SDIO_D3 |  |  | VDIO_PWR_ | GPIO_183 | I/O |
| DOWN_N |  |  |  |  |  |

Physical Interfaces

### 2.4 High-Speed Universal Asynchronous Receiver/Transmitter (UART) Interface Signals

Table 11. UART Interface Signals

| Signal Name | GPIO\# | Dir. | I/O Voltage | Type | Description |
| :---: | :---: | :---: | :---: | :---: | :---: |
| LPSS_UARTO_RXD | GPIO_38 | I | V1P8 | GPIO | UARTO data input |
| LPSS_UARTO_TXD | a GPIO_39 | 0 | V1P8 | GPIO | UARTO data output |
| LPSS_UARTO_RTS_N | GPIO_40 | 0 | V1P8 | GPIO | UARTO <br> Ready to Send |
| LPSS_UARTO_CTS_N | GPIO_41 | I | V1P8 | GPIO | UARTO Clear to Send |
| LPSS_UART1_RXD | GPIO_42 | 1 | V1P8 | GPIO | UART1 data input |
| LPSS_UART1_TXD | GPIO_43 | 0 | V1P8 | GPIO | UART1 <br> data <br> output |
| LPSS_UART1_RTS_N | GPIO_44 | 0 | V1P8 | GPIO | UART1 <br> Ready to Send |
| LPSS_UART1_CTS_N | $\begin{gathered} \text { GPIO_45/GPIO1 } 53 \\ \text { (Fn 3) } \end{gathered}$ | I | V1P8 | GPIO | UART1 Clear to Send |
| LPSS_UART2_RXD | $\begin{gathered} \text { GPIO_46/GPIO_ } 150 \\ \text { (Fn 3) } \end{gathered}$ | 1 | V1P8 | GPIO | UART2 data input |
| LPSS_UART2_TXD | $\begin{gathered} \text { GPIO_47/GPIO_ } 151 \\ \text { (Fn 3) } \end{gathered}$ | 0 | V1P8 | GPIO | UART2 <br> data output |
| LPSS_UART2_RTS_N |  | 0 | V1P8 | GPIO | UART2 <br> Ready to Send |
| LPSS_UART2_CTS_N | GPIO_49 | 1 | V1P8 | GPIO | UART2 Clear to Send |
| LPSS_UART3_RXD | GPIO_112 (Fn2) | 1 | V1P8 | GPIO | UART3 data input |
| LPSS_UART3_TXD | GPIO_113 (Fn2) | 0 | V1P8 | GPIO | UART3 data output |
| LPSS_UART3_RTS_N | GPIO_116 (Fn2) | 0 | V1P8 | GPIO | UART3 <br> Ready to Send |


| Signal Name | GPIO\# | Dir. | I/O Voltage | Type | Description |
| :---: | :---: | :---: | :---: | :---: | :---: |
| LPSS_UART3_CTS_N | GPIO_117 (Fn2) | I | V1P8 | GPIO | UART3 Clear <br> to Send |

## NOTES:

1. The E3900 and A3900 Series Processors support four LPSS_UART ports, while the N- and JSeries Processors support only LPSS_UART [2:1] ports.
2. The LPSS_UART1 port is dedicated for discrete Global Navigation Satellite System (GNSS). This port can be used for generic UART functionality if GNSS is not used.
3. The LPSS_UART2 port is dedicated for host OS debug.
4. The LPSS_UARTO and LPSS_UART3 ports are for generic UART functionality.
5. Only UART [1:0] ports support DMA.

### 2.5 Audio Interface Signals

Table 12. Audio Interface Signals

| Signal Name | GPIO\# | Dir. | I/O Voltage | Type | Description |
| :---: | :---: | :---: | :---: | :---: | :---: |
| AVS_I2S1_MCLK | GPIO_74 | 0 | V1P8 | GPIO | MCLK for Master Mode operation or GPIO |
| AVS_I2S1_BCLK | GPIO_75 | I/O | V1P8 | GPIO | Analog microphone ${ }^{12}$ S Bit Clock bidirectional. In master mode, the BCLK is supplied by the processor; in slave mode, it serves as an input. |
| AVS_I2S1_WS_SYNC | GPIO_76 | I/O | V1P8 | GPIO | Word Select or SYNC input marks the beginning of serial sample. |
| AVS_I2S1_SDI | GPIO_77 | I | V1P8 | GPIO | Analog microphone ${ }^{1}$ S S Data in - serial data input |
| AVS_I2S1_SDO | GPIO_78 | I/O | V1P8 | GPIO | Audio Codec $\mathrm{I}^{2} \mathrm{~S}$ Data out - serial data output |
| AVS_I2S2_MCLK | GPIO_84 | 0 | V1P8 | GPIO | MCLK for Master Mode operation or GPIO |


| Signal Name | GPIO\# | Dir. | I/O Voltage | Type | Description |
| :---: | :---: | :---: | :---: | :---: | :---: |
| AVS_I2S2_BCLK | GPIO_85 | I/O | V1P8 | GPIO | Analog microphone $\mathrm{I}^{2} \mathrm{~S}$ Bit Clock bidirectional. In master mode, the BCLK is supplied by the processor; in slave mode, it serves as an input. |
| AVS_I2S2_WS_SYNC | GPIO_86 | 1/0 | V1P8 | GPIO | Word Select or SYNC input marks the beginning of serial sample. |
| AVS_I2S2_SDI | GPIO_87 | 1 | V1P8 | GPIO | Analog microphone ${ }^{2}$ S Data in - serial data input |
| AVS_I2S2_SDO | GPIO_88 | 1/0 | V1P8 | GPIO | Audio Codec ${ }^{2}{ }^{2} \mathrm{~S}$ Data out - serial data output |
| AVS_I2S3_BCLK | GPIO_89 | 1/0 | V1P8 | GPIO | Audio Codec ${ }^{2}$ S Bit Clock - bidirectional. In master mode, the BCLK is supplied by the processor; in slave mode, it serves as an input. |
| AVS_I2S3_WS_SYNC | GPIO_90 | I/O | V1P8 | GPIO | Audio Codec frame synchronization or word select signal. Bidirectional - may be configured for master or slave. |
| AVS_I2S3_SDI | eGPIO_91 | 1 | V1P8 | GPIO | Audio Codec $\mathrm{I}^{2}$ S Data in <br> - serial data input |
| AVS_I2S3_SDO | GPIO_92 | 1/0 | V1P8 | GPIO | Audio Codec $\mathrm{I}^{2} \mathrm{~S}$ Data out - serial data output |
| AVS_I2S4_BCLK | GPIO_79 | 1/0 | V1P8 | GPIO | Audio Codec ${ }^{2}$ S Bit Clock - bidirectional. In master mode, the BCLK is supplied by the processor; in slave mode, it serves as an input. |


| Signal Name | GPIO\# | Dir. | I/O Voltage | Type | Description |
| :---: | :---: | :---: | :---: | :---: | :---: |
| AVS_I2S4_WS_SYNC | GPIO_80 | I/O | V1P8 | GPIO | Audio Codec frame synchronization or word select signal. Bidirectional - may be configured for master or slave. |
| AVS_I2S4_SDI | GPIO_81 | I | V1P8 | GPIO | Audio Codec $\mathrm{I}^{2} \mathrm{~S}$ Data in <br> - serial data input |
| AVS_I2S4_SDO | GPIO_82 | 1/0 | V1P8 | GPIO | Audio Codec $I^{2} \mathrm{~S}$ Data out - serial data output |
| AVS_I2S5_BCLK | GPIO_150 | I/O | V1P8 | GPIO | Audio Codec ${ }^{2}$ S Sit Clock - bidirectional. In master mode, the BCLK is supplied by the processor; in slave mode, it serves as an input. |
| AVS_I2S5_WS_SYNC | GPIO_151 | 1/0 | V1P8 | GPIO | Audio Codec frame synchronization or Word select signal. Bidirectional - may be configured for master or slave. |
| AVS_I2S5_SDI | GPIO_152 | I | V1P8 | GPIO | Audio Codec ${ }^{2}$ S Data in <br> - serial data input |
| AVS_I2S5_SDO | GPIO_153 | 1/0 | V1P8 | GPIO | Audio Codec $I^{2} \mathrm{~S}$ Data out - serial data output |
| AVS_I2S6_BCLK | GPIO_146 | 1/0 | V1P8 | GPIO | Audio Codec ${ }^{2}$ S Bit Clock - bidirectional. In master mode, the BCLK is supplied by the processor; in slave mode, it serves as an input. |
| AVS_I2S6_WS_SYNC | GPIO_147 | 1/0 | V1P8 | GPIO | Audio Codec frame synchronization or Word select signal. Bidirectional - may be configured for master or slave. |
| AVS_I2S6_SDI | GPIO_148 | 1 | V1P8 | GPIO | Audio Codec I ${ }^{2}$ S Data in <br> - serial data input |

Physical Interfaces

| Signal Name | GPIO\# | Dir. | I/O Voltage | Type | Description |
| :---: | :---: | :---: | :---: | :---: | :---: |
| AVS_I2S6_SDO | GPIO_149 | I/O | V1P8 | GPIO | Audio Codec IS <br> Data out - serial <br> data output |

## NOTES:

1. The E3900 and A3900 Series Processors support six I2S interfaces, while the N - and J- Series Processors support only AVS_I2S2 and AVS_I2S6 interfaces.
2. I2S1_MCLK and I2S2_MCLK can be used respectively for I2S1 and I2S2 interface only.

### 2.6 Serial I/O (SIO) (LPSS) SPI Signals

Table 13. SIO (LPSS) SPI Signals

| Signal Name | GPIO | Dir. | I/O Voltage | Type | Description |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SIO_SPI_O_CLK | GPIO_104 | 1/0 | V1P8 | GPIO | SIO SPI 0 Clock: SPI Clock signal |
| SIO_SPI_O_FSO | GPIO_105 | 0 | V1P8 | GPIO | SIO SPI 0 Frame Select 0: Used as the SPI bus request signal |
| SIO_SPI_0_FS1 | GPIO_106 | 0 | V1P8 | GPIO | SIO SPI 0 Frame Select 1: Used as the SPI bus request signal |
| SIO_SPI_O_RXD | GPIO_109 | 1 | V1P8 | GPIO | SIO SPI 0 Data Pad: Data Input pin for the processor |
| SIO_SPI_O_TXD | GPIO_110 | $0$ | V1P8 | GPIO | SIO SPI 0 Data Pad: Data Output pin for the processor |
| SIO_SPI_1_CLK | GPIO_111 | I/O | V1P8 | GPIO | SIO SPI 1 Clock: SPI Clock signal |
| SIO_SPI_1_FSO | GPIO_112 | 0 | V1P8 | GPIO | SIO SPI 1 Frame Select 0: Used as the SPI bus request signal |
| SIO_SPI_1_FS1 | GPIO_113 | 0 | V1P8 | GPIO | SIO SPI 1 Frame Select 1: <br> Used as the SPI bus request signal |
| SIO_SPI_1_RXD | GPIO_116 | $e^{1}$ | V1P8 | GPIO | SIO SPI 1 Data Pad: Data Input pin for the processor |
| SIO_SPI_1_TXD | GPIO_117 | 0 | V1P8 | GPIO | SIO SPI 1 Data Pad: Data Output pin for the processor |
| SIO_SPI_2_CLK | GPIO_118 | 1/0 | V1P8 | GPIO | SIO SPI 2 Clock: SPI Clock signal |


| Signal Name | GPIO | Dir. | I/O Voltage | Type | Description |
| :--- | :---: | :---: | :---: | :---: | :--- |
| SIO_SPI_2_FSO | GPIO_119 | O | V1P8 | GPIO | SIO SPI 2 Frame Select 0: <br> Used as the SPI bus <br> request signal |
| SIO_SPI_2_FS1 | GPIO_120 | O | V1P8 | GPIO | SIO SPI 2 Frame Select 1: <br> Used as the SPI bus <br> request signal |
| SIO_SPI_2_FS2 | GPIO_121 | O | V1P8 | GPIO | SIO SPI 2 Frame Select 2: <br> Used as the SPI bus <br> request signal |
| SIO_SPI_2_RXD | GPIO_122 | I | V1P8 | GPIO | SIO SPI 2 Data Pad: Data <br> Input pin for the <br> processor |
| SIO_SPI_2_TXD | GPIO_123 | O | V1P8 | GPIO | SIO SPI 2 Data Pad: Data <br> Output pin for the <br> processor |

NOTE: The E3900 and A3900 Series Processors support three SPI ports, while the N - and J-Series Processors support only the SIO_SPI_O port.

Physical Interfaces

### 2.7 GPIO Multiplexing

Table 14. GPIO Multiplexing

| GPIO No. | Signal Name | Process or Pin No. | Community | Community Offset | I/O Voltage | Default Termination | Buffer Type | Default Mode | Fn 1 | Fn 2 | Fn 3 | Fn 4 | Fn 5 | Fn 6 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| GPIO_20 | GPIO_20 | B27 | N | 320 | 1.8 V | 20K PD | HSMV | GP-In | RSVD | RSVD | RSVD | RSVD | IERR | 0 |
| GPIO_21 | GPIO_21 | C26 | N | 336 | 1.8 V | 20K PD | HSMV | GP-In | RSVD | RSVD | RSVD | RSVD | MCERR | 0 |

Intel Atom ${ }^{\circledR}$ Processor E3900 and A3900 Series

## $2.8 \quad$ RTC Signals

In addition to the internal RTC oscillator, an optional mode is available to supply the RTC clock from an external source. In this case, an oscillator or a single clock output can be used to drive into X1 with X2 left as no contact. Contact your Intel representative for more information.

Table 15. RTC Signals

| Signal Name | Dir. | I/O Voltage | Type | Description |
| :---: | :---: | :---: | :---: | :---: |
| RTC_X1 | I | NA | RTC PHY | Crystal Input 1: This signal is connected <br> to a 32.768 kHz crystal (max 50k ESR). <br> If using an external oscillator, the <br> RTC X1 Vih must be within the range of <br> O.8V to 1.5V (1.5V max) and Vil must be <br> within range of -0.2V to 0.2V (0.2V max). |
| RTC_X2 | O | NA | RTC PHY | Crystal Input 2: This signal is connected <br> to a 32.768 kHz crystal (max 50k ESR). <br> If using an external oscillator, RTC_X2 <br> should be left floating. |

## $2.9 \quad$ Other Signals

Other signals that are not mentioned in this document, such as Digital Display Interface and SVID, have the same names as those in Intel ${ }^{\ominus}$ Pentium ${ }^{\ominus}$ and Celeron ${ }^{\ominus}$ Processor N and J- Series Datasheet Volume 1 of 3 (Document Number: 334817).

### 3.0 Functional Description

### 3.1 Processor Core Overview

The processor core for Intel Atom ${ }^{\oplus}$ processor E3900 and A3900 series (formerly Apollo Lake-I) is the same as the processor core for Intel ${ }^{\oplus}$ Pentium ${ }^{\oplus}$ and Celeron ${ }^{\oplus}$ Processor Nand J- Series (formerly Apollo Lake). Figure 2 and Figure 3 show the CPU L2 Cache structure for the dual-core processor and the quad-core processor, respectively.

Note: L1 cache has Parity Protection and L2 cache has ECC Protection.

Figure 2. CPU L2 Cache Structure (Dual Core)


Figure 3. CPU L2 Cache Structure (Quad Core)


### 3.2 System Memory Controller

### 3.2.1 Supported Memory Overview

The processor Integrated Memory Controller (IMC) supports the following memory technologies on two independent 64-bit (72-bit for ECC) channels.

Table 16. Supported Memory Technologies

| Technology Attributes | LPDDR4 | DDR3L | DDR3L ECC |
| :---: | :---: | :---: | :---: |
| Channels | Up to 4 (x32) | Up to 2 (x64) | Up to 2 (x72) |
| Peak Bandwidth (GB/s) | Up to 38.4 | Up to 29.86 | Up to 25.6 |
| Maximum Data Transfer Rate (MT/s) | NOTE | NOTE | 1333/1600 |
| Maximum Total System Capacity | NOTE | NOTE | $8 \text { GB }$ |
| Raw Card Support | NOTE | NOTE | $\begin{aligned} & C(1 R x 8) \\ & D(2 R x 8) \end{aligned}$ |
| Densities (Gb) | NOTE | NOTE | 4, 8 |
| CMD/Adds pins per channel | NOTE | NOTE | 16 |
| DQ pins per channel | NOTE | NOTE | 72 |
| Voltage Rail (V) | NOTE | NOTE | 1.35 |
| Scrambling | Yes ${ }^{\text {a }}$ |  |  |
| On Die Termination Control | Yes |  |  |
| Same Rank Interleaving | Yes |  |  |
| Refresh | No per bank-refresh, only at rank level |  |  |
| Power-Saving Features | Fast Exit Power Down, Self-Refresh plus extra features, Power/Trunk gating |  |  |

NOTE: Same as the N- and J- Series Processors.

### 3.2.2 Memory Configurations

For further information, refer to the Memory Configurations section in Intel ${ }^{\ominus}$ Pentium ${ }^{\circledR}$ and Celeron ${ }^{\oplus}$ Processor N - and J- Series Datasheet Volume 1 of 3 (Document Number: 334817). Disregard the LPDDR3 contents; they are not supported by E3900 and A3900 series processors.

## 3.3

SDIO
The processor has an integrated SDIO controller, which implements the following features.

Note: SD cards are not supported by this interface.

Table 17. SDIO Features

| Category | Feature Supported |
| :--- | :--- |
| Specification | Supports SDIO Specification Version 3.00 |
| Data Rate | Supports up to $100 \mathrm{MB} / \mathrm{s}$ data rate using 4 parallel data lines <br> (SDR104 modes) |
| Transfer Modes | Supports transfer data in 1-bit and 4-bit SD modes |
| Mode of Operation | Supports both ADMA2/DMA and Non-DMA modes of operation |
| Cyclic Redundancy Check | Supports CRC7 for command and CRC16 for data integrity |
| Others | •Supports Async Interrupt Cards <br> $\bullet$ •Supports in-band wake during S0 <br> $\bullet$ •Supports Interrupt Coalescing |

Table 18. SDIO Working Modes

| SDIO Mode | Data Rate | Maximum Clock <br> Frequency | Maximum Data <br> Throughput |
| :--- | :---: | :---: | :---: |
| SDR12 | Single | 25 MHz | $2.5 \mathrm{MB} / \mathrm{s}$ |
| SDR25 | Single | 50 MHz | $25 \mathrm{MB} / \mathrm{s}$ |
| SDR50 | Single | 100 MH | $50 \mathrm{MB} / \mathrm{s}$ |
| DDR50 | Dual | 50 MHz | $50 \mathrm{MB} / \mathrm{s}$ |
| SDR104 | Single | 200 MHz | $100 \mathrm{MB} / \mathrm{s}$ |

### 3.4 Audio Controller

Table 19. Audio Controller Features

| Category | d Description |
| :---: | :---: |
| 12S/SSP Interfaces | Six $1^{2} \mathrm{~S} / \mathrm{SSP}$ interfaces for platform peripherals |
| DSPs | Two high-performance DSPs configured with: <br> - 32kB 4-way set associative L1 Instruction Cache <br> - 64kB 4-way set associative L1 Data Cache |
| L2 | - L2 memory controller with the local highperformance interconnect fabric <br> - L2 cache controller with caching and prefetch capabilities |
| ROM Size | 8kB ROM |
| DMA Interfaces | Two 8-channel universal DMA interfaces to transfer data between memory buffers and peripherals, and between memories |
| DMIC Interfaces | Two dual-channel DMIC interfaces |
| Intel ${ }^{\oplus}$ High Definition Audio (Intel ${ }^{\ominus}$ HD Audio) and LPE Audio | Supports Intel ${ }^{\oplus}$ HD Audio and LPE Audio for DDI [1:0]: DisplayPort* and High Definition Multimedia Interface (HDMI*) |
| CODEC | Supports one external CODEC for attaching audio peripherals |
| Burst Mode | Local power sequencer for burst-mode data processing in micropower modes (SOix) |
| Debug Interface | DSP On-chip Debug interface with two JTAG ports |

## $3.5 \quad$ Serial I/O (SIO) (LPSS)

Table 20. 1/O Supported Interfaces

| Interface | Number of Ports | Maximum Speed |
| :--- | :---: | :---: |
| [SIO] I ${ }^{2} \mathrm{C}^{*}$ | 8 | $3.1 \mathrm{Mb} / \mathrm{s}$ |
| [SIO] HSUART | 4 | $115,200 \mathrm{~kb} / \mathrm{s}$ (standard 16550) <br> $3.6864 \mathrm{Mb} / \mathrm{s}$ (high-speed 16750) |
| [SIO] SPI | 3 | $25 \mathrm{Mb} / \mathrm{s}$ |

### 3.6 Clocking

Table 21. Summary of Clock Signals

| dil Interface | Clock Signal | Clock Frequency |
| :---: | :---: | :---: |
| Memory - DDR3L | NOTE | NOTE |
| Memory - LPDDR4 | 3 NOTE | NOTE |
| PCle* | NOTE | NOTE |
| Storage - eMMC* 4.51 and 5.0 | NOTE | NOTE |
| Storage - SD Card | NOTE | NOTE |
| Storage - SDIO | SDIO_CLK | 25, 50, 100, 200 MHz |
| Display - DisplayPort, HDMI | NOTE | NOTE |
| Display - MIPI*-DSI | NOTE | NOTE |
| Camera - MIPI-CSI | $8^{\circ}$ NOTE | NOTE |
| Audio - Intel ${ }^{\text {® }}$ HD Audio | NOTE | NOTE |
| Audio Codec/Analog Microphone - I2S | AVS_I2S[1:6]_BCLK AVS_I2S[1:2]_MCLK | BCLK = <programmable> MCLK = <programmable> |
| Audio - Digital Microphone | NOTE | NOTE |
| SIO (LPSS) $I^{2} \mathrm{C}$ | NOTE | NOTE |
| PMIC | NOTE | NOTE |
| SVID | NOTE | NOTE |
| LPC | NOTE | NOTE |
| SMBus | NOTE | NOTE |
| SIO (LPSS) SPI | SIO_SPI_[0:2]_CLK | 25 MHz |
| FAST SPI - SPI NOR and TPM | NOTE | NOTE |
| SPI | NOTE | NOTE |
| Platform - OSC_CLK_OUT | - NOTE | NOTE |
| Platform - SUSCLK | NOTE | NOTE |
| XTAL Source - RTC Clock | NOTE | NOTE |
| XTAL Source - Processor <br> Clock - as default | NOTE | NOTE |

NOTE: Same as the N - and J-Series Processors.

### 3.7 Spread Spectrum Clocking for EMI mitigation

Spread Spectrum Clocking for Electrical Magnetic Interference is supported in Apollo Lake -I, up to a maximum down-spread amplitude of $0.5 \%$. The components affected by SSC are the following:

- DDR Memory
- HSIO interfaces (USB3, PCle, eDP, DP, eMMC, SD Card and SDIO)


### 3.8 Other Interfaces

For other interfaces that are not mentioned in this document, such as display controller, graphics and media engine, refer to Intel ${ }^{\circledR}$ Pentium ${ }^{\circledR}$ and Celeron ${ }^{\circledR}$ Processor N- and J- Series Datasheet Volume 1 of 3 (Document Number: 334817).

### 4.0 Electrical Specifications

Table 22 lists the Power Rail DC specifications and ICCMAX for the processor. Table 25 lists the DC specifications for SDIO. Refer to Intel ${ }^{\oplus}$ Pentium ${ }^{\oplus}$ and Celeron ${ }^{\oplus}$ Processor N and J- Series Datasheet Volume 1 of 3 (Document Number: 334817) for other electrical specifications.

### 4.1 Voltage and Current Specifications

Table 22. Power Rail DC Specifications and ICCMAX Values

| Power Type | Voltage Range (V) | Voltage Tolerance (AC+DC+Ripple) | Power Well Description | $I_{\text {CCMAX }}$ <br> (A) |
| :---: | :---: | :---: | :---: | :---: |
| VCC_VCGI | NOTE | With AVP: (NOTE) | NOTE | Refer to Table 2 and Table 4 |
|  |  | Without AVP: (NOTE) |  |  |
| VNN_SVID | NOTE (DDR3L) | NOTE | NOTE | 4.4 |
|  | NOTE (LPDDR4) | NOTE | NOTE | 2.9 |
| VCCIOA | NOTE | NOTE | NOTE | Included in either VNN_SVID (DDR3L) or VDDQ (LPDDR4) |
| VCCRAM_1P05 | NOTE | NOTE | NOTE | NOTE |
| VCCRAM_1P05_IO | NOTE | NOTE | NOTE |  |
| VCC_1P05_INT | NOTE | NOTE | NOTE |  |
| VDD2_1P24_GLM | NOTE | NOTE | NOTE | NOTE |
| $\begin{aligned} & \text { VDD2_1P24_AUD_ } \\ & \text { ISH_PLL } \end{aligned}$ | NOTE | NOTE | NOTE |  |
| VDD2_1P24_MPHY | NOTE | NOTE | NOTE |  |
| VDD2_1P24_USB2 | NOTE | NOTE | NOTE |  |
| $\begin{aligned} & \text { VDD2_V1P24_DSI_C } \\ & \text { SI } \end{aligned}$ | NOTE | NOTE | NOTE |  |
| VCC_1P8V_A | NOTE | NOTE | NOTE | NOTE |
|  | NOTE (DDR3L) | NOTE | NOTE | 2.8 |
|  | NOTE (LPDDR4) | NOTE | NOTE | $4.3$ |


| Power Type | Voltage <br> Range(V) | Voltage <br> Tolerance <br> (AC+DC+Ripple) | Power Well <br> Description | I <br> (A) <br> (A) |
| :--- | :---: | :---: | :---: | :---: |
| VCC_3P3V_A | NOTE | $+5 \%-6.5 \%$ | NOTE | NOTE |
| VCC_RTC_3P3V | 3.3 (coin <br> battery <br> backed) | NOTE | NOTE | 2 m (SO state) 6 |
| $\mu$ (G3 state) |  |  |  |  |

NOTE: Same as the N - and J- Series Processors.

Table 23. Intel Atom ${ }^{\oplus}$ Processor E3900 Series Vcc_ $_{\text {cGI }}$ Rail Iccmax Values

| SKU Name | IcCMAX (A) |
| :---: | :---: |
| E3950 | 16 |
| E3940 | 15 |
| E3930 | 10.5 |

Table 24. Intel Atom ${ }^{\ominus}$ Processor A3900 Series Vcc__ $_{\text {cGI }}$ Rail Iccmax Values

| SKU Name | $I_{\text {ccmax }}(A)$ |
| :---: | :---: |
| A3960 | 21 |
| A3950 | 16 |
| A3940 | 15 |
| A3930 | 10.5 |
| A3920 | 16 |

### 4.2 SDIO DC Specifications

Table 25. SDIO Signal Group DC Specifications

| Symbol | Parameter | Minimum <br> Value | Maximum <br> Value | Unit | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VCC | I/O voltage | 1.66 | 1.89 | V | 1.8 V nominal |
| VOH | Output high <br> voltage | 1.35 | - | V | At 1.80 V nominal <br> $($ Vcc- 0.45$)$, at 3 mA <br> load |
| VOL | Output low <br> voltage | - | 0.45 | V | At -3 mA load |


| Symbol | Parameter | Minimum Value | Maximum Value | Unit | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VIH | Input high voltage | 1.17 | - | V | At 1.80 V nominal ( $0.65 x \mathrm{xcc}$ ) |
| VIL | Input low voltage | - | 0.63 | V | At 1.80 V nominal ( 0.35 xVcc ) |
| CL | Bus signal line capacitance | $8^{\prime}$ | 5 | pF |  |
| IPAD | Pad leakage current | -5 | 5 | $\mu \mathrm{A}$ | - |
| ZUP | Driver pull-up impedance | 32 | $48$ | $\Omega$ | $40 \Omega$ nominal |
| ZDN | Driver pull-down impedance | 32 | $48$ | $\Omega$ | $40 \Omega$ nominal |
| Wpup20K | Weak pull-up impedance 20 K | $8$ | 44 | k $\Omega$ | $20 \mathrm{k} \Omega$ nominal |
| Wpdn20K | Weak pull-down impedance 20 K | 8 | 44 | k $\Omega$ | $20 \mathrm{k} \Omega$ nominal |
| Vhys | RX hysteresis | 100 | - | mV | - |
| Cin | Pad capacitance | - | 5 | pF | - |
| vos | Overshoot voltage magnitude [time duration for 200 $\mathrm{MHz}<0.4 \mathrm{~ns} \text { ] }$ |  | $2.15$ | V | (1), (2) |
| VUS | Undershoot voltage magnitude [time duration for 200 MHz < 0.4 ns ] | - | $-0.35$ | V | (1), (2) |
| vos | Overshoot voltage magnitude [time duration for 200 $\mathrm{MHz}<0.8 \mathrm{~ns}$ ] | $e^{8+1} e^{8}$ | $-0.35$ | V | (1), (2) |
| VUS | Undershoot voltage magnitude [time duration for 200 MHz < 0.8 ns ] | - | $2.1$ | V | (1), (2) |


| Symbol | Parameter | Minimum <br> Value | Maximum <br> Value | Unit | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VOS | Overshoot <br> voltage <br> magnitude <br> [time duration <br> for 200 MHz < <br> $1.25 \mathrm{~ns}]$ | - | -0.3 | V | (1), (2) |
| VUS | Undershoot <br> voltage <br> magnitude <br> [time duration <br> for 200 MHz <br> $1.25 \mathrm{~ns}]$ | - | 2.06 | V | (1), (2) |

## NOTES:

1. Activity Factor $=0.25$, that is, one out of four received cycles has the VOS/VUS.
2. $\mathrm{Tj}=105^{\circ} \mathrm{C}$

### 5.0 Ball Map, Processor Pin Locations, and Package Information

Table 26 compares the signal names of the N - and J- Series Processors to those of the E3900 and A3900 Series Processors. Refer to Intel ${ }^{\circledR}$ Pentium ${ }^{\circledR}$ and Celeron ${ }^{\circledR}$ Processor N- and J- Series Datasheet Volume 1 of 3 (Document Number: 334817) for other processor pin names.

Table 26. Signal Name Comparison between N- and J- Series Processors and E3900 and A3900 Series Processors

| PIN Number | N - and J- Series Processors | E3900 and A3900 Series Processors |
| :---: | :---: | :---: |
| AW48 | NCTF | MEM_CHO_ECC_DQO ${ }^{(N O T E)}$ |
| AW47 | NCTF | MEM_CHO_ECC_DQ1 ${ }^{(N O T E)}$ |
| BB43 | NCTF | MEM_CHO_ECC_DQ2 ${ }^{(\text {NOTE) }}$ |
| AW45 | NCTF | MEM_CHO_ECC_DQ3 ${ }^{(\text {NOTE) }}$ |
| AV48 | NCTF | MEM_CHO_ECC_DQ4 ${ }^{(\text {NOTE) }}$ |
| AV47 | NCTF | MEM_CHO_ECC_DQ5 ${ }^{(N O T E)}$ |
| BD43 | NCTF | MEM_CHO_ECC_DQ6(NOTE) |
| BA45 | NCTF | MEM_CHO_ECC_DQ7(NOTE) |
| BD47 | NCTF | MEM_CHO_ECC_DQS_P ${ }^{\text {(NOTE) }}$ |
| BB47 | NCTF | MEM_CHO_ECC_DQS_N ${ }^{(\text {NOTE) }}$ |
| AR21 | NCTF | MEM_CH1_ECC_DQO ${ }^{(\text {NOTE) }}$ |
| AT21 | NCTF | MEM_CH1_ECC_DQ1 ${ }^{(\text {NOTE) }}$ |
| AW23 | NCTF | MEM_CH1_ECC_DQ2 ${ }^{(N O T E)}$ |
| AW21 | NCTF | MEM_CH1_ECC_DQ3 ${ }^{(\text {NOTE }}$ |
| BA19 | NCTF | MEM_CH1_ECC_DQ4 ${ }^{(N O T E)}$ |
| AW19 | NCTF | MEM_CH1_ECC_DQ5 ${ }^{(\text {NOTE) }}$ |
| BA23 | NCTF | MEM_CH1_ECC_DQ6(NOTE) |
| BB23 | N NCTF | MEM_CH1_ECC_DQ7(NOTE) |
| BD23 | NCTF | MEM_CH1_ECC_DQS_P ${ }^{\text {(NOTE) }}$ |
| BE23 | NCTF | MEM_CH1_ECC_DQS_N ${ }^{(\text {Note })}$ |
| P58 | GPIO_166 | SDIO_CLK |


| PIN Number | N-and J-Series <br> Processors | E3900 and A3900 Series |
| :---: | :---: | :---: |
| Processors |  |  |

NOTE: Applicable to the DDR3L ECC option only

## 5.1 <br> Package Mechanical Drawing: Apollo Lake-I ${ }^{1}$

Figure 4. Package Mechanical Drawing: Apollo Lake-I ${ }^{1}$ (1 of 2)


Figure 5. Package Mechanical Drawing: Apollo Lake-I ${ }^{11}$ (2 of 2)


