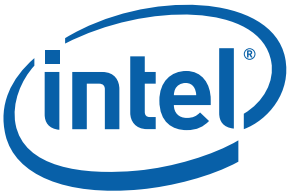

Techniques for Lowering Power Consumption in Design Utilizing the Intel® EP80579 Integrated Processor Product Line

Application Note

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Revision History

Date	Revision	Description
February 2010	003	Updated Table 5
May 2009	002	Update content in Table 1, Table 4, and Table 5
August 2008	001	Initial Release.

1.0 Introduction

This application note discusses techniques that are used to conserve power when using the Intel® EP80579 Integrated Processor Product Line (EP80579) in system platform designs.

1.1 Related Documents

Table 1. Related Documents

Document Title	Document Number
Intel® EP80579 Integrated Processor Product Line Datasheet	320066
Intel® EP80579 Integrated Processor Product Line Platform Design Guide	320068
Intel® EP80579 Integrated Processor Product Line BIOS Writers Guide	***Note:*** Contact your Intel Field Representative to obtain document

2.0 Overview

The EP80579 architecture is comprised of several functional units not all simultaneously utilized in all target applications. This application note describes the power savings achieved by utilizing the clock gating and IA-32 core throttling features designed into the EP80579.

By default, several internal functional units are brought out of reset with their respective clocks enabled. The clocks for these functional units are disabled on a per unit basis under BIOS control, by programming the IO_DEVICE_CONFIG register. Refer to the *Intel® EP80579 Integrated Processor Product Line BIOS Writers Guide* for additional details on the IO_DEVICE_CONFIG register.

Additionally it is feasible to configure the IA-32 core internal clock to throttle, to lower the aggregate frequency for lower data rate applications. This results in additional power savings for applications that do not require the IA-32 core to operate at the normal internal clock rate.

The power savings that is achieved using these features is presented within this document. These power saving techniques are used, in conjunction with the power management capabilities described in the *Intel® EP80579 Integrated Processor Product Line Datasheet,* to determine the total power consumption for a particular application.

3.0 Device Disabling

There are several internal functional units within the EP80579 that come up out of reset with their internal clocks enabled, but BIOS can be used to disable the units that are not utilized in the platform application. This allows applications that do not require the use of all of the hardware interface units to reduce the total platform power consumption. Devices are enabled/disabled by using the IO_DEVICE_CONFIG Register. BIOS uses this register to put unused devices into a powered down state. Devices that are disabled do not show up in the PCI configuration space, hence the IO_DEVICE_CONFIG Register has to be configured prior to PCI enumeration to avoid potential conflicts.

Table 2 provides a list of devices that are disabled with BIOS by using the IO_DEVICE_CONFIG Register.

Note: *Consult with your BIOS vendor to configure the IO_DEVICE_CONFIG register to disable any unused interface devices in your platform design.*

Table 2. Configurable Devices That Can be Disabled

Device	Description
PCIE1	PCI Express Port 1
PCIE0	PCI Express Port 0
SATA1	Serial ATA Port 1
SATA0	Serial ATA Port 0
GbE2	Gigabit Ethernet Port 2
GbE1	Gigabit Ethernet Port 1
GbE0	Gigabit Ethernet Port 0
USB1	Universal Serial Bus Port 1
USB0	Universal Serial Bus Port 0
CAN1	Controller Area Network Port 1
CAN0	Controller Area Network Port 0
TDM	Time Division Multiplex Ports (HSS)
SSP	Synchronous Serial Port

4.0 IA-32 core Throttling

The EP80579 provides the capability to force the IA-32 core to throttle, as a means to conserve power. The FORCE_THTL bit in the Processor Control Register (PROC_CNT) allows the BIOS to force the IA-32 core to throttle, independent of the ACPI software.

When the FORCE_THTL bit is set in the PROC_CNT register, the IA-32 core starts throttling, using the throttle ratio defined by the PROCHOT_DTY field in the PROC_CNT register. Alternatively, the ACPI software is also used to force throttling by setting both the THTL_EN and FORCE_THTL bits in PROC_CNT register. Under ACPI control, the throttle ratio is defined by the THTL_DTY field.

The throttling ratios results in stop clock (STOPCLK#) control signal to be set active for a minimum of 12.5% and a maximum of 87.5%. The period is 1024 PCI clocks. Thus, the STOPCLK# signal is active for as little as 128 PCI clocks or as much as 896 PCI clocks depending on the setting of the throttling ratio bits.

Table 3 shows the throttling control by using FORCE_THLT bit. Refer to the *Intel® EP80579 Integrated Processor Product Line Datasheet* for additional details on the throttling configuration options.

Table 3. Throttling Configuration with FORCE_THLT

PROCHOT_DTY Bits[2:0]	Throttle Mode ratio	PCI Clocks (STPCLK# low)
000	Default (50%)	512
001	87.5%	896
010	75.0%	768
011	62.5%	640
100	50%	512
101	37.5%	384
110	25%	256
111	12.5%	128

Note: The 3-bit PROCHOT_DTY field determines the duty cycle of the throttling when the FORCE_THTL bit is set. The duty cycle indicates the approximate percentage of time the STPCLK# signal is asserted while in the throttle mode. The STPCLK# throttle period is 1024 PCICLKs.

Throttling only occurs when the system is in the C0 state. When in the C2, C3, or C4 state, no throttling occurs. Once the PROCHOT_DTY field is written, subsequent writes have no effect until PLTRST# goes active.

4.1 IA-32 core Throttling Implementation and Effects

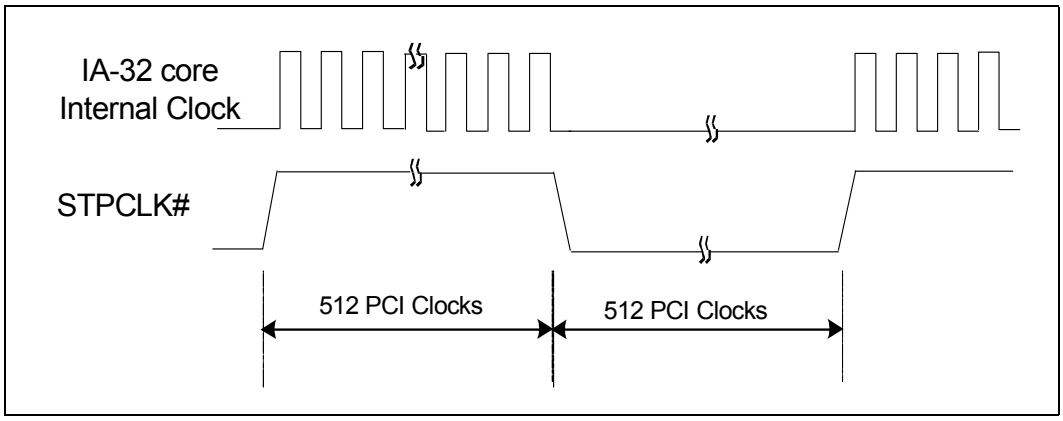
While throttling is enabled, the 'internal stop clock' (STOPCLK#) signal is asserted for some time, and then deasserted for some time. This modulation of the stop clock regulates the aggregate IA-32 core internal clock frequency. The exact times for assertion and deassertion of the internal clock is determined by the Throttle Mode ratios defined in Table 3.

When throttling is forced, the IA-32 core internal clock is limited in the amount of time it runs. For example, by setting the PROCHOT_DTY bits to '100' (or 50% Duty Cycle), the internal clocks only runs for 50% of the throttling period of 1024 PCI clocks, as shown in Figure 1.

During the time when Stop Clock is asserted (in other words, when the internal clock is not running), there is no code execution. However, interrupts are registered, as is all I/O activity. This is because the interrupt and I/O Controllers are not affected by the assertion of the "Internal Stop Clock".

In the case of an interrupt, this has the effect of extending the time it takes to run the interrupt service routine (ISR). In other words, at 50% throttling it takes an ISR that normally takes 1ms, up to 2ms to execute. These are considerations the developer must take into account when throttling the IA-32 core.

Figure 1. Clocks Relationship for 50% Throttling Ratio



4.2 Benefits of Throttling

The most significant benefit from throttling is that the overall power consumption of EP80579 is reduced, and thus allows the EP80579 to hit power envelopes that are not achieved otherwise.

4.2.1 Throttling Power Savings

Table 4 and Table 5 provide the percentage drop in total power consumption by the EP80579 when throttling is enabled.

Table 4 shows the percentages of total power savings per EP80579 SKU, by throttling the IA-32 core across the throttle ratio spectrum with all interface device units enabled.

Table 5 shows the percentages of total power savings per EP80579 SKU, by throttling the IA-32 core across the throttle ratio spectrum with the various interface units enabled or disabled during the test.

The percentage power savings values in Table 4 and Table 5 are referenced to the Thermal Design Power (TDP) value specifications for the EP80579 SKUs provided in the *Intel® EP80579 Integrated Processor Product Line Datasheet*. The TDP is a system design target associated with the maximum component operating temperature specifications. The TDP values are based on typical DC electrical specification and maximum component temperature for a realistic case application running at maximum utilization.

Both Table 4 and Table 5 indicate that the EP80579 SKU's power saving increases as the throttling ratio increases.

Note: It should be noted that the power saving values provided in Table 4 and Table 5 are for informational purposes only. Thermal solutions for EP80579-based platforms must be designed to meet the TDP values specified in the *Intel® EP80579 Integrated Processor Product Line Datasheet* and voltage regulators must be designed to meet specifications in the *Intel® EP80579 Integrated Processor Product Line Platform Design Guide*.

Table 4. Throttling Power Savings (All Interface Device Units Enabled)

EP80579 SKU		600 MHz	1066 MHz	1200 MHz
PROCHOT_DTY Bits	Throttle Mode (%)	EP80579 Total Power Saving (%)	EP80579 Total Power Saving (%)	EP80579 Total Power Saving (%)
001	87.5	21.0	47.6	42.8
010	75	18.8	40.7	37.2
011	62.5	16.3	36.2	32.1
100 or 000	50	13.3	29.4	26.5
101	37.5	9.4	22.8	20.2
110	25	6.7	15.9	15.6
111	12.5	5.0	9.5	9.8
N/A[1]	0	0	0	0

1. No throttling active

Table 5. Throttling Power Savings with Devices Enabled/Disabled

EP80579 SKU			600 MHz SKU	1066 MHz SKU	1200 MHz SKU
Device Configuration		PCIE1	Disabled		
		PCIE0	Disabled	**Enabled**	
		SATA1	Disableda		
		SATA0	Disabled		
		GbE2	Disabled		
		GbE1	Disabled	**Enabled**	
		GbE0	**Enabled**		
		USB1	**Enabled**		
		USB0	**Enabled**		
		CAN1	Disabled		
		CAN0	Disabled		
		TDM	Disabled		
		SSP	Disabled		
PROCHOT_DTY Bits	**FORCE_THTL Bit**	**Throttle Mode (%)**	**EP80579 Total Power Saving (%)**	**EP80579 Total Power Saving (%)**	**EP80579 Total Power Saving (%)**
001	1	87.5	30.4	53.0	43.8
010	1	75	28.5	46.8	38.3
011	1	62.5	26.3	42.8	33.3
100 or 000	1	50	23.7	36.7	27.9
101	1	37.5	20.3	30.8	21.6
110	1	25	17.9	24.7	15.6
111	1	12.5	16.3	18.9	9.8
XXX[1]	0[1]	0	11.9	10.4	1.8

1. The FORCE_THTL is used to turn on/off throttling. Therefore when FORCE_THTL is off the PROC_DTY bits are ignored and throttling is not enbled.

5.0 Power Management

The EP80579 is compatible with the *PCI Bus Power Management Interface Specification, Rev. 1.1*. It is also compatible with *Advanced Configuration and Power Interface (ACPI) Specification.* The EP80579 is designed to operate seamlessly with systems operating under these specifications.

5.1 Supported System Power States

The EP80579, like all systems, supports the S0 state. The EP80579 also supports S3 (STR- Suspend to RAM), S4 and S5 (Soft Off).

5.2 BIOS Support for Power Management

The EP80579 supports all PCI-to-PMI and PCI Express messaging required to place any subordinate device on any of its PCI Express ports into any of the defined device low power states. Peripherals attached to the PCI segments provided via a PXH component are placed in any of their supported low power states via messaging directed from the EP80579 through the intervening PCI Express hierarchy. BIOS designers for EP80579-based platforms must make allowances to support power-off device states within the PCI Express hierarchy.

6.0 Conclusions

The EP80579 architecture provides a flexible mechanism for managing power consumption. Although all the internal units come up enabled out of RESET, the EP80579 component provides BIOS the flexibility to disable those units that are not used by the design.

Additionally, BIOS can be used to configure the IA-32 core to operate at reduced internal clock frequencies for lower data rate applications by utilizing the IA-32 core throttling capability to reduce power consumption.

Finally, BIOS should make provisions to support the power management features provided by the part. All of these features provide the developer with options on how to minimize the overall power consumption of the application.

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