Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor: Boot-Up Options

Application Note

September 2004

Document Number: 254067-002

Contents

Tables

Revision History

Date	Revision	Description
September 2004	002	Updated Product Branding
December 2003	001	Initial release.

1.0 Introduction

1.1 Scope

This application note describes the configuration strapping options of the Intel® IXP42X product line and IXC1100 control plane processors during boot-up or reset. This document also describes how to configure user-defined values that will be read as part of the configuration strapping.

1.2 Related Documentation

Title	Document Number
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual	252480
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet	252479
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Specification Update	252702

2.0 Overview

The Intel® IXP42X product line and IXC1100 control plane processors use their expansion bus address lines as inputs when the processor comes out of reset during boot-up. The values on the bus can control the behavior of the processor (such as its clock frequency) or can be used as flags to indicate a certain configuration. The bit values present on the expansion bus address lines are latched into Configuration Register 0 of the Expansion Bus Controller when RESET_IN_N goes high (de-asserted). This register can then be read to determine the values that were present on the bus at boot-up and the configuration they indicate.

2.1 Configuration Register 0 Description

The following is a diagram of the Expansion Bus Configuration Register 0. It shows each of the bit fields as they have been defined during the time immediately following boot-up. Bits [23:0] are read from the values on the expansion bus address lines. Bits [31:24] are not read from the expansion bus. The memory map bit, bit 31, is predefined to a value of 1 whenever a boot-up or reset occurs.

Register Name:	**EXP_CNFG0**																										
Hex Offset Address:	0XC4000020								**Reset Hex Value:**	0x80000000																	
31	**30**						**24**	**23**	**22**	**21**	**20**			**17**	**16**									**6**	**5**	**4**	**3**	**2**	**1**	**0**
MEM_MAP	exp_config[30:24] **RESERVED**							CLK Bit 2	CLK Bit 1	CLK Bit 0	exp_addr [20:17] **USER CONFIG**			exp_addr[16:6] **RESERVED**									RES	PCI_CLK	RES	PCI_ARB	PCI_HOST	8/16

2.1.1 Memory Map Bit

After booting, this register can be read from and written to. Only the bits representing the clock frequency [23:21] cannot be written to; however, they still can be read. Care should be taken when writing to bit 31, the memory map bit. This bit controls the expansion bus's location in the memory map. While it is a 1, the expansion bus is located starting at 0x00000000 to 0x0FFFFFFF. When the bit is cleared, the expansion bus is at its normal location, 0x50000000 to 0x5FFFFFFF and the SDRAM is mapped back to the 0x00000000 location. The system should be ready to handle the switch of the memory map, as this could lead to unpredictable behavior if changed at an inappropriate time.

2.1.2 Core Clock Frequency Bits

Bits [23:21] may be used to under-clock a part from its factory-specified speed. To change the core clock speed of the device, refer to Table 1 for information about configuring the expansion bus clock bits [23:21]. Table 1 also shows the valid clock speed settings.

Table 1. Intel XScale® Core Speed Settings

Intel XScale® Core Speed (Factory Part Speed)	Cfg_en_n EX_ADDR(23)	Cfg1 EX_ADDR(22)	Cfg0 EX_ADDR(21)	Actual Core Speed (MHz)
533 MHz	1	0	0	533 MHz
533 MHz	0	0	1	400 MHz
533 MHz	0	1	1	266 MHz
400 MHz	1	0	0	400 MHz
400 MHz	0	1	1	266 MHz
266 MHz	1	0	0	266 MHz

2.1.3 PCI Configuration Bits

Bits 4, 2, and 1 each configure different aspects of PCI operation. Table 2 describes the function of each bit and its settings.

Table 2. PCI Operation Settings

Bit 4: PCI_CLK	Configure 66Mhz Mode of PCI Interface	0 = 33 MHz Mode 1 = 66 MHz Mode
Bit 2: PCI_ARB	Enables the PCI Controller Arbiter	0 = PCI arbiter disabled 1 = PCI arbiter enabled
Bit 1: PCI_HOST	Configures the PCI Controller as PCI Bus Host	0 = PCI as non-host 1 = PCI as host

Bit 4 can be read to determine if 66 MHz mode has been selected for the PCI bus. This bit must have a value of one if the PCI bus will be run in 66 MHz mode.

Bit 2 should be read to determine whether or not the PCI Arbiter is enabled or disabled. Upon de-assertion of reset, the value on the Expansion Bus Address Bus Bit 2 is used by the PCI Controller to configure the use of the internal arbiter.

Bit 1 should be read to determine whether or not the PCI Controller is configured as host. Upon de-assertion of reset, the value on the Expansion Bus Address Bus Bit 1 is used by the PCI Controller to set host or option operational mode.

2.1.4 Expansion Bus Device Data Bus Width

Bit 0 controls the width of the data bus to a memory device on the expansion bus. A value of 1 sets the data bus width to 8 bits, and a value of 0 sets the width to 16 bits.

2.2 User Configuration Field

2.2.1 Expansion Bus Configuration

On the Intel® IXP42X product line and IXC1100 control plane processors, the expansion bus address lines for the user config bit-field are internally pulled up. Users may then change the values by adding weak pull-down resistors (~10KΩ). Switches can also be used so that changeable values are available for the user configuration bits.

2.2.2 Practical Implementations

The user-defined bit-field can be used in many ways. For example, this field could be used for board-revision identification; a series of board revisions may be made over the course of development. To indicate a particular board revision, one of the 16 possible values can be encoded using the hardware configuration indicated in Section 2.2.1. Another potential use for this field would be to predefine a set of values to indicate a particular board configuration — for example, one with a different set of devices and memory map. Many other creative options, not identified in this document, are possible.